2-Channel Phase Delay

SLG47011

This application note describes how to create a signal delay equal to half of the input positive pulse (input signal Duty Cycle range is ~5%…50%) for two independent channels with an operation frequency range of ~200 Hz…200 kHz (first channel PIN3 ⟶ PIN7) and ~3 kHz…200 kHz (second channel PIN16⟶PIN6).

The design can be adjusted for different angle phase shifts and optimized to support a wide Duty Cycle range (however for one channel only) per customer request. Please contact Renesas if you are interested in such a solution. The application note comes complete with design files which can be found in the Reference section.

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1. Figures

2. References

Download our free Go Configure Software Hub [1] to open the *.aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-392 2-Channel Phase Delay.aap, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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3. Terms and Definitions

DFF D Flip-Flop
FSM Finite State Machine
LUT Look-Up Table
OSC Oscillator
SHR Shift Register

4. Introduction

The main goal of this application is to design a 2-channel Phase delay. The designed phase delay equal to half of positive pulse time for both independent channels and can operate across a wide range of frequencies ~200 Hz – 200 kHz (first channel PIN3⟶PIN7) and ~3 kHz…200 kHz (second channel PIN16 ⟶ PIN6). The current design implements two different approaches to creating a phase delay function using the SLG47011. The timing diagram below shows the design functionality principle. The first input clock doesn't produce any output, the 2nd output pulse is shifted to half compared to the input pulse. When the input signal frequency changes, a single next output pulse is shifted for the time of the previous input pulse, while all others are to half.

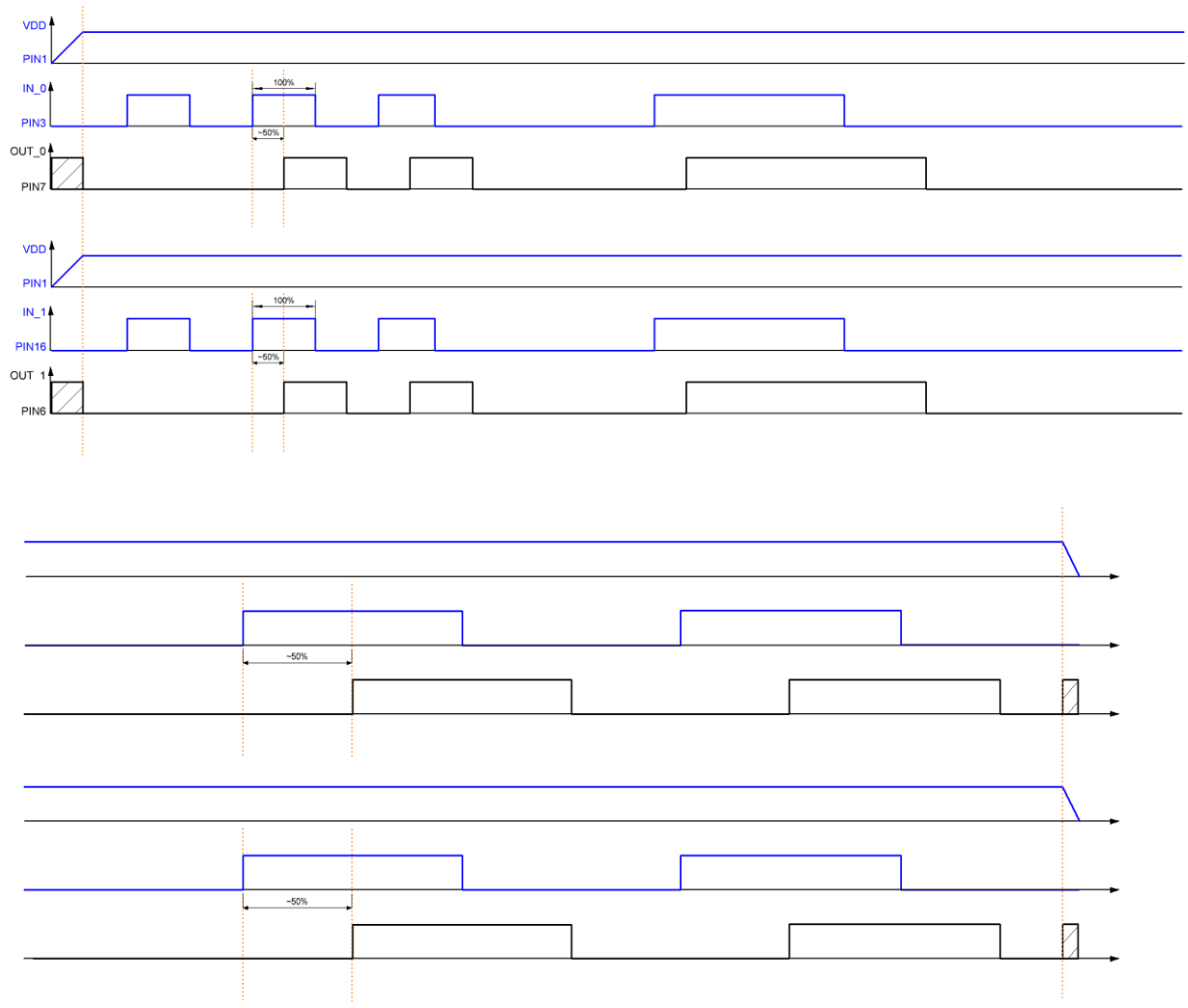

Figure 1. Timing Diagrams

5. Operating Principle

The first phase delay channel uses two FSM blocks (FSM0 and FSM1). There are two matrix inputs for Up and Keep to support FSM functionality. Any counter within the GreenPAK counts down by default. In FSM mode (CNT/DLY0 and CNT/DLY1) it is possible to reverse the counting by applying a High level to the Up input. Also, it is possible to pause counting by applying a High level to Keep input, and once the level goes Low, the counter will continue counting.

When the first pulse arrives at input PIN3, the FSM0 block starts to count (UP) with a fixed frequency of ½ OSC1. When PIN3 is HIGH, FSM0 counts up, and when LOW it stops counting (KEEP input signal). This block is reset by the rising edge at PIN3.

The FSM1 block has two fixed clock frequencies: OSC1 and ½ OSC1. Until the first pulse occurs at PIN3, the block is in the kept state (KEEP input is HIGH) and will be reset by a falling edge at PIN3. After the input PIN's falling edge, the FSM0 block starts to count (UP) with OSC1's frequency. Once the counted value exceeds the FSM0 counted value, 3-bit LUT22 with DFF13 will keep the value. After the second rising edge, FSM1 starts counting (DOWN) with ½ OSC1's frequency. Because both FSM blocks start counting toward each other (FSM0 – UP; FSM1 – DOWN) with the same frequency, the counted values will be equal at the halfway point of the input of the PIN3 pulse.

In the design, two Data Buffers (Data Buffer0, and Data Buffer2) are used for storing data from FSM0 and FSM1. Every rising edge at the LOAD input, the data buffer loads data from the source. If the LOAD signal comes from the internal source, then the matrix output operates as LOAD_EN. If LOAD_EN is HIGH, it enables LOAD from an internal connection. If LOAD_EN is LOW, it disables internal LOAD. Both of the data buffer blocks are configured in storage mode: new data buffer data is written in place of the oldest data in the data buffer according to the FIFO principle (first in first out).

The DCMP block periodically compares the values of Data Buffer0 and Data Buffer2, which have practically identical values to FSM0 and FSM1 data accordingly (there is a latency of five OSC1 clock cycles between data buffers from the buffer LOAD signal arrival to buffer READY signal asserting).

A 12-bit Memory Control Counter is used to control the address input of the Memory Table macrocell. It is configurated in full range mode (the address ranges from 0 to upper limit value).

SHR2 and 3-bit LUT6 are additional components of the design that provides the PIN7 LOW signal until the second input pulse arrives at PIN3.

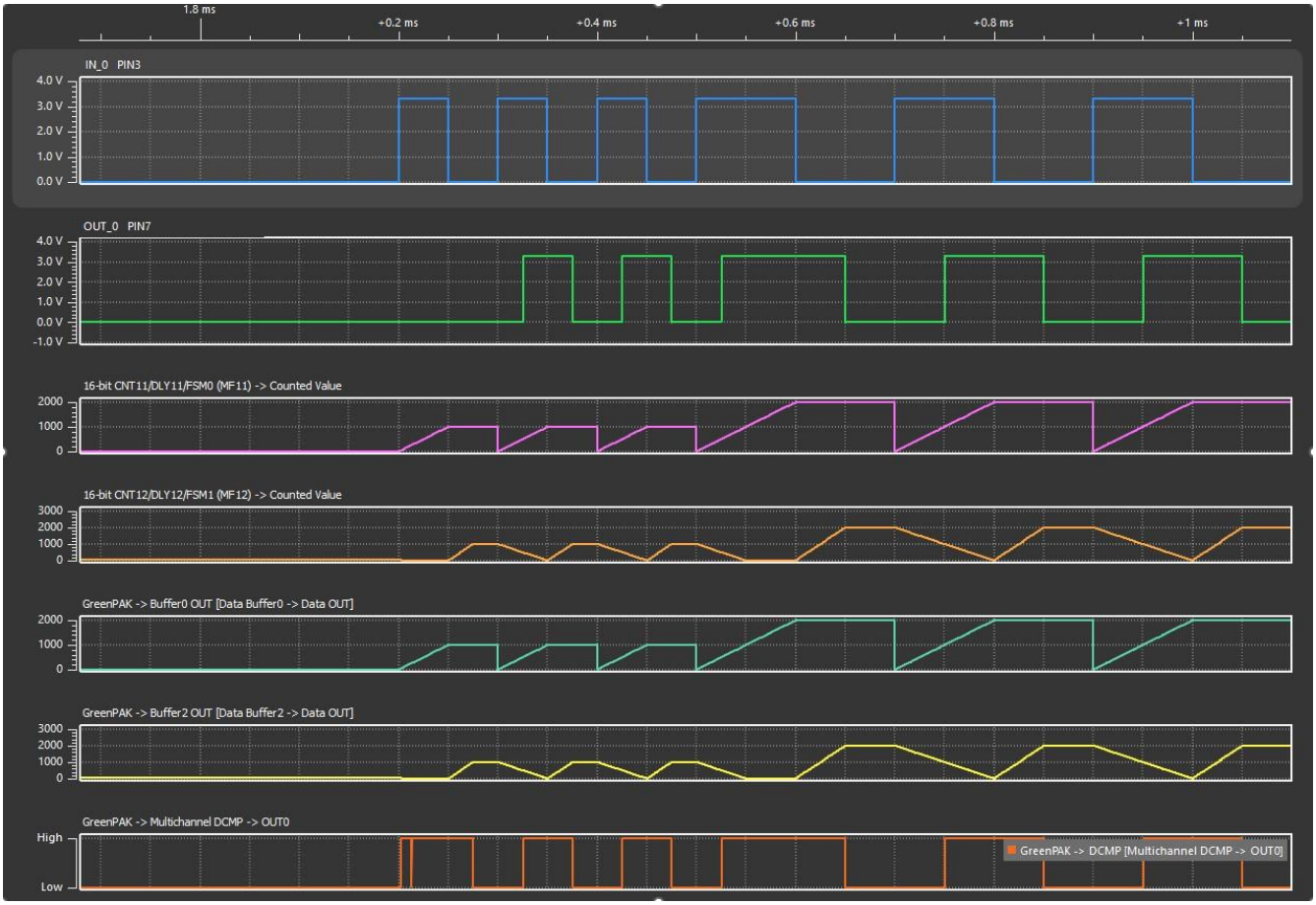

Figure 2. FSM Blocks Functionality Explanation (Simulation Result)

The main blocks that provide the functionality of the second phase delay channel are the Memory Control Counter, Memory Table, and 12-bit CNT/DLY9 Macrocell Dynamic Counter Data Change.

The Memory Control Counter inputs include the following:

- **Clock input** – provides a clock signal to the macrocell. It can be an external signal (from the connection matrix) or the output signal from one of the internal oscillators.
- **Up/Down input** – controls the increment (+1) or decrement (-1) of the current counter value.
- **Reset/Set input** –loads zero (Reset option) or the default counter data (Set option) to the counter.
- **Keep/Range select input** – stops the counter (Keep option) or selects one of two operation ranges (Range option, when two ranges mode is selected).

The current counter value of the memory control counter is changed by ±1 every clock pulse at the CLK input. The Up/Down input is used to select between incrementing (Up/Down is HIGH) or decrementing (Up/Down is LOW) the current CNT value.

The Memory Table macrocell is a memory block that consists of 4096 12-bit words. It has a 12-bit address and a 12-bit data port. The address of each particular word comes from the address input, and its content is available after some propagation delay and access time at the output. The maximum clock speed for the Memory Table is 20 MHz. The address input source for the Memory Table can be selected from the Memory Control Counter and the Data output is sent to DLY9.

The counter data of the 12-bit CNT/DLY9 macrocell can be dynamically changed with the data from the Memory Table macrocell. At power-up, the 12-bit CNT/DLY9 always loads its default CNT Data value from the NVM. New data will be loaded from the Memory Table to the CNT data after each CLK pulse at the LOAD input. In this design, CNT/DLY9 is configured in both edges delay mode.

When the input PIN16 (IN_1) is HIGH, the Memory Control Counter counts up and when LOW it is kept. This block is reset by the rising edge of the PIN16 (IN_1) input. Memory table data is configured so that each byte address is equal to its data. For example, Address: 0x00, Data: 0x00; Address: 0x01, Data: 0x01; Address: 0x02, Data: 0x02 … Address: 0xFFF, Data: 0xFFF. When the input PIN16 (IN_1) goes LOW, the data is loaded from the Memory Table according to DLY9's both edges delay, where its clock source is two times faster (OSC1) than the Memory Control Counter clock source (½ OSC1). Since DLY IN of DLY9 is connected to input PIN16 this gives a delay equal to half of the input positive pulse on the output PIN6.

6. GreenPAK Design

The GreenPAK Design is presented in Figure 3.

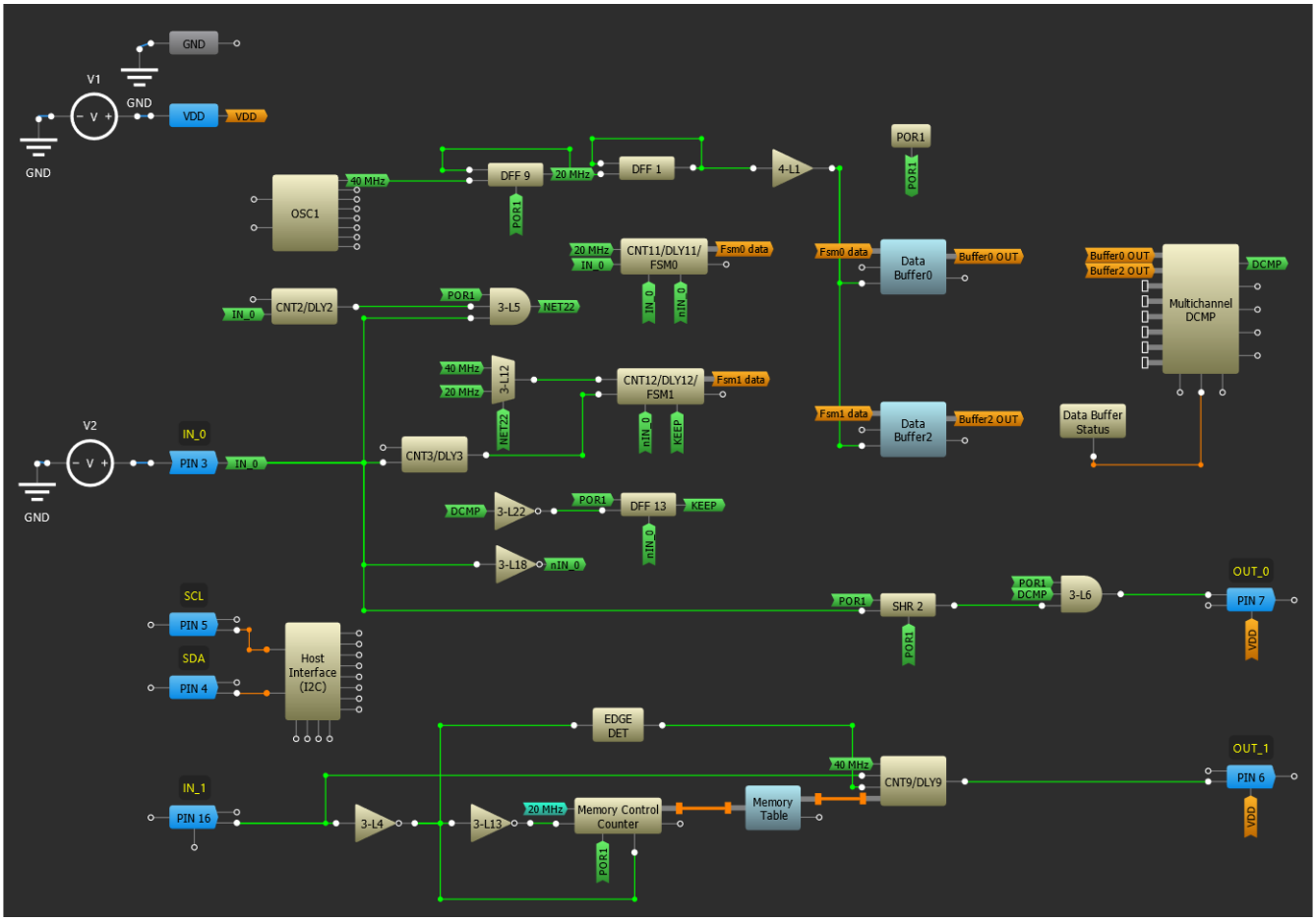

Figure 3: 2-Channel Phase Delay GreenPAK

7. Design Testing

Functionality of the first phase delay channel.

Channel 1 (yellow/top line) – PIN1 (VDD)

Channel 2 (light blue/2nd line) – PIN3 (IN_0)

Channel 3 (magenta/3rd line) – PIN7 (OUT_0)

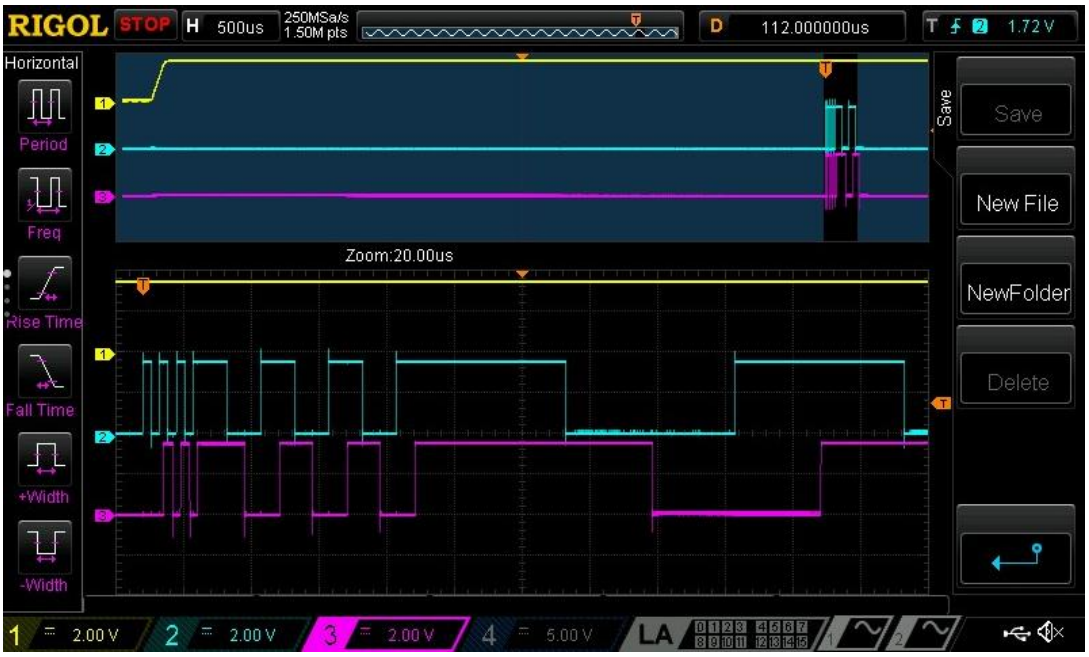

Figure 4. General Functionality Waveform

Figure 5. Operation at 200 kHz Input Frequency Waveform

The functionality of the second phase delay channel is the same.

Channel 1 (yellow/top line) – PIN1 (VDD)

Channel 2 (light blue/2nd line) – PIN16 (IN_1)

Channel 3 (magenta/3rd line) – PIN6 (OUT_1)

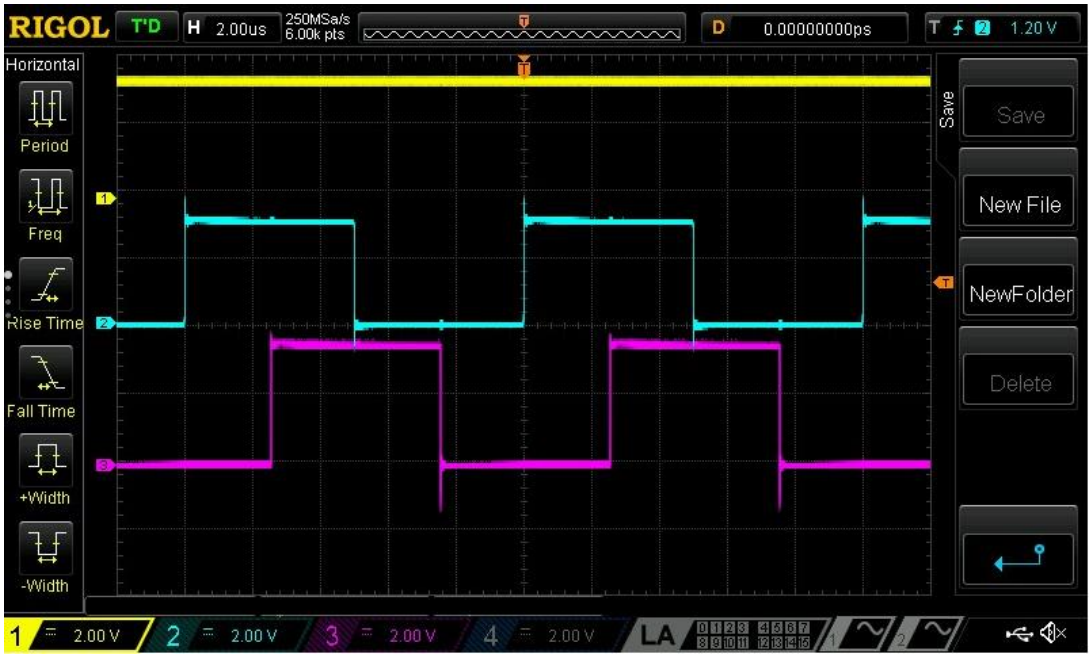

Figure 6. Operation at 100 kHz Input Frequency Waveform

8. Conclusion

The application note describes how to configure the SLG47011 to create a 2-Channel phase delay that's provides shifting equal to half of the positive pulse for two independent channels with a wide range of frequencies. The SLG47011 internal resources, including the FSMs, Data Buffers, Memory Control Counter, Memory control Table, oscillators, logic, and GPIOs are easily configured to implement the desired functionality for this design.

9. Revision History

Revision	Date	Description
1.00	Sep 24, 2024	Initial release.

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