ADC with Oversampling
SLG47011

This application note describes the oversampling function in the SLG47011 Analog-to-Digital Converter (ADC). The application note comes complete with design files, which can be found in the References section.

Contents

References

For related documents and software, please visit: AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-391 ADC with Oversampling.aap, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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1. Introduction

The Renesas SLG47011 IC features a 14-bit ADC. While 14-bit resolution often suffices, there are situations when higher accuracy is preferred. Specialized signal processing techniques like oversampling can be employed to enhance measurement resolution without the need for an external ADC. Oversampling, a feature of the SLG47011 Data Buffers designed to store or process the ADC data, allows for an increase in ADC resolution up to 15 bits or 16 bits.

2. Basics of Oversampling

2.1 Principle of Work

There are a couple of reasons for performing oversampling. This application note examines the case of when oversampling increases resolution. Instead of sampling an analog signal at the desired rate, it is sampled at a higher rate, so that additional samples can be used to compute a virtual result with higher accuracy than what a single real sample can provide.

For each additional bit of resolution, the signal must be oversampled by a minimum factor of four:

$$f_{OS} = 4^w f_s$$

where:

f_{os} – the oversampling frequency

w – the number of additional bits of resolution

f_s – the original sampling frequency.

It should be noted that the factor of four is the minimum value. In fact, a larger number of samples can be used to increase the resolution by one bit. To obtain the best possible representation of an analog input signal, oversampling to a significant degree is necessary. This is because a larger number of samples provide a more accurate representation of the input signal when averaged.

To increase the resolution, decimation must be performed after oversampling. Decimation is the averaging method, sometimes referred to as interpolation because it is used to produce new samples as a result of averaging a larger set of samples. During decimation, extra samples acquired from oversampling are incorporated. The result is right-shifted by n to scale the output correctly (equivalent to dividing by 2^n), where n represents the desired extra bits of resolution.

For example, if there is a need to increase the SLG47011 ADC resolution from 14 bits to 15 bits, the oversampling frequency should be $4^1 f_s$ or four times higher than the original sampling frequency and with n = 1. To achieve 16-bit resolution, f_{OS} should be $4^2 f_s$, that is, 16 times higher than the original frequency and with n = 2 respectively.

Increasing the resolution from 14 bits to 15 bits requires the summation of four 14-bit values. This summation produces a 16-bit result, where the last two bits are not expected to contain valuable information. To return to a 15-bit value, scaling the result by dividing it by 2 is necessary. Figure 1 shows a block diagram of this procedure.

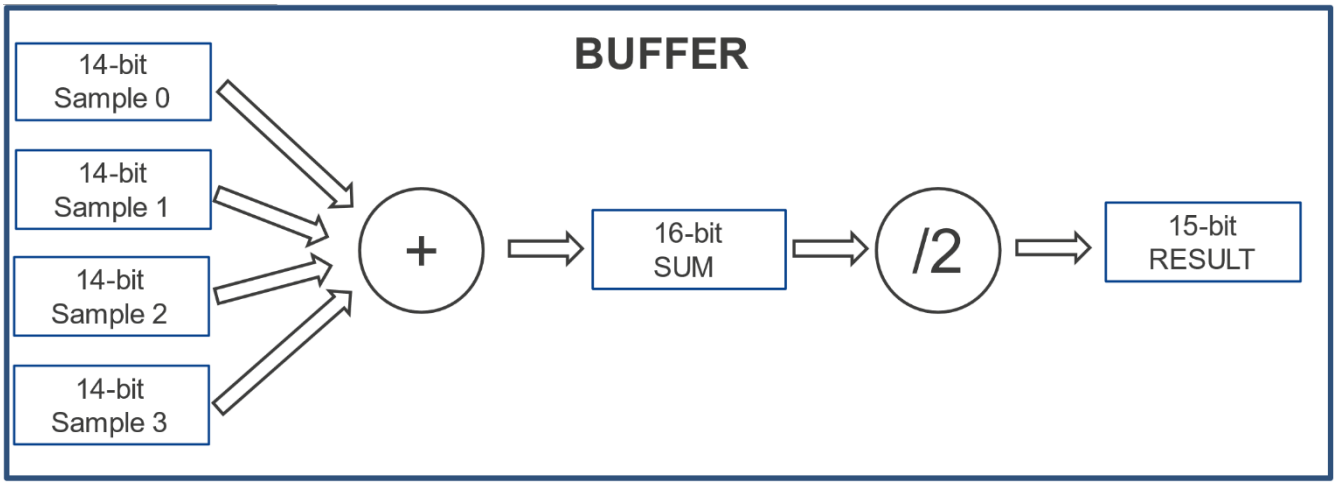


Figure 1. Oversampling Block Diagram in SLG47011 Data Buffer

2.2 Impact on Performance

The quality of a digital representation for an analog signal is closely tied to the resolution of the ADC, exerting a substantial impact on its overall performance. Higher resolution reduces quantization error, the difference between the true value of the analog signal and its digital representation. Additionally, higher resolution increases the ADC dynamic range, defined as the ratio between the largest and smallest signals that can be precisely measured. The extended dynamic range enables the ADC to detect smaller changes even in the presence of signals with large amplitude. Higher resolution boosts signal-to-noise ratio (SNR) because the noise level, which is brought on by quantization error, is reduced while the signal intensity range is maintained.

However, the use of high resolution is not always appropriate. Increasing the resolution also leads to a decrease in the sampling rate, which is critical for the conversion of high-frequency signals.

The SLG47011 supports a maximum sample rate of 1 Msps. The equation below shows the maximum sampling rate when the resolution is increased by 1 bit to 15-bit:

$$f_s = \frac{1\text{Msps}}{4^1} = 250\ \text{ksps}$$

And when increasing the resolution by 2 bits to 16-bit, the maximum sampling rate is:

$$f_s = \frac{1\ \text{Msps}}{4^2} = 62.5\ \text{ksps}$$

3. Oversampling in SLG47011 ADC

3.1 GreenPAK Design

Figure 2 shows an internal design, which demonstrates the SLG47011 ADC oversampling in the Go Configure software.

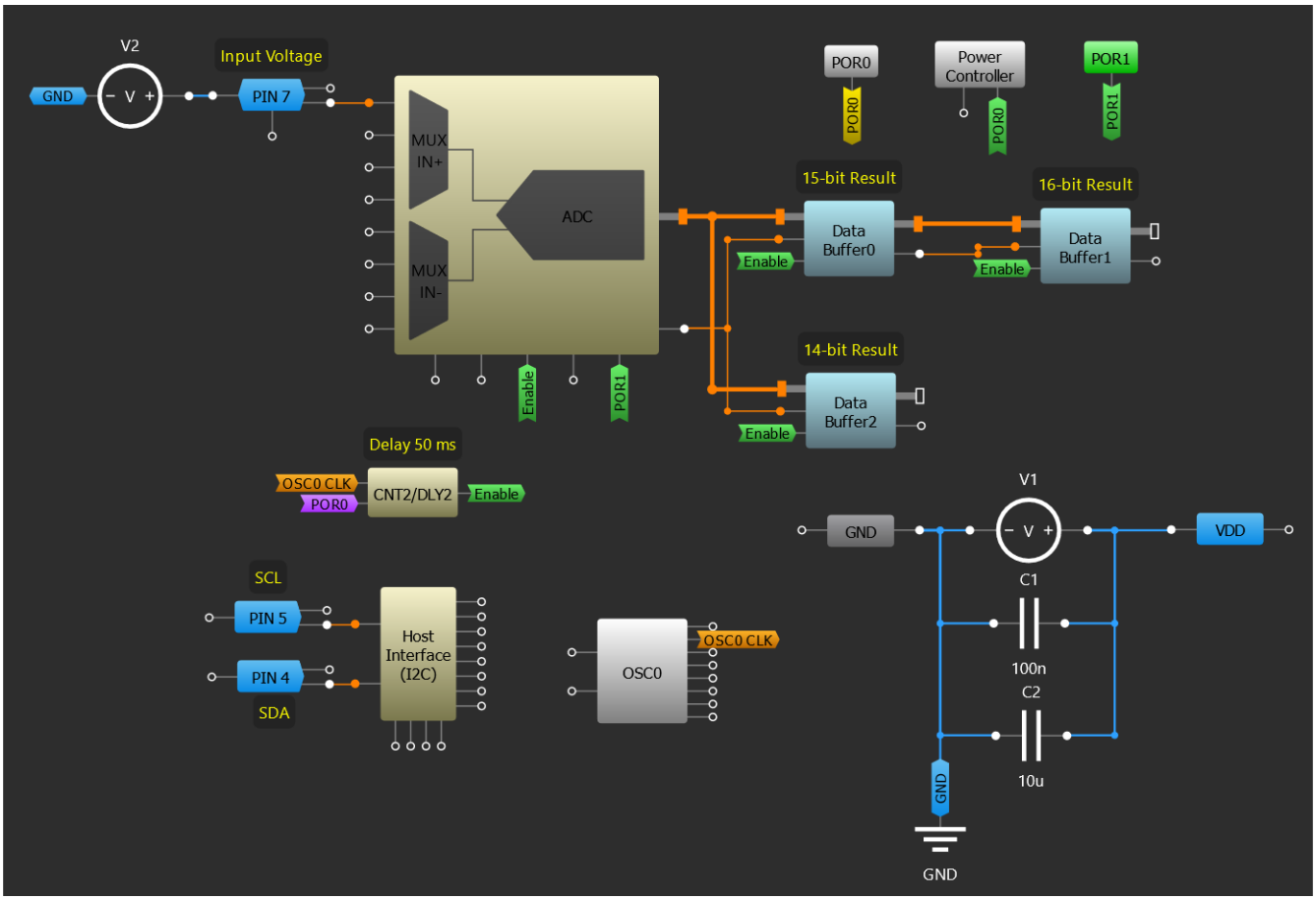


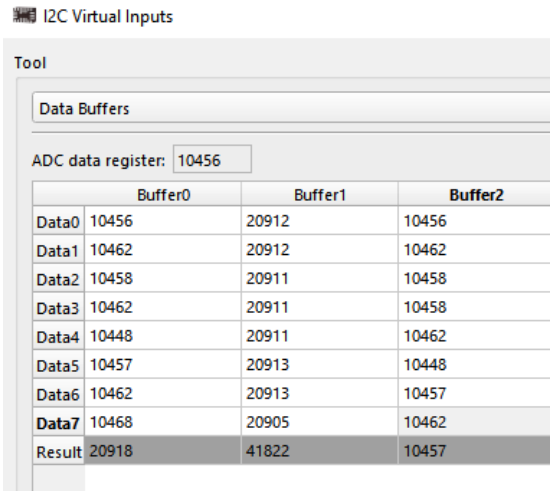
Figure 2. Go Configure Schematic of ADC Oversampling

In the GreenPAK SLG47011, oversampling is implemented with the help of Data Buffers. In this application note, Data Buffer 2 operates in Moving Average Mode using eight words for averaging. This mode involves conventional averaging by adding eight 14-bit samples and dividing the result by eight. This averaging reduces noise and flattens out peaks in the input signal, but it does not increase the resolution.

On the other hand, Data Buffer 0 functions in Oversampling mode. Oversampling mode is only available for buffer lengths of 4 or 8, as 4 samples are the minimum required to increase the resolution by 1 bit. As mentioned earlier, 8 samples make it possible to reduce oversampling noise, providing a more accurate representation of the input signal. However, this comes at the cost of a further reduced sampling rate. In this design, after the oversampling using 4 words and the decimation procedure, Data Buffer 0 stores the measured input signal with a 15-bit resolution, but the sampling rate is restricted to 250 ksps. Data Buffer 0 and Data Buffer 1 are connected in a daisy chain. This allows Data Buffer 1 to use the oversampled 15-bit result of Data Buffer 0 and perform further oversampling and decimation on it, increasing the resolution to 16 bits.

To initiate the ADC conversion, it is necessary to provide a delay, which is achieved using a 50 ms delay (DLY2).

Figure 3 shows the Data Buffers values in the Go Configure Tool after reading I²C Virtual Inputs at an input voltage of 1 V for Data Buffer 0 (with 4x oversampling), Data Buffer 1 (with 16x oversampling), and Data Buffer 2 (without oversampling).



	Buffer0	Buffer1	Buffer2
Data0	10456	20912	10456
Data1	10462	20912	10462
Data2	10458	20911	10458
Data3	10462	20911	10458
Data4	10448	20911	10462
Data5	10457	20913	10448
Data6	10462	20913	10457
Data7	10468	20905	10462
Result	20918	41822	10457

Figure 3. Data Buffers Values in the Go Configure Tool at 1 V Input Voltage

3.2 Design Simulation

The design was simulated in the Go Configure Simulation Tool. Figure 4 shows simulation waveforms with ADC oversampling.

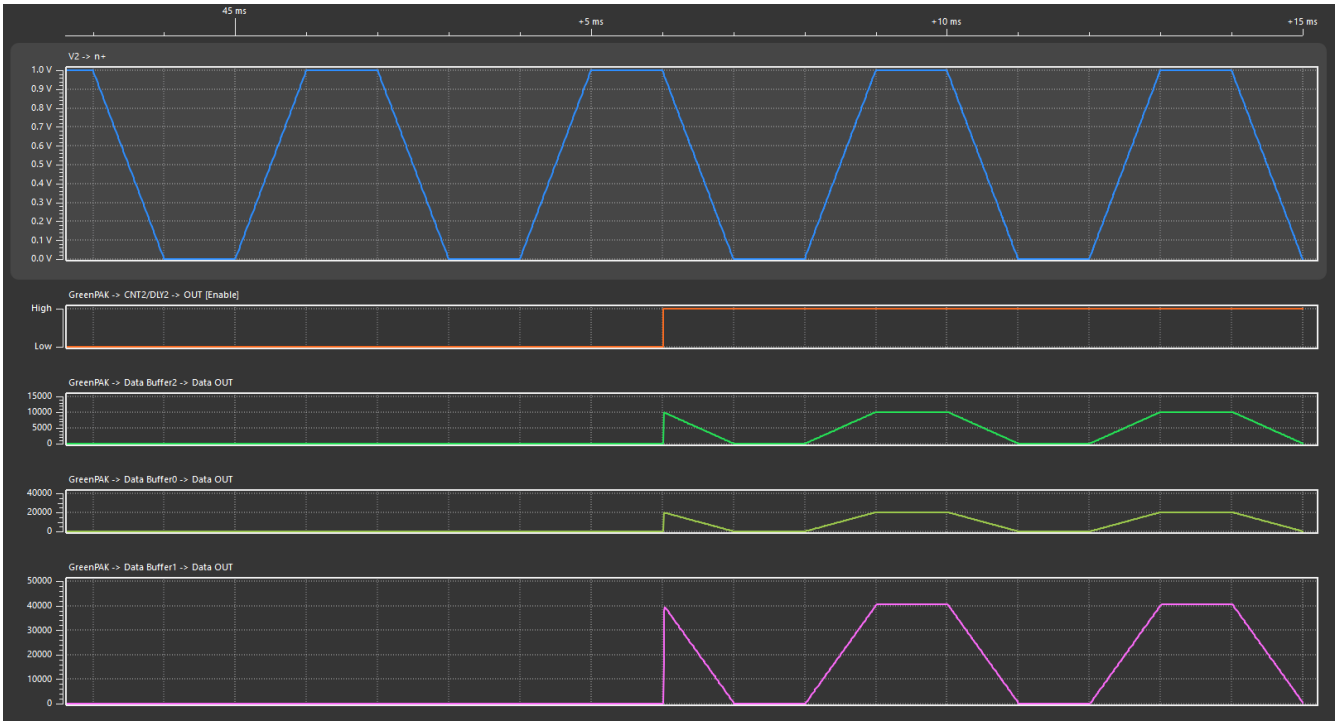


Figure 4. Simulation Waveforms Illustrating ADC Oversampling

3.3 Applications

There are a couple of applications for the SLG47011 ADC oversampling:

1. Oversampling enables the ADC to function as a 15-bit or 16-bit ADC in designs that require high accuracy but when the sampling rate is not critical.
2. Because in the design given in this application note the analog signal is available in 14-bit, 15-bit, and 16-bit representations, it becomes feasible to read one of the digitized values via I^2C, based on the frequency of the input signal. A more suitable 14-bit value can be requested for a high-frequency signal, whereas a 16-bit value can be chosen for a low-frequency signal.

3. Oversampling is useful in scenarios where initial system requirements, such as 14-bit resolution, evolve to necessitate increased resolution. A notable historical example relates to the development of Audio CD. There was considerable debate between an audio electronics manufacturer, advocating for 16-bit quantization, and another favoring 14-bit. Despite the second manufacturer having already developed a 14-bit Digital-to-Analog Converter (DAC), the competitor's preference for 16-bit prevailed. However, they innovatively achieved 16-bit quality using oversampling for its 14-bit DAC.

4. Conclusions

This application note describes an oversampling technique to increase the resolution of the ADC, its advantages and disadvantages, and how it is implemented in the SLG47011. Also, oversampling in the SLG47011 allows to get a flexible design, where the customers can change the resolution of the ADC depending on their needs and even when system requirements change. Furthermore, the SLG47011 features low power consumption and a compact package of only 2.0 mm x 2.0 mm.

5. Revision History

Revision	Date	Description
1.00	Sep 23, 2024	Initial release.

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