Maximum Power Point Tracker
SLG47011

This application note describes how to create a Maximum Power Point Tracking System for a 12 V solar panel. It also shows how to control the DC Buck converter for charging a 3.7 V battery using AnalogPAK SLG47011.

The application note comes complete with design files which can be found in the Reference section.

Contents

Figures

1. Terms and Definitions

DFF	D Flip-Flop
LUT	Look-up Table
MF	Multi-function
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
OSC	Oscillator
PV	Photovoltaic

2. References

For related documents and software, please visit: AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure Software Hub, Software Download, and User Guide
[2] AN-CM-390 Maximum Power Point Tracker.aap, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47011 Datasheet, Renesas Electronics
[6] SLG47115 Datasheet, Renesas Electronics

3. Introduction

The main goal of this application note is to create the MPPT of a 12 V solar panel controller for a DC Buck converter to charge a 1-cell 3.7 V battery using the AnalogPAK SLG47011.

The Maximum Power Point Tracking (MPPT) is an algorithm for continuously adjusting the impedance of a solar cell so that a photovoltaic (PV) system operates at or near the peak power point of the PV panel under various conditions, such as changes in solar radiation, temperature, and load. The MPPT method is more efficient than the standard PWM method, which regulates the output voltage regardless of the solar panel's power, which in turn leads to large energy losses.

The GreenPAK design algorithm consists of two parts: maximum power scanning and maximum power operating. During the scanning, SLG47011 goes through all duty cycles and remembers amongst of them at position did the panel worked at maximum power. Then during the operating part, the chip sends the PWM with this only duty cycle value to the Buck converter and monitors the battery charging current and voltage not to overrate.

4. Basic MPPT

4.1 Operating Principle and GreenPAK Design

The MPPT Controller Block Diagram is shown in Figure 1.

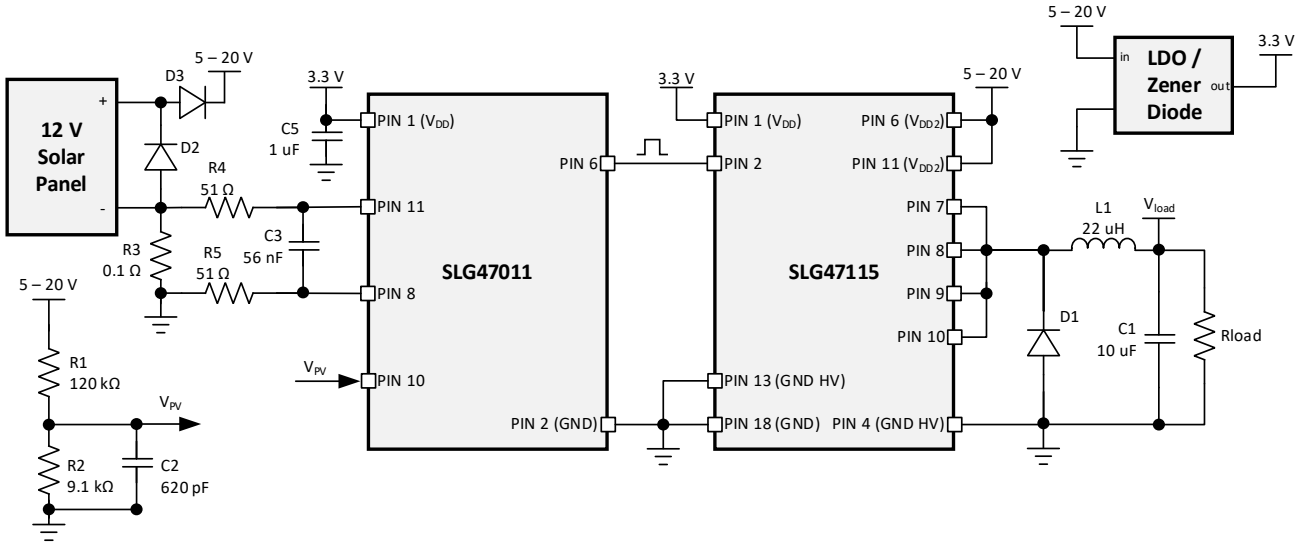

Figure 1. MPPT Controller Circuit Diagram

The design consists of MPPT and Buck Converter parts.

For the Buck Converter, the SLG47115 was chosen. It allows to decrease in the number of external components (MOSFET Driver + High Side NFET) to only one tiny package chip. The switching signal is received from SLG47011 by PIN 2 of SLG47115. Then this signal goes to HV OUT CTRL (Half Bridge), which drives the Buck Converter.

The chips' power supply V_{DD} of 3.3 V can be provided by converting the voltage of the solar panel through an LDO or a Zener diode. Total V_{DD} group current consumption during the charging process is less than 2 mA.

The GreenPAK Design is shown in Figure 2.

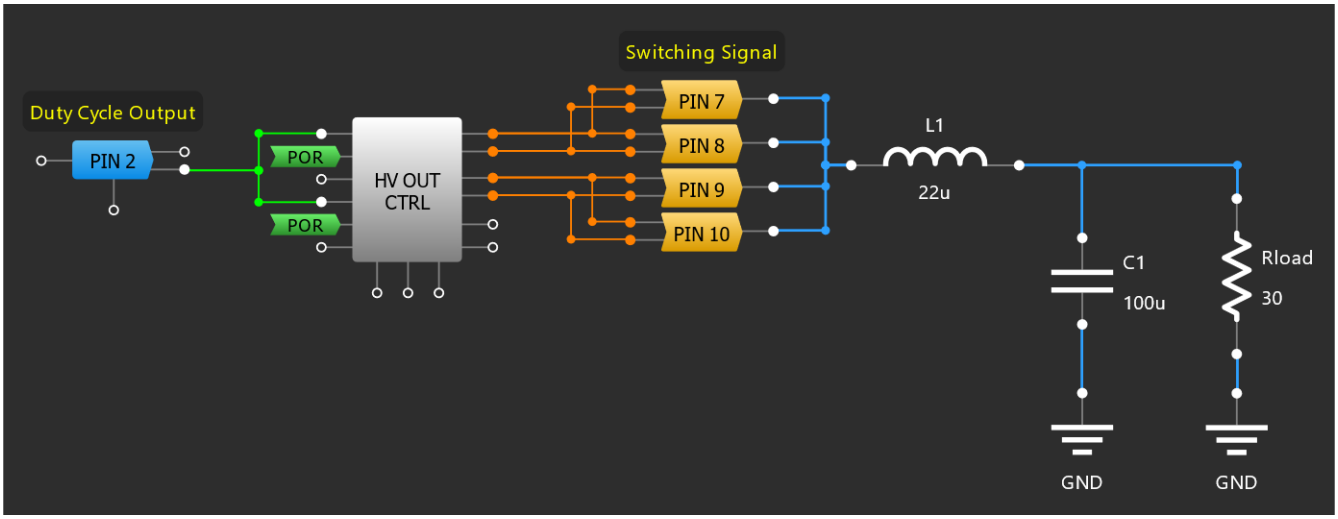

Figure 2. Buck Converter Driver GreenPAK Design (SLG47115)

The MPPT part, in turn, has two modes: Max Power Scanning and Max Power Operating.

During the Max Power Scanning mode, the SLG47011 generates a signal with a frequency of 200 kHz with a different duty cycle starting from 75% and ending at 10%. Please take note that the maximum and minimum values of the duty cycle were selected according to the results of the testing and can change depending on the chosen solar panel, battery, buck driver, and so on.

SLG47011 measures the solar panel voltage and current. Then the panel power is calculated and compared with the maximum power at each duty cycle. Suppose the power at a given duty cycle is greater than the current maximum power value, in that case, the maximum value is overwritten, and the duty cycle value is saved for the Max Power Operating mode.

The SLG47011 output signal goes to SLG47115 PIN 2, which enables the Half Bridge to drive the Buck converter with a load.

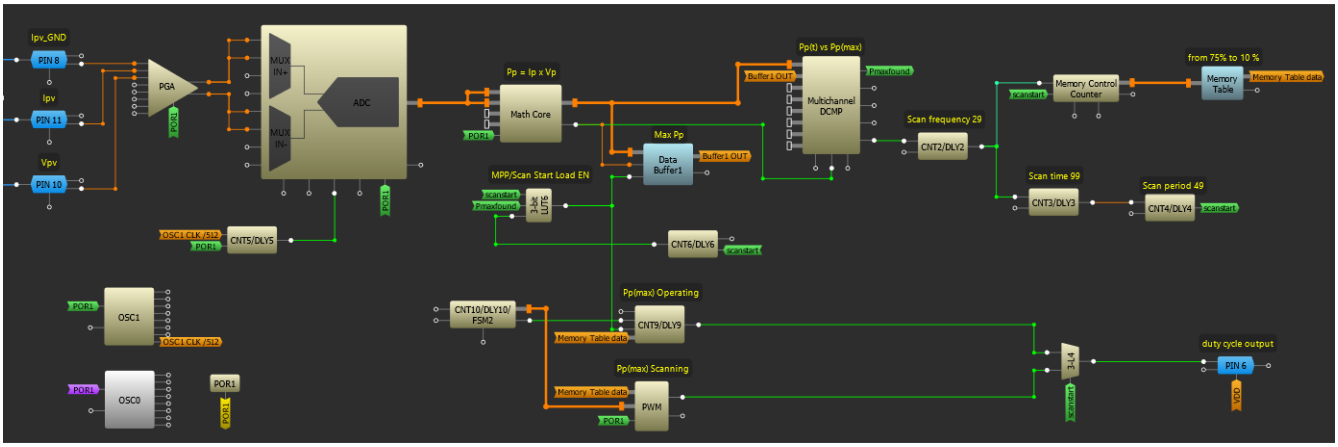

Figure 3. Basic MPPT GreenPAK Design (SLG47011)

Memory Control Counter clocks the Memory Table, where the counter data is stored for PWM block (**Max Power Scanning**) and CNT9/DLY9 (**Max Power Operating**). The PWM block and CNT9/DLY9 are clocked with CNT10/DLY10/FSM2. So, during the Scanning mode, PWM provides duty cycles from 75% to 10% with a 5% step. This duty cycle goes to the output PIN 6 of the SLG47011 and the input PIN 2 of the SLG47115, which drives the Buck converter. For each duty cycle, we measure the power of the solar panel.

The CNT5/DLY5, configured as a Delay, is used to turn on the ADC after the first turn-on when the POR arrives, as well as in further work when turning on and off the ADC from the POR signal.

The solar panel's current sense (PIN11) signal I_{pv} comes to the differential input (IN– source) of the PGA Channel 0. IN+ source of Channel 0 is PIN 8. Channel 0 Mode is $V_{ref}/2$ biased diff amp diff out, so the final value will be 2048± measured values depending on the positive/negative value. Channel 0 Gain – 4x.

To measure a solar panel voltage, there is the V_{pv} signal from the resistive divider (PIN 10) that comes to the single-ended input of the PGA Channel 1.

Then these signals go to ADC with V_{ref} = 1.62 V, which measures 1 sample of each signal. Consider the closed-loop bandwidth (GBWP/Gain) when setting the delay time. See more in datasheet section 3.8 Programmable Gain Amplifier Specifications.

ADC has a 12-bit resolution, so the maximum value of the V_{pv} is 4095, and the maximum I_{pv} is 3160.

The value of measured voltage is:

$$V_{PVdec} = V_{PV} \cdot \frac{4095}{1620},$$

where 1620 – V_{ref}, mV,

V_{pv} – measured solar panel voltage, mV.

Value of measured current:

$$I_{PVdec} = 2048 + I_{PV} \cdot 4 \cdot \frac{4095}{1620},$$

where 1620 – V_{ref}, mV,

2048 – $V_{ref}/2$, dec,

4 – Gain,

I_{pv} – measured solar panel current x sense resistor of 0.11 Ohm, mV.

To measure a solar panel's power, Ip, and Vp signals after sampling in ADC, go to MathCore which is configured as “Multiplier” with the output formula:

MathCore OUT = K x X,

Where K – ADC channel 0 (Ip),

X – ADC channel 1 (V_{pv}).

Since the maximum calculated value exceeds 4095, a right shift of 12 bits is applied. Accordingly, the maximum possible value is 4095 x 3160 / 2^12 = 3160.

After calculating the power, it is compared in DCMP with the maximum power stored in Data Buffer1 (initially 0). If the power value at the MathCore output is greater than the power value in Data Buffer1, a high signal is sent to the load enable input of Data Buffer1, which allows recording a new maximum value corresponding to a specific duty cycle from a Memory table. The duty cycle at this maximum power is maintained on the CNT9/DLY9 output during the **Max Power Operating** mode.

CNT2/DLY2 forms the scan frequency – Memory Control Counter clock.

CNT3/DLY3 sets the scan time and should be equal to the Memory Table size, CNT10/DLY10/FSM2 counter data, and Memory Control Counter Upper Limit.

CNT4/DLY4 sets the Max Power Operating Time as (Max Power Scanning Time x CNT Data – 1). This signal switches the 3-bit LUT4 Multiplexer and resets the Memory Control Counter to the initial value for the new scanning.

CNT4/DLY4 output is connected to CNT6/DLY6 (One shot) DLY IN, which in turn sends the 100 µs HIGH pulse to Data Buffer1 Load EN input through 3-bit LUT6 at each scanning beginning to set Data Buffer1 with the first calculated power value.

4.2 Design Testing

The design was tested for three different loads – 30, 40, and 50 Ω. Figure 4, Figure 6, and Figure 8 show the dependence of the panel Ppv (in green) and load Pload (in red) power on the duty cycle. Figure 5, Figure 7, and Figure 9 show the result of maximum power scanning – the duty cycle at maximum power point.

Channel 1 (yellow / 1st line) – SLG47011 PIN 6 (Duty Cycle Output).

Channel 2 (light blue / 2nd line) - V_{load}.

R_{LOAD} = 30 Ω

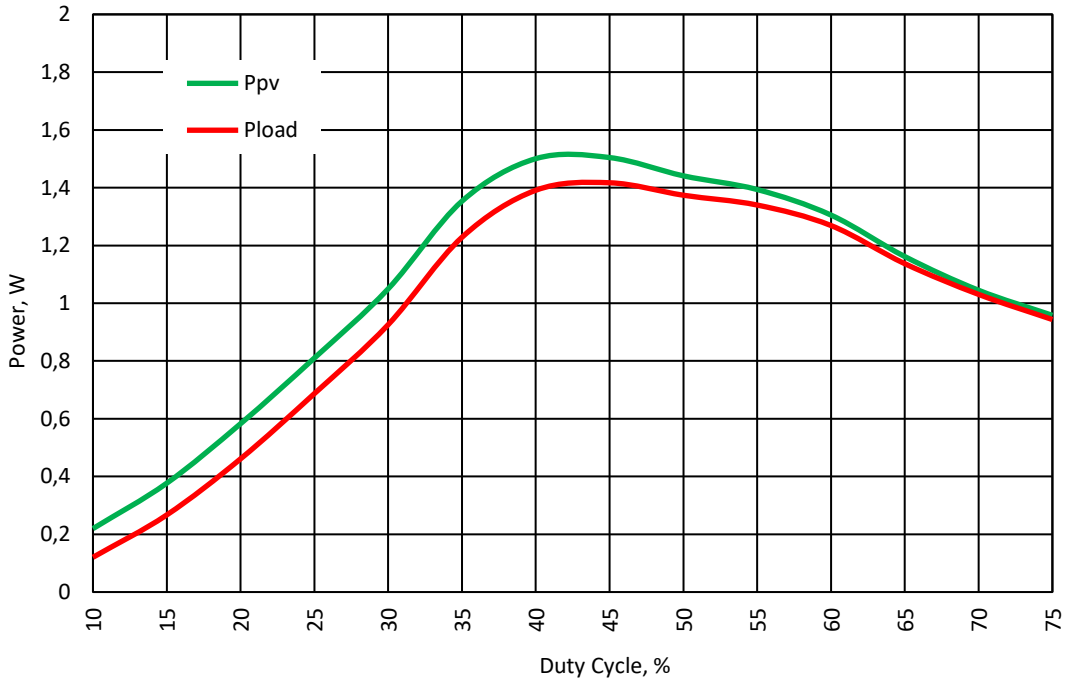

Figure 4. Power vs. Duty Cycle @ R_{LOAD} = 30 Ω

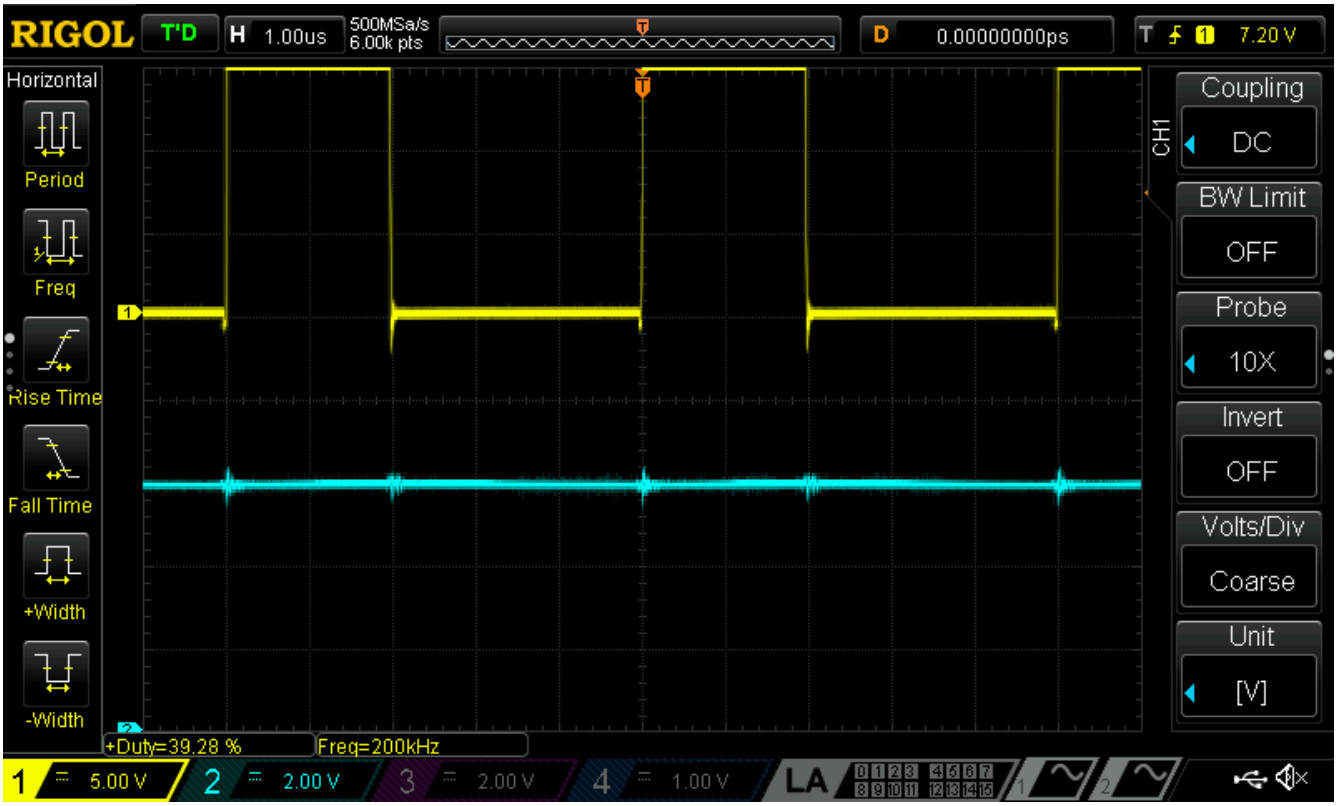

Figure 5. Duty Cycle at MPP @ R_{LOAD} = 30 Ω (yellow), V_{LOAD} (blue)

R_{LOAD} = 40 Ω

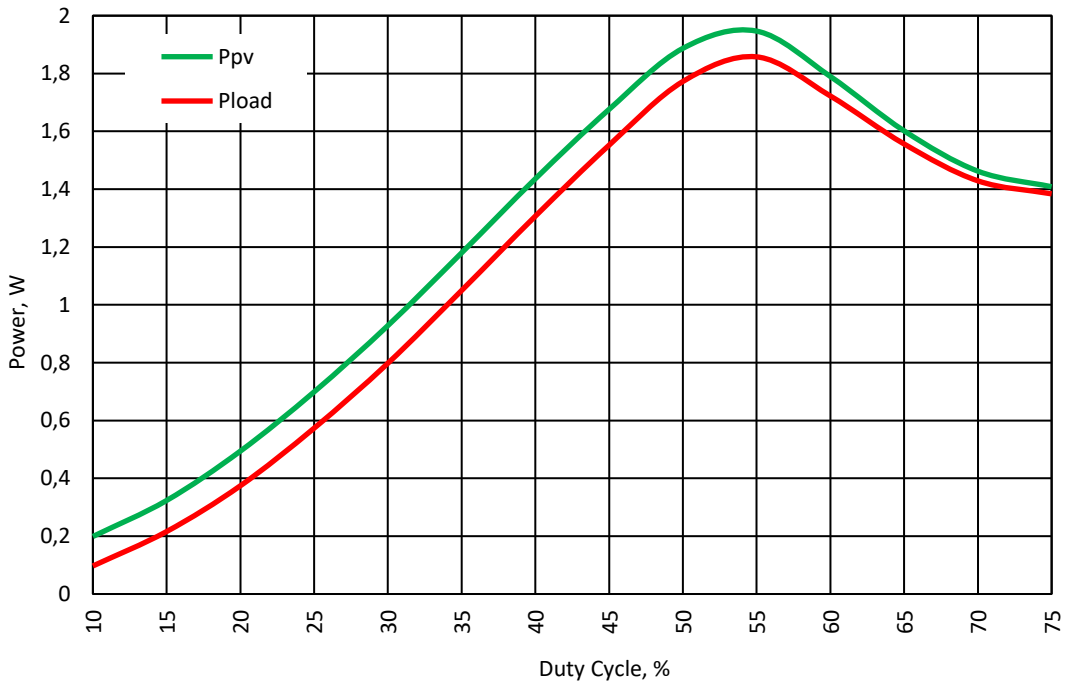

Figure 6. Power vs. Duty Cycle @ R_{LOAD} = 40 Ω

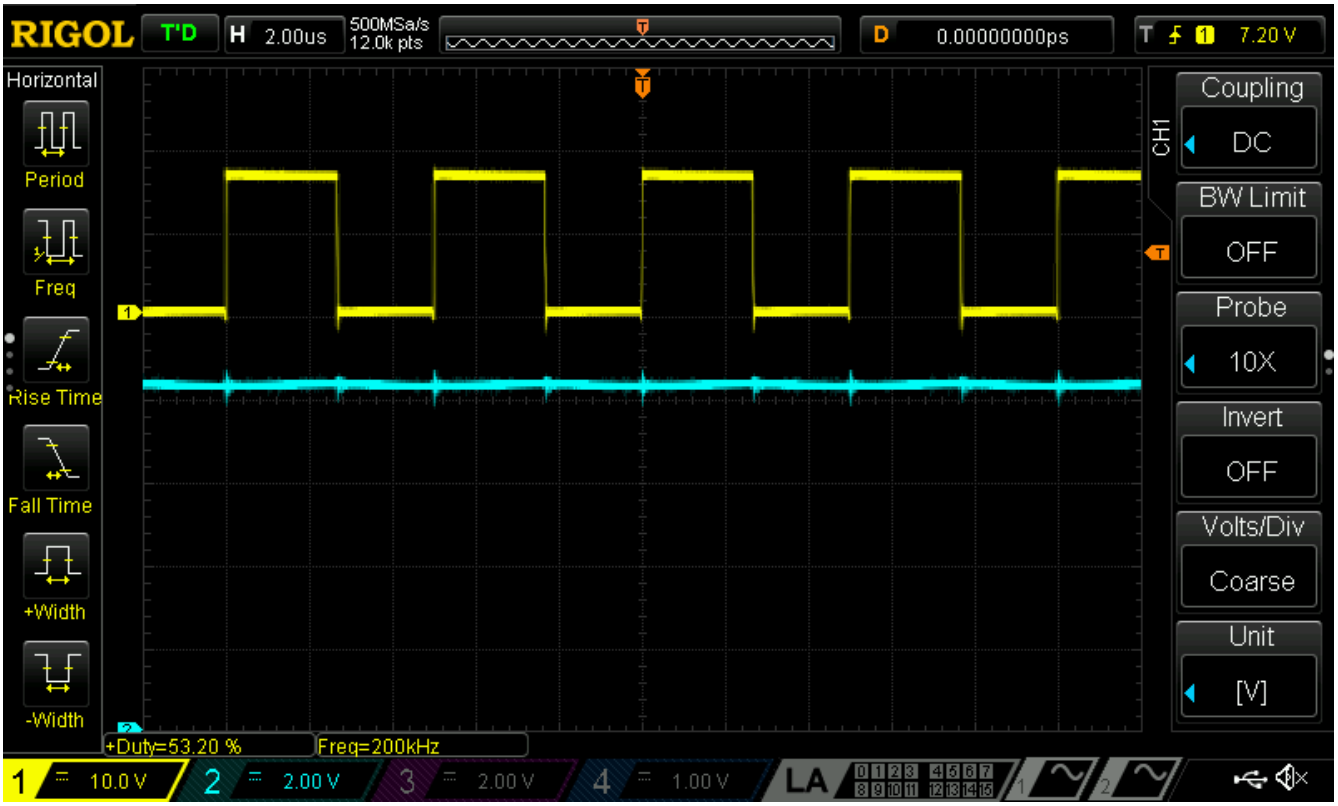

Figure 7. Duty Cycle at MPP @ R_{LOAD} = 40 Ω (yellow), V_{LOAD} (blue)

R_{LOAD} = 50 Ω

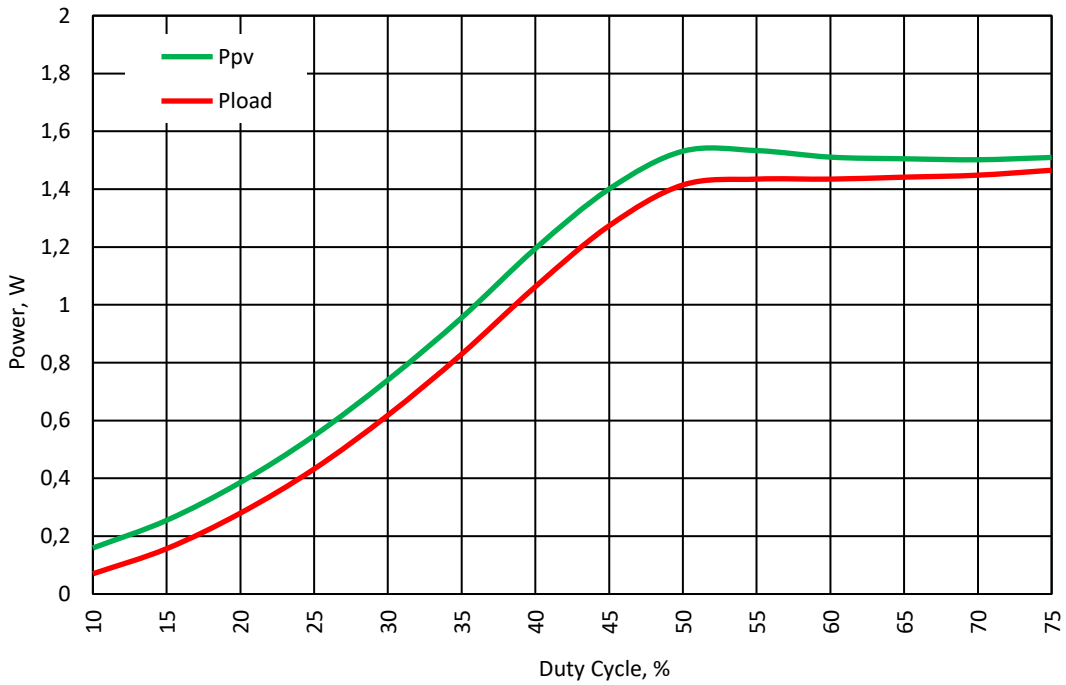

Figure 8. Power vs. Duty Cycle @ R_{LOAD} = 50 Ω

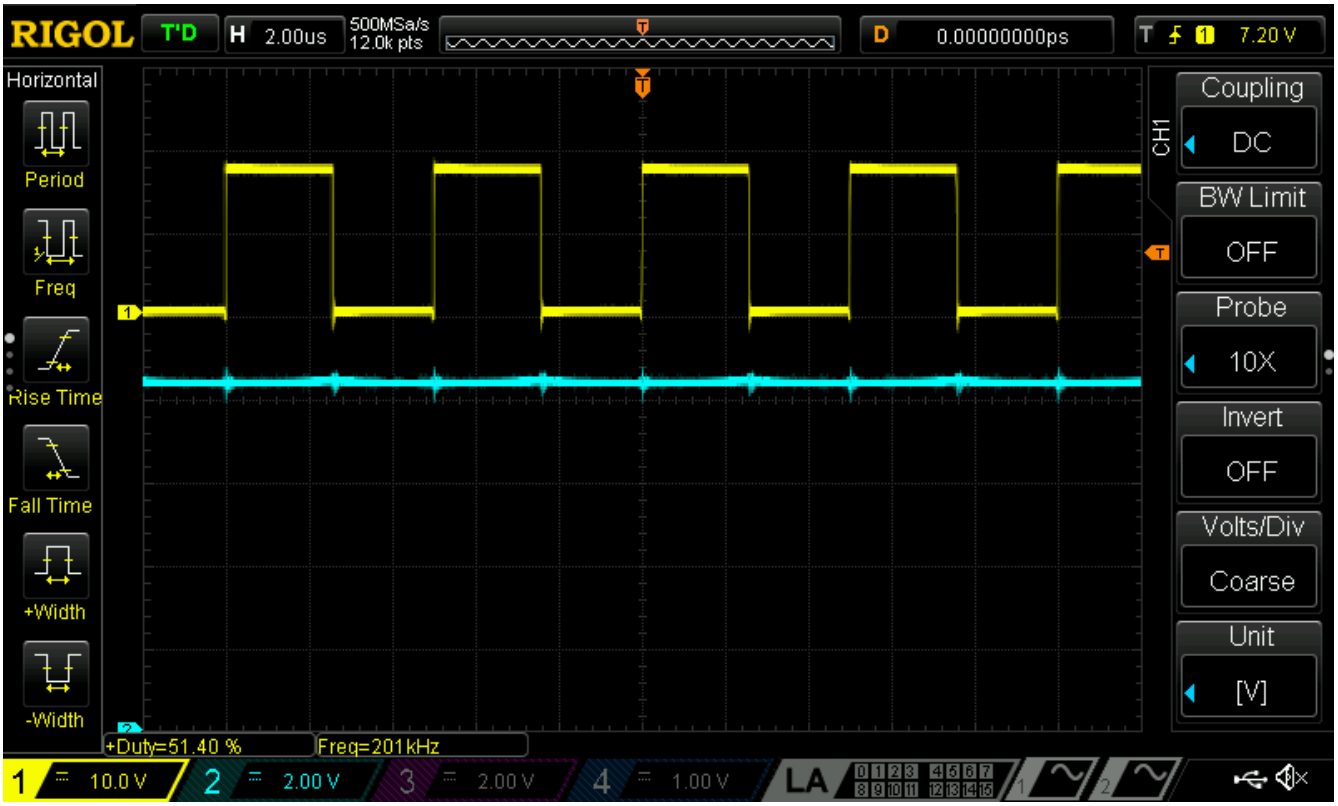

Figure 9. Duty Cycle at MPP @ R_{LOAD} = 50 Ω (yellow), V_{LOAD} (blue)

As shown from the figures above, the design works well, so a photovoltaic (PV) system operates at or near the peak power point.

5. MPPT for Battery Charging

5.1 Operating Principle and GreenPAK Design

To charge the 3.7 V lithium-ion battery, some changes must be made to the Basic MPPT design shown above. The SLG47115 Half Bridge is in High Side mode and an external Schottky diode is added. Also, there is battery voltage feedback to SLG47011 PIN 9 and PIN 12 and battery current feedback to SLG47011 PIN 7. See a circuit diagram in Figure 10.

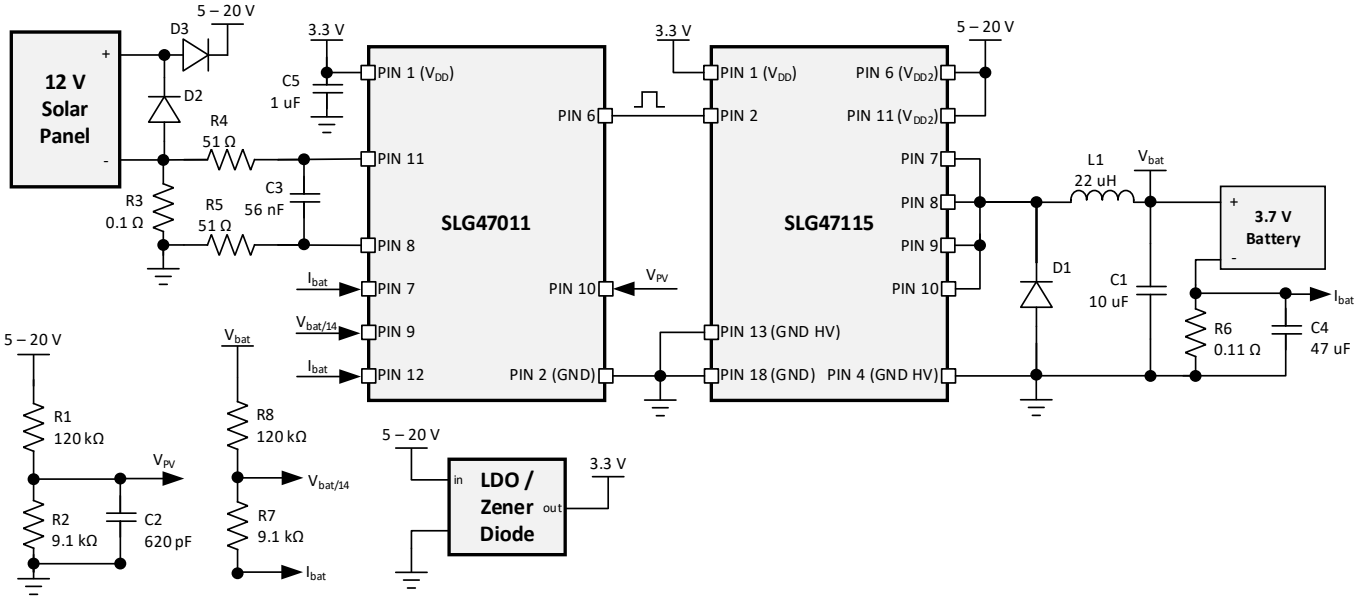

Figure 10. MPPT for Battery Charging Controller Circuit Diagram

The GreenPAK design and the main algorithm stay the same with some additional features. See Figure 11.

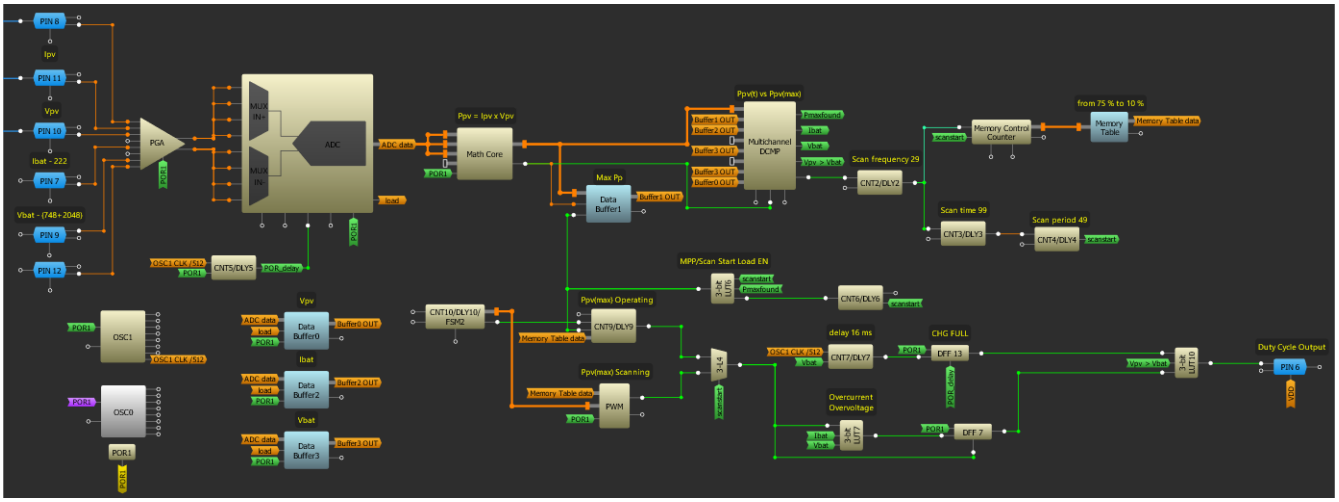

Figure 11. MPPT for Battery Charging GreenPAK Design (SLG47011)

The battery current feedback comes through PIN 7 to the single-ended input with a 4x Gain of the PGA Channel 2. The maximum allowable value for 200 mA is 222. This value is averaged in Data Buffer2. Then the average value is compared in DCMP CH1 with Static threshold #0 of 222. The output of DCMP CH1 goes to 3-bit LUT7.

The battery voltage feedback from the resistive divider comes through PIN 9 to the single-ended input of the PGA Channel 3. The maximum allowable value for 4.2 V is 748. This value is averaged in Data Buffer3. Then the

average value is compared in DCMP CH2 with Static threshold #1 of 748. The output of DCMP CH2 goes to 3-bit LUT7.

The CH3 of DCMP compares if the solar panel voltage is greater than the battery voltage to be able to carry out the charging process with a buck converter. If the solar panel voltage is lower than the battery voltage, the charging terminates through 3-bit LUT10.

The signal from Multiplexer 3-bit LUT4 goes to DFF 7 nRESET and 3-bit LUT7. The 3-bit LUT7 output is connected to DFF 7 CLK. Thus, the DFF 7 output will be the same as the 3-bit LUT4 output if the DCMP CH1&CH2 output is LOW, meaning that no overcurrent and/or overvoltage state occurs. If one of DCMP CH1&CH2 output is HIGH – the duty cycle will be chopped. This final signal goes to 3-bit LUT10.

CNT/DLY7 is configured as a Delay and monitors the battery voltage value. If it is 222 for a specified time that means that the battery is charged, the HIGH signal is sent to DFF 13 which turns off the charging through 3-bit LUT10.
3-bit LUT10 is connected to PIN 6, and this is the final Duty Cycle Output signal for the Buck Driver. PIN 6 is connected to PIN 2 of the SLG47115.

5.2 Design Testing

The test bench consists of a 12 V solar panel, three automotive halogen 60 W lamps, a GreenPAK Universal Dev. Board with an SLG47011, a GreenPAK Universal Dev. Board with an SLG47115, and a breadboard with soldered filters and resistors. There is also a holder and a 3.7 V ICR 14500 battery with a capacity of 800 mAh. The connected multimeter shows the battery voltage. The charging current is limited to 0.25 C – 200 mA.

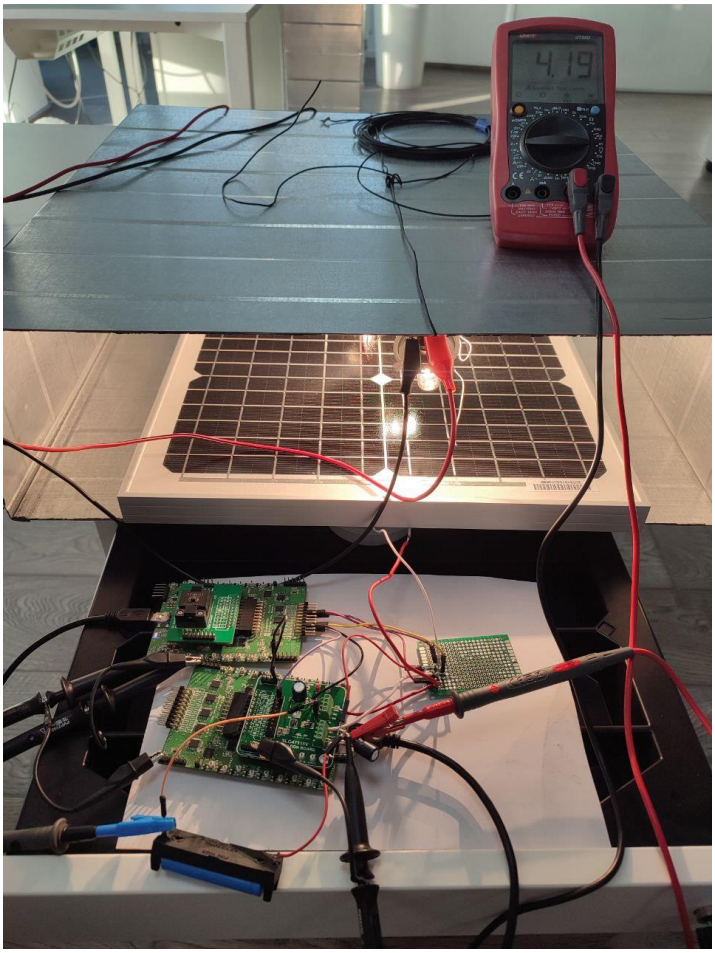

Figure 12. Testing Prototype

The following Figure 13 - Figure 16 shows the charging process of the 800 mAh Li-ion battery. For each subsequent figure, the power of the lamps acting on the solar panel was increased. As can be seen from the figures below, the duty cycle decreases. The battery voltage level can also impact on solar panel's maximum power point and duty cycle of the switching signal in accordance.

Figure 17 shows the charging termination.

Channel 1 (yellow / 1st line) – SLG47011 PIN 6 (Duty Cycle Output).

Channel 2 (light blue / 2nd line) - V_{bat}.

Channel 3 (magenta / 3rd line) - DCMP CH2 Output (voltage monitor).

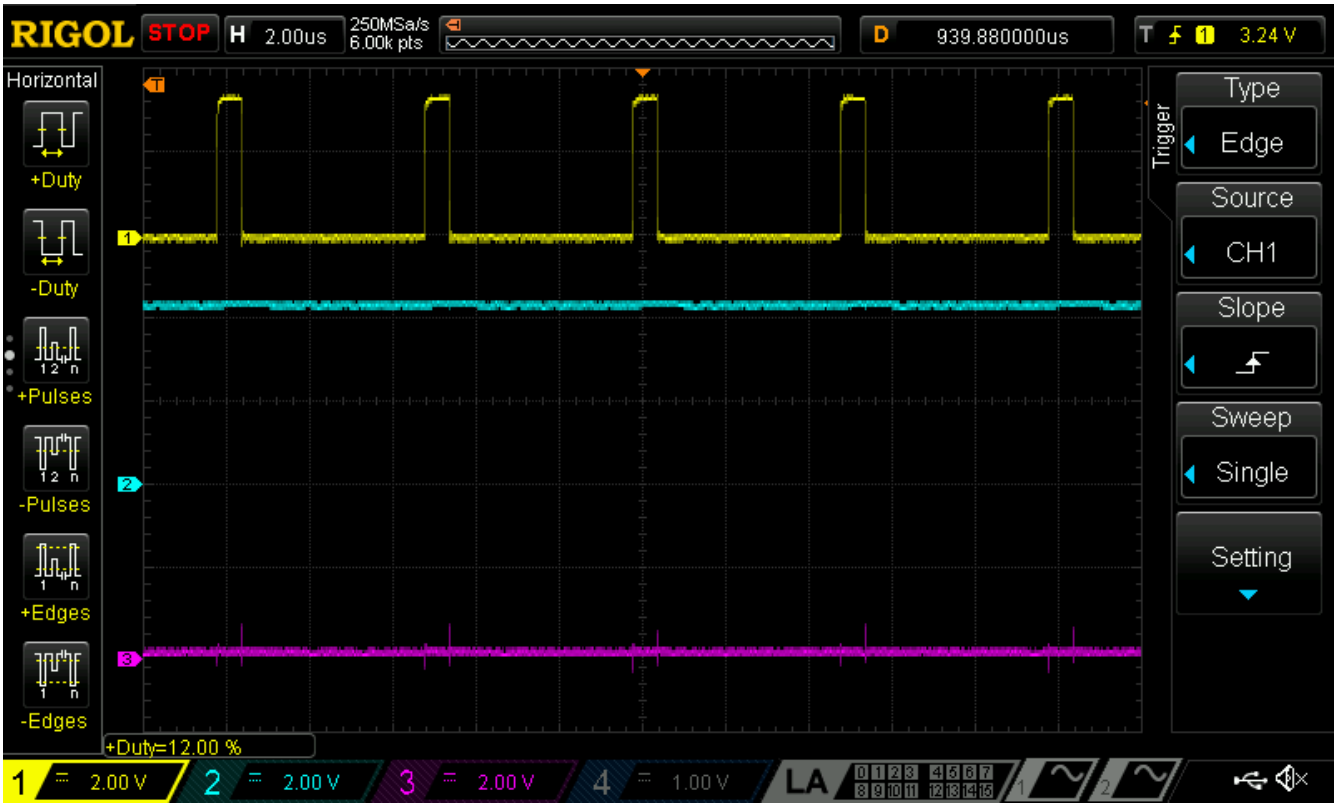

Figure 13. Duty Cycle 12 %

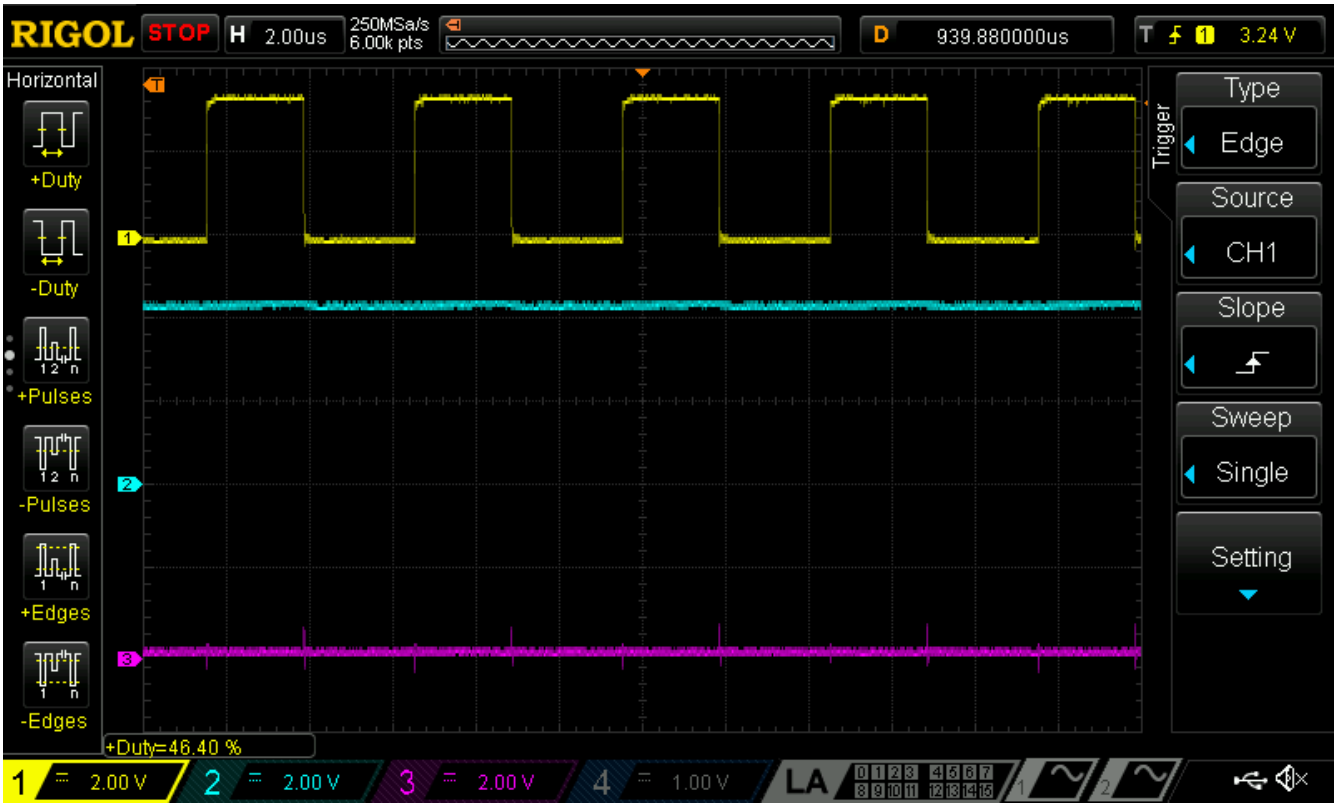

Figure 14. Duty Cycle 46 %

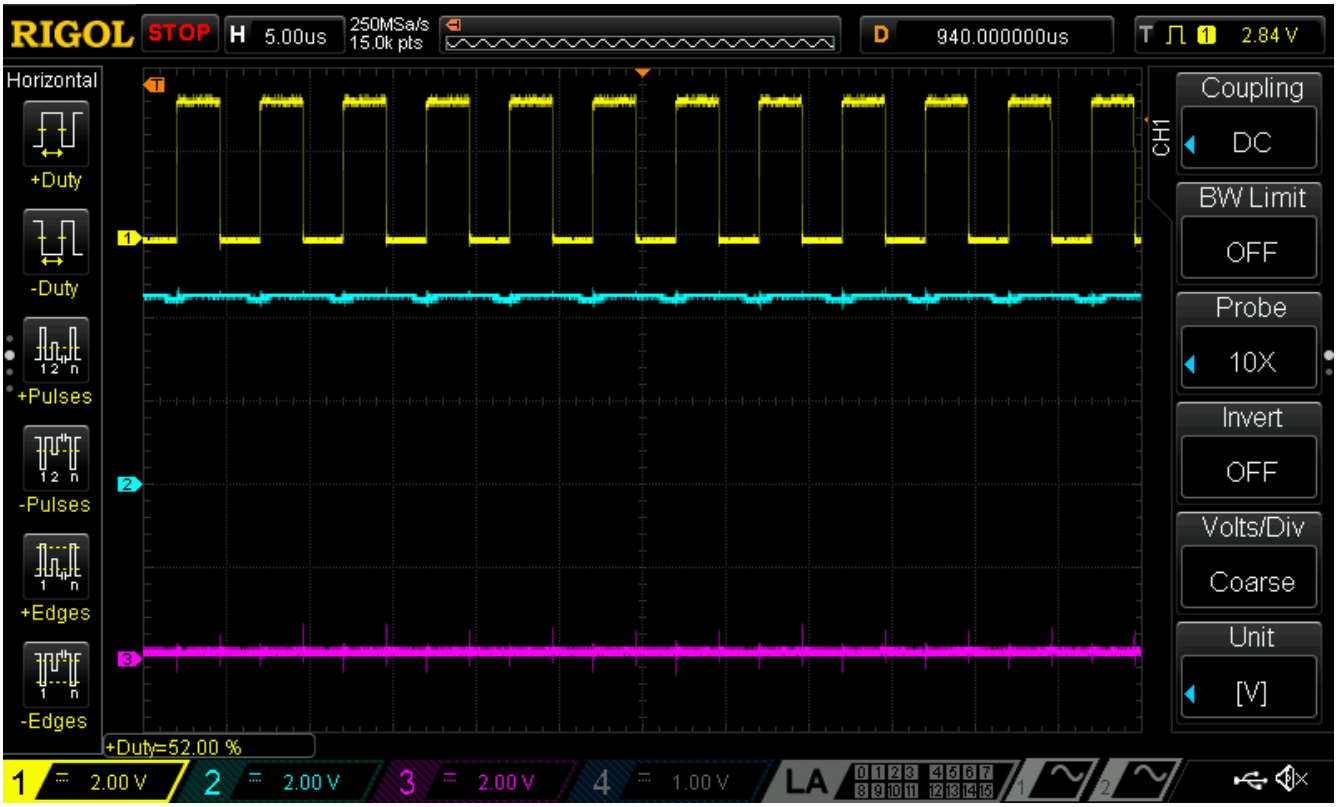

Figure 15. Duty cycle 52%

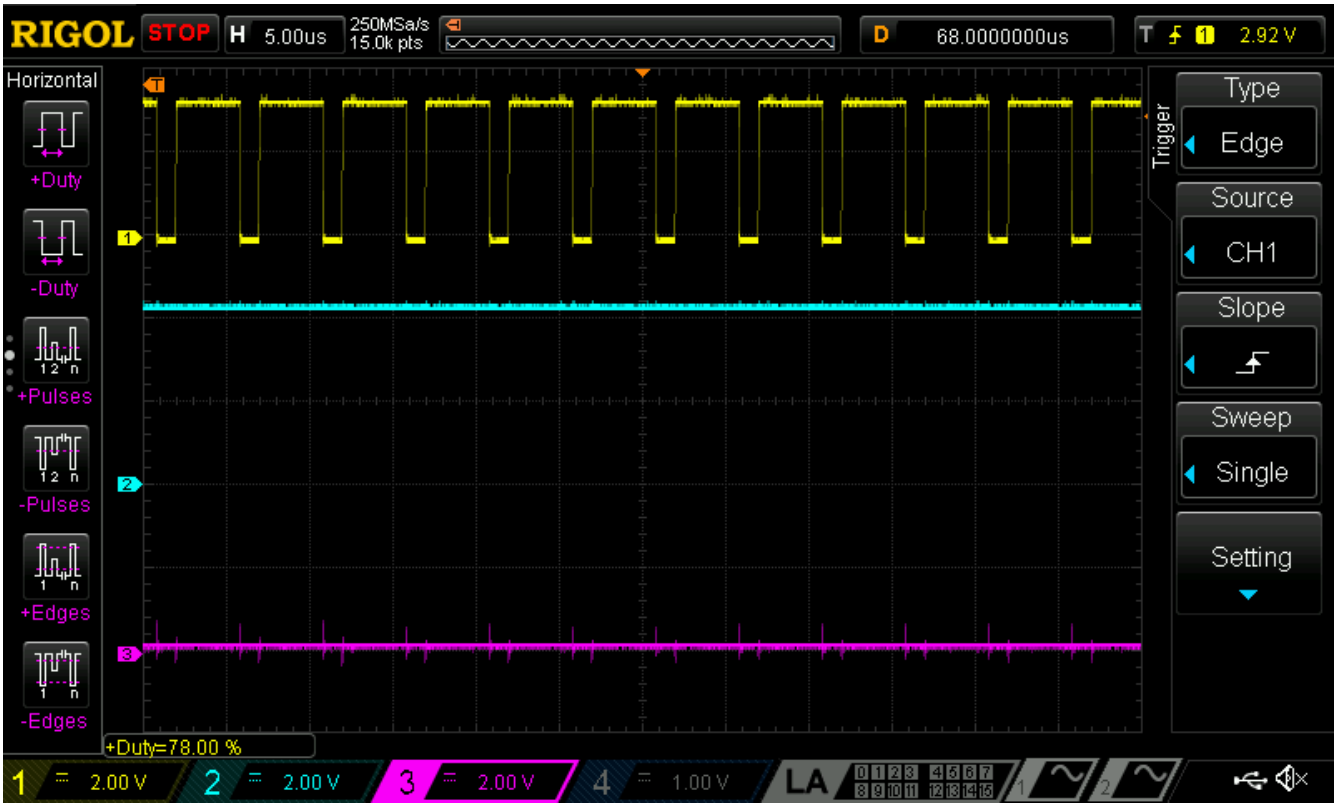

Figure 16. Duty cycle 78%

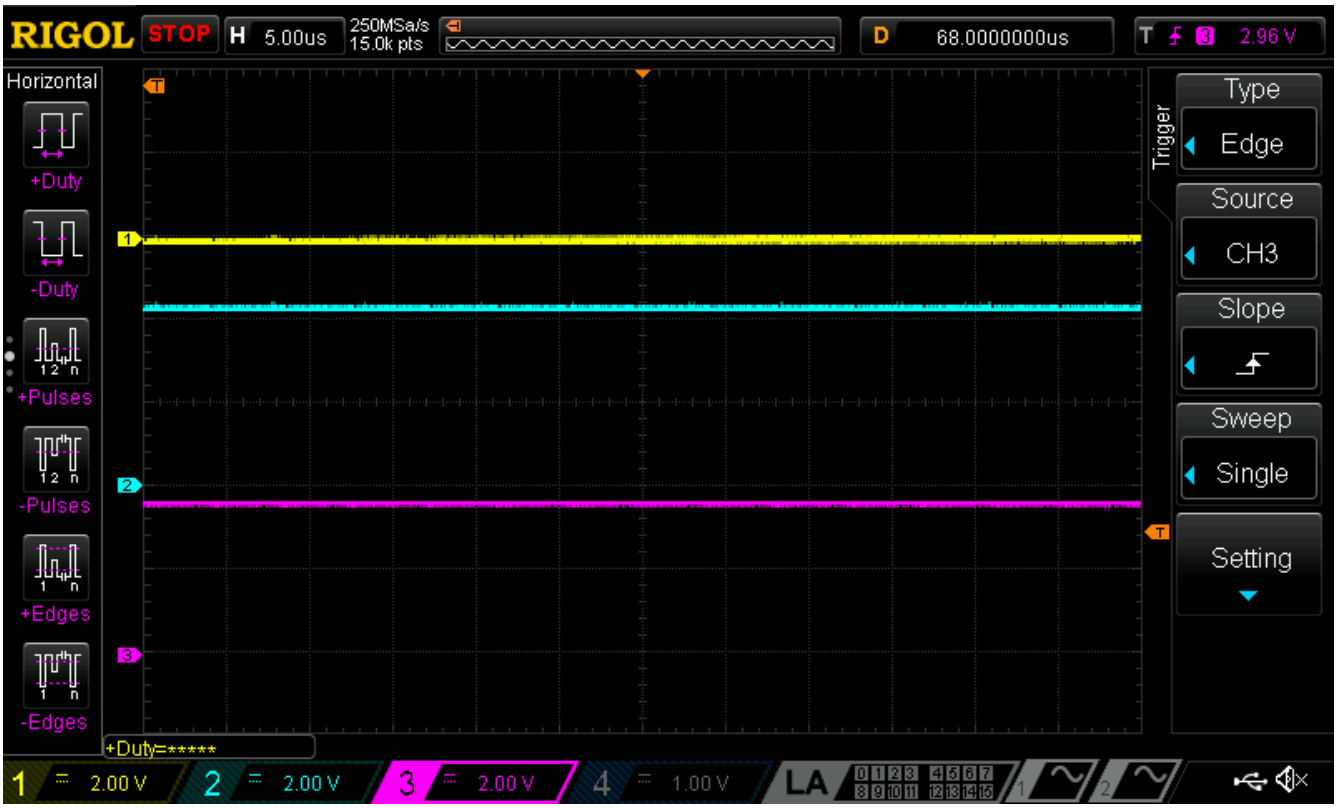

Figure 17. Charging Termination

6. Anti-Aliasing Filters

Low-pass filtering is essential to eliminate any frequency components (harmonics) within the analog signal that surpass the Nyquist frequency. When frequency components in the analog signal exceed the Nyquist frequency, an undesired phenomenon called aliasing occurs.

Resistor R2 and capacitor C2 form a filter with a cutoff frequency equal to $f_{(-3dB)} = \frac{1}{2\Pi \cdot R2 \cdot C3} \sim 28.2\ kHz$ and is intended to prevent aliasing when the solar panel voltage is measured.

Resistors R4, R5, and capacitor C3 form a filter for solar panel current measurement channel with a cutoff frequency equal to $f_{(-3dB)} = \frac{1}{2\Pi (R4+R5) \cdot C3} \sim 27.9\ kHz$.

Resistor R6 and capacitor C4 form a filter for battery current measurement channel with a cutoff frequency equal to $f_{(-3dB)} = \frac{1}{2\Pi \cdot R6 \cdot C4} \sim 30.8\ kHz$.

7. Conclusion

This application note describes how to configure the AnalogPAK SLG47011 to create a Maximum Power Point Tracker. It also shows how to charge a 3.7 V battery using this method.

The design allows to monitor the solar panel power thanks to PGA, ADC, MathCore, and Data Buffers. With DCMP, it is easy to find the maximum power. This value can then be reproduced using the PWM block. Four ADC channels also allow you to monitor battery voltage and current.

The flexibility of the internal resources allows adapting it to the needs of the customer without effort.

8. Revision History

Revision	Date	Description
1.00	Oct 28, 2024	Initial release