Pattern Generator for Addressable RGB LEDs
SLG47011

This application note describes the features of addressable RGB LEDs and how to utilize the SLG47011 as an extended pattern generator and as a control unit for the LEDs. This application note is also accompanied by design files, which can be found in the References section.

Contents

References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-388 Pattern Generator for Addressable RGB LEDs.aap, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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1. Introduction

Over the past few years, programmable LEDs such as the WS2812B have revolutionized the field of illumination and creating visual effects. These compact modules integrate individual red, green, and blue LEDs along with a control chip into a single small package. Control of each individual LED within a strip or a matrix allows for mesmerizing lighting displays, from subtle gradients to complex animations, enhancing the aesthetics of various applications such as architectural lighting, gaming setups, and stage performances.

One of the crucial elements in harnessing the full potential of the addressable RGB LEDs is the use of a pattern generator. It enables users to design, program, and display intricate lighting patterns and animations effortlessly. The Renesas SLG47011 is the perfect solution for controlling addressable LEDs, serving as a versatile pattern generator.

2. Control of Addressable LEDs

The WS2812B is an addressable RGB LED that combines an RGB LED and an integrated driver in one package, enabling users to independently control the color and brightness of each LED. It also includes signal reshaping and amplification circuits, allowing each LED to transmit a signal received from a preceding LED. The WS2812B is controlled using a digital serial protocol and requires only one data line.

Figure 1 illustrates the data transmission method.

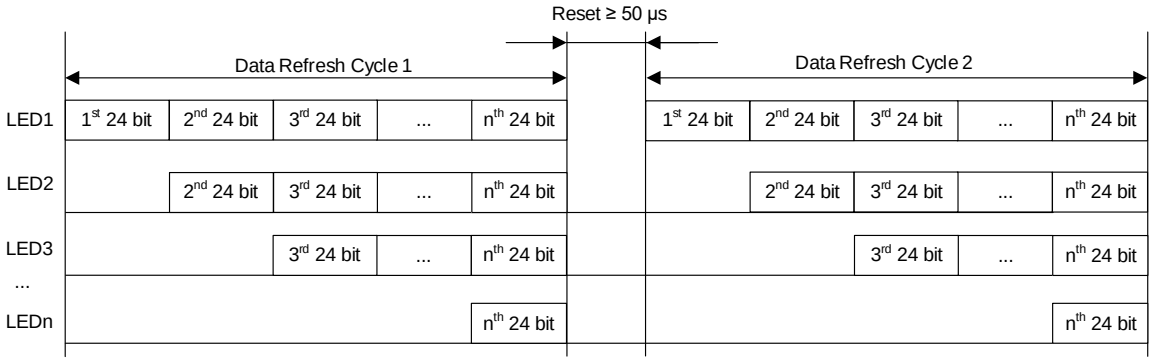

Figure 1. Timing Diagram of Data Transmission Method

3. GreenPAK Design

In this application note, an 8 x 8 LED matrix is used to implement the control of each of the addressable LEDs. Each LED requires 24 bits, resulting in 8 x 8 x 24 = 1536 bits per matrix. Figure 2 shows the general schematic using the SLG47011.

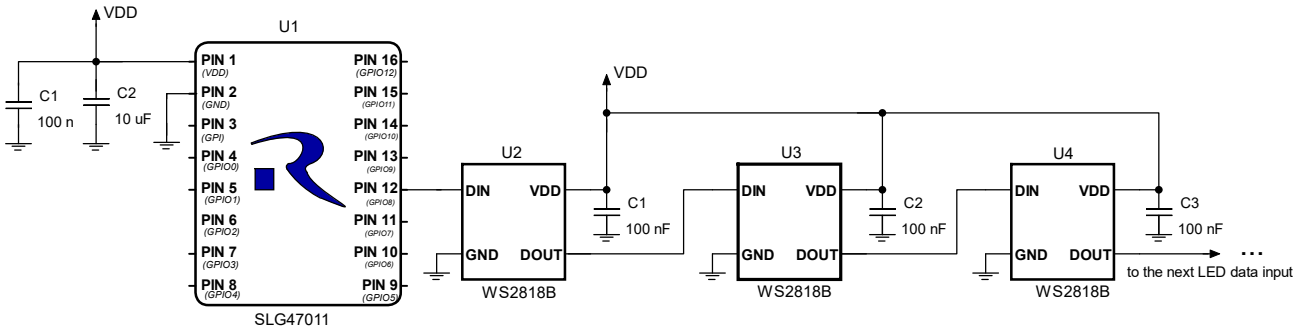

Figure 2. General Schematic of Addressable RGB LEDs Control

The schematic specifies that, after the pixel's power-on reset, the DIN port receives data from the SLG47011. The first pixel collects the initial 24-bits of data and then sends the remaining data to an internal data latch. This

data is then processed by the internal signal reshaping and amplification circuit and then sent to the next cascaded pixel through the DOUT port.

3.1 Static Pattern Generator

Figure 3 shows the internal design of the pattern generator in the GreenPAK Designer tool within the Go Configure Software Hub.

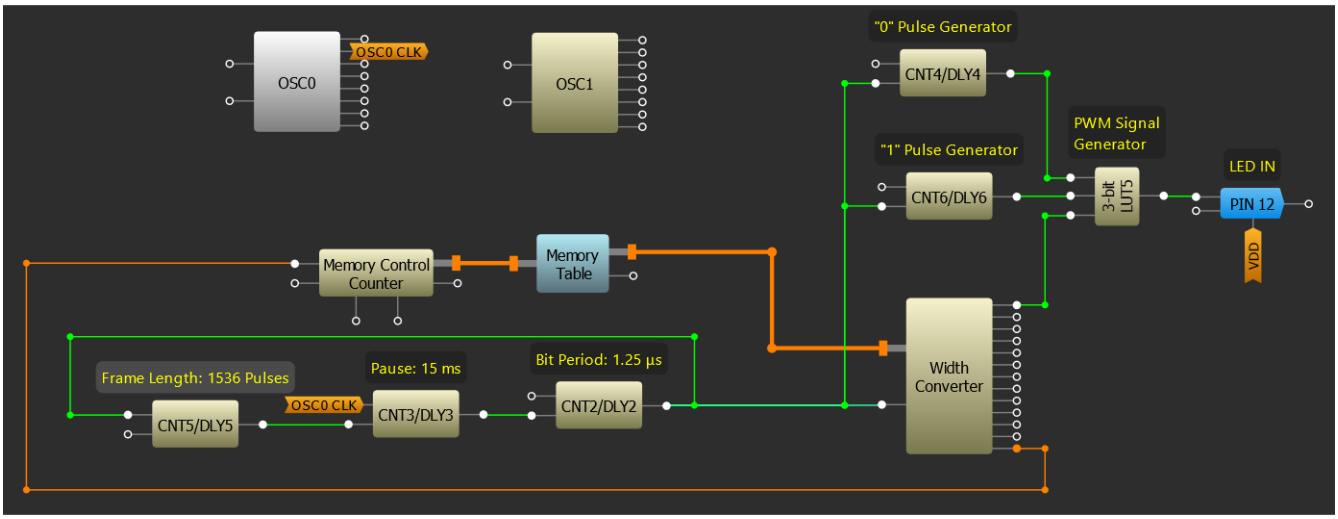

Figure 3. GreenPAK Designer Schematic of the Pattern Generator

Data intended for display on the LEDs is stored in the Memory Table. The Memory Control Counter is used to control the input address of the Memory Table. To store 1536 bits (in the case of a single matrix), 1536 / 12 = 128 rows of Memory Table are needed as it has a 12-bit bus output to the Width Converter. Each LED requires two words (24 bits) of data in the Memory Table. The 24-bit data segment contains information about the brightness of each of the three primary colors: red, green, and blue. Each primary color has 256 brightness steps (8 bits). Figure 4 illustrates the composition of the 24-bit data segment.

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

Figure 4. Composition of 24-Bit Data

The Memory Control Counter's initial counter data is set to “126”, which is one less than the upper limit. In this case, the data in the Memory Table is read sequentially, starting from the last word, which should be considered when creating a pattern. To enter a pattern into the Memory Table, a ready-made .csv file can be imported, or it can be entered manually in the Memory Table Data Editor. It is also possible to export the contents of the memory table in CSV format. Each pixel of the pattern is divided into its individual RGB components and entered into the Memory Table: first an 8-bit binary code for the blue color component, then red, and then finally green.

Because the Memory Table has a 12-bit parallel output, the Width Converter is used in “12-to-1” mode. When the Width Converter is enabled, the clock input for the Memory Control Counter is sourced from the Width Converter. The Memory Table data is serialized via the Width Converter and then converted into a PWM signal which is then output to Pin 12. To program the WS2812B LED strip, the data must be converted into a pulse-width modulated (PWM) signal (see Figure 5). The timing intervals for this PWM signal are shown in Table 1. As shown in this table, the time intervals are not overly strict and allow for some margin.

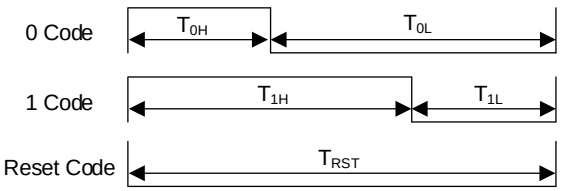

Figure 5. PWM Control Signal

Table 1. Timing Intervals of 0 and 1 Coded Signals

Symbol	Parameter	Typical Value	Margin
T_{0H}	0 code, High Voltage Time	0.4 µs	±150 ns
T_{1H}	1 code, High Voltage Time	0.8 µs	±150 ns
T_{0L}	0 code, Low Voltage Time	0.85 µs	±150 ns
T_{1L}	1 code, Low Voltage Time	0.45 µs	±150 ns
RST	Low Voltage Time	Above 50 µs	--

The WS2812B LED is available in various varieties made by different manufacturers, each with its own data timings. To determine the duration of the pulses for both logic HIGH and logic LOW signals, the recommended method is to configure the SLG47011 IC in emulation mode with standard timing settings. Next, connect the LED chain and measure the timings by observing the next LED using an oscilloscope. In this example, after the measurement, pulse durations of 0.32 µs and 0.7 µs were obtained for the LOW and HIGH signals respectively.

CNT/DLY4 and CNT/DLY6 operate as One Shots, generating a 0.32 µs pulse for logic 0 and a 0.7 µs pulse for logic 1, as determined by the previous measurements. Furthermore, the 3-bit LUT5 component generates an output PWM signal based on these pulses (see Figure 6). The period of the generated PWM signal is equal to $T_{0H} + T_{0L} = T_{1H} + T_{1L} = 1.25$ µs.

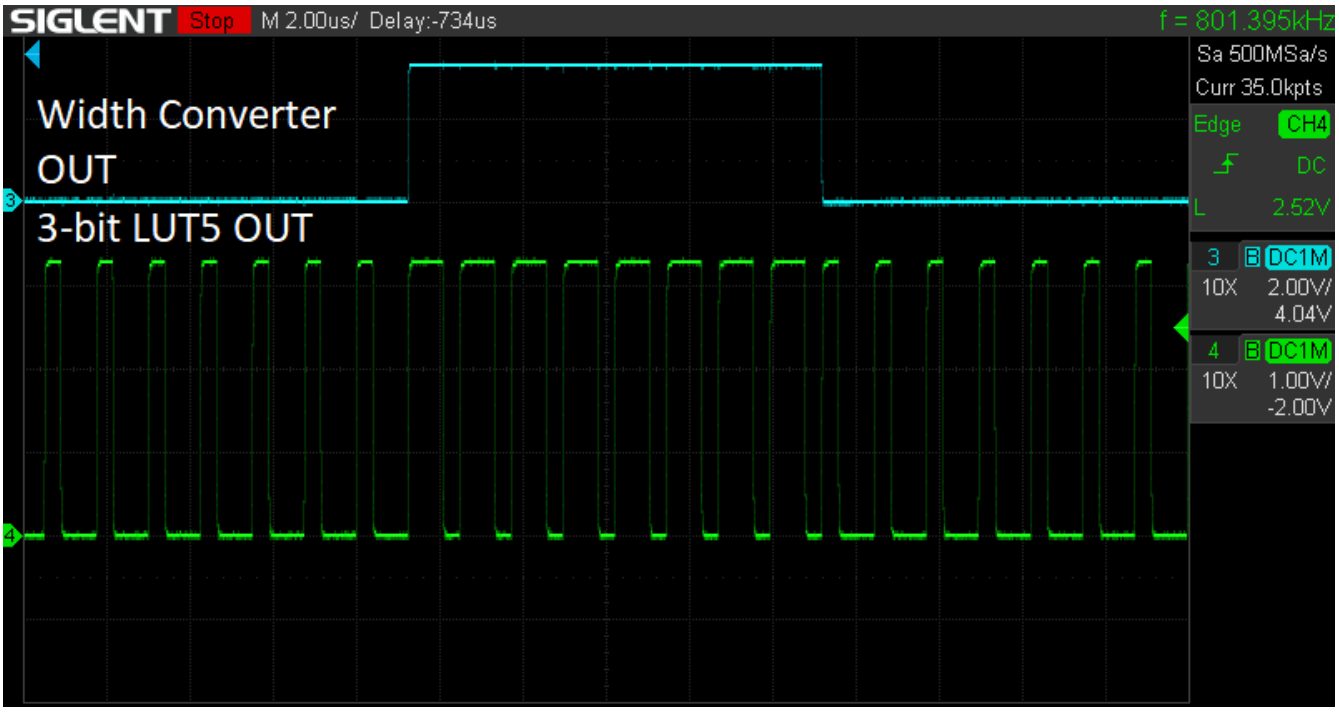

Figure 6. Generated PWM Signal

The CNT2 counter is designed to generate the Width Converter clock signal as well as the period for one bit of the PWM signal. After power-up, the RST input of the CNT2 counter is LOW, and the counter starts counting pulses on the CLK input. When the counter value reaches “49”, a pulse appears at its output, which is then sent to the CLK input of the CNT5 counter. The CNT5 counter is designed to form one frame, which is a sequence of bits before a pause. Upon receiving the first pulse at its input, the CNT5 counter outputs a LOW-level signal and increases its current count value by one, while the CNT2 counter continues to count without stopping. This process repeats until the 1536th pulse is received at the CLK input of the CNT5 counter. After this pulse, a HIGH-level signal appears at the output of the CNT5 counter. On the rising edge of this HIGH-level signal, the One Shot (CNT3/DLY3) generates a 15 ms pulse, which serves as the pause signal. This pulse enters the RST

input of the CNT2 counter and stops it. The CNT2 counter resumes its operation after 15 ms, and the entire cycle repeats. The pause reset signal is a delay between two frames and is necessary to latch the data previously sent to the LEDs and to set the LED's refresh rate to avoid flickering. The 15 ms delay time from CNT/DLY3 results in 66 frames per second.

Consider the counter's data value for the 8 x 8 LED matrix. The upper limit of the Memory Control Counter is calculated as follows:

$$\text{Upper Limit} = \frac{\text{number of LEDs} \times \text{LED data width}}{\text{word width}} - 1 = \frac{8 \times 8 \times 24}{12} - 1 = 127$$

The frame length counter data from CNT5 is calculated as follows:

$$\text{CNT5 Data} = (\text{number of LEDs} \times \text{LED data width}) - 1 = (8 \times 8 \times 24) - 1 = 1535$$

The results of the hardware testing are shown in Figure 7.

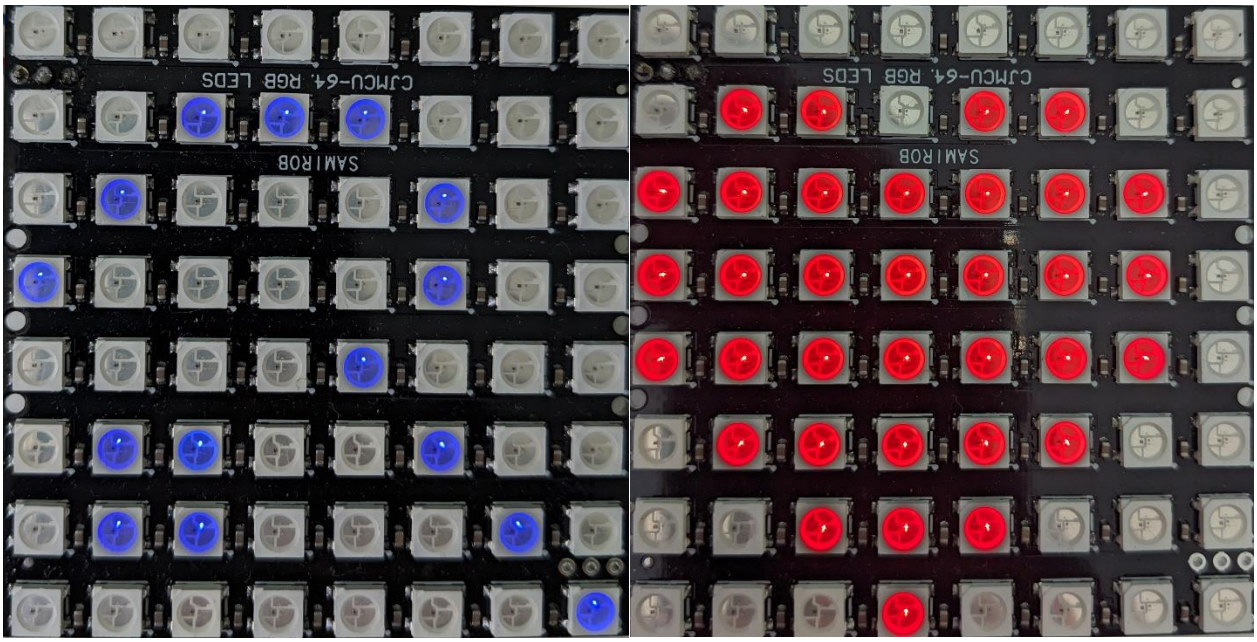

Figure 7. Images Generated by the Pattern Generator

In this application note, an 8 x 8 LED matrix is used for demonstration purposes. However, since the Memory Table consists of 4096 12-bit words, a much larger LED matrix or LED strip can be utilized. Because one LED requires 24 bits or two words, this allows for up to 4096/2 = 2048 LEDs to be controlled by the SLG47011.

3.2 Running Colors Generator

In addition to a static image, a running colors effect can also be implemented. Figure 8 shows a modified design to achieve this effect.

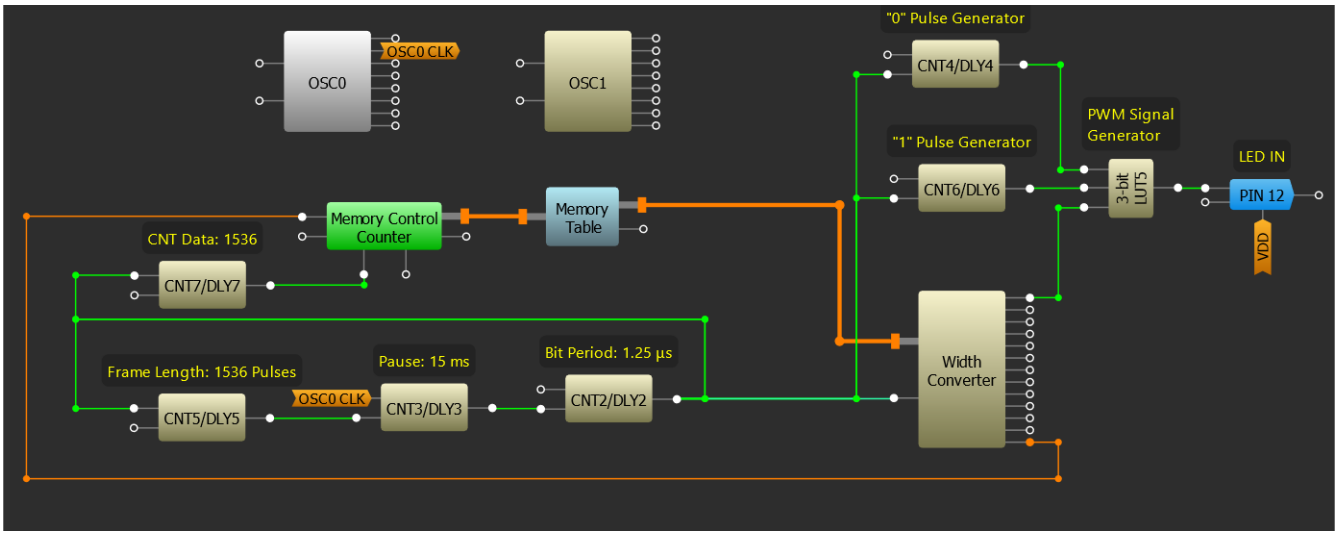

Figure 8. GreenPAK Designer Schematic for a Running Colors Effect

In this design, the CNT7 counter was added. The counter value must be a multiple of 24 bits and at the same time also have a value greater than “96” to avoid flickering. By increasing the value of the CNT7 counter, the speed of the running colors can be reduced. For clarity, the CNT7 counter value of “1536” is selected. The Memory Control Counter is set to decrement mode because its Up/Down input is logic LOW when it is turned on. When pulses are received at the Memory Control Counter CLK input, its value is incremented instead of decremented every 1536-th pulses, as the CNT7 counter outputs a short pulse to its Up/Down input. Because the counter data value of the CNT7 counter is one more than the value of the CNT5 counter, the Memory Control Counter provides the address of the previous 12 bits instead of giving the address of the next 12 bits of the Memory Table, causing a 24-bit shift with each subsequent frame. The results of the hardware testing are shown in Figure 9.

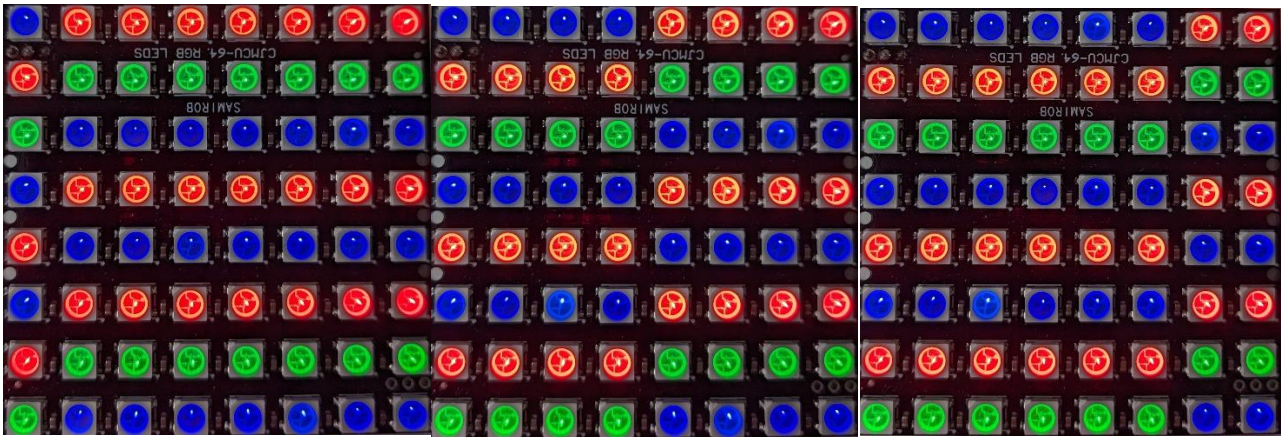

Figure 9. Running Colors Effect. Sequential Photos

4. Project Simulation

The GreenPAK Designer has a built-in simulation tool that allows users to evaluate the functionality of the design even in the absence of the development board. Figure 10 shows the simulation waveforms.

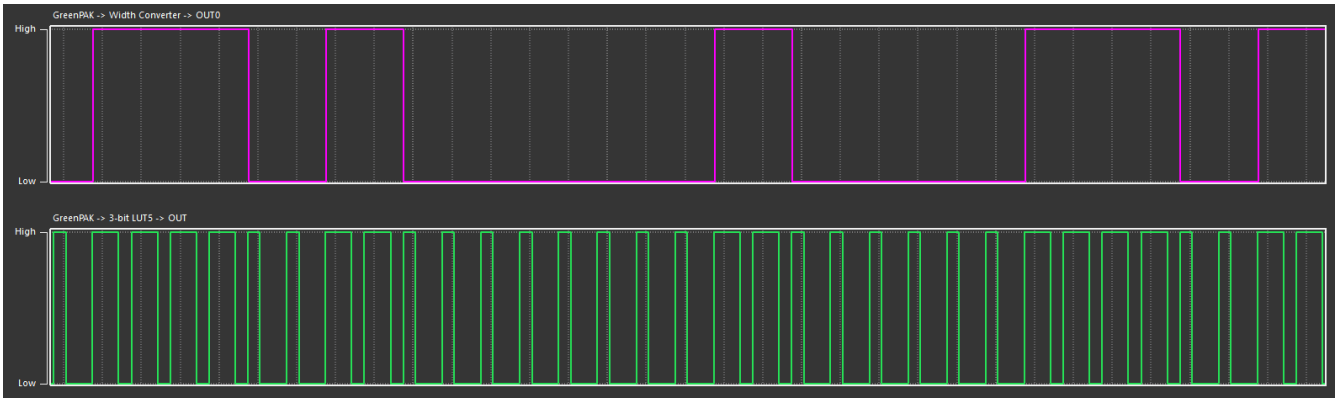

Figure 10. Software Simulation Waveforms

5. Conclusions

This application note demonstrates the use of the SLG47011 as an extended pattern generator and a control unit for RGB Addressable LEDs. Because a non-standard protocol is required to control these LEDs, it is necessary to emulate this protocol. Traditionally, such drivers are program-controlled, which requires the use of a high-speed system clock which increases power consumption. The SLG47011 performs this task with minimum power consumption. The availability of the Memory Table macrocell allows for the control of up to 2048 LEDs. Additionally, visual effects like running colors can be implemented. Furthermore, the SLG47011 features a compact package size of 2.0 mm x 2.0 mm.

6. Revision History

Revision	Date	Description
1.00	Sep 23, 2024	Initial release.

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