Capacitive Sensor
SLG47011

This application note describes the circuitry using the SLG47011 to create a capacitive sensor.

The application note comes complete with design files, which can be found in the References section.

Contents

References

For related documents and software, please visit: AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the AnalogPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure™ Software Hub | Renesas, Software Download and User Guide, Renesas Electronics

[2] AN-CM-387 Capacitor Sensor.aap, AnalogPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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1. Terms and Conditions

ADC	Analog-to-Digital Converter
DFF	D Flip-Flop
DI w/o ST	Digital input without Schmitt trigger
IC	Integrated circuit
MDCMP	Multichannel Digital Comparator

2. Introduction

There are a lot of ICs on the market that allow the implementation of only a single-channel capacitive sensor. The purpose of this documentation is to implement a two-channel capacitive sensor circuit based on the SLG47011V IC. This solution allows to reduce the number of components, leading to a reduction in the cost of devices using capacitive sensors.

3. How Does the Circuit Work?

This idea is implemented using the SLG47011 IC, and the implementation schematic is shown below.

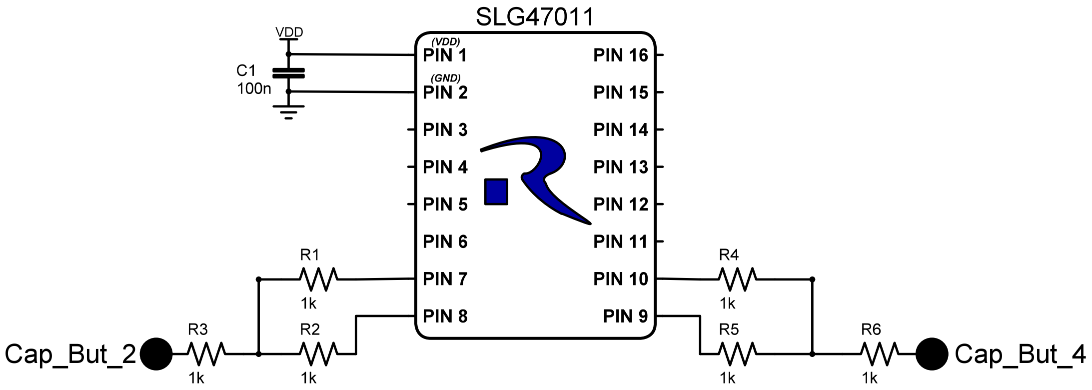

Figure 1. Application Circuit

The idea is that when a capacitor pin is touched, the capacitance is added to the circuit, which increases the charging and discharging time of the capacitor. With the help of an ADC embedded in the IC, the voltage across the capacitor during charging or discharging must be read simultaneously, and if the capacitance is decreasing at the same time, the voltage will be higher during discharging. These voltage values are used to determine whether the surface has been touched.

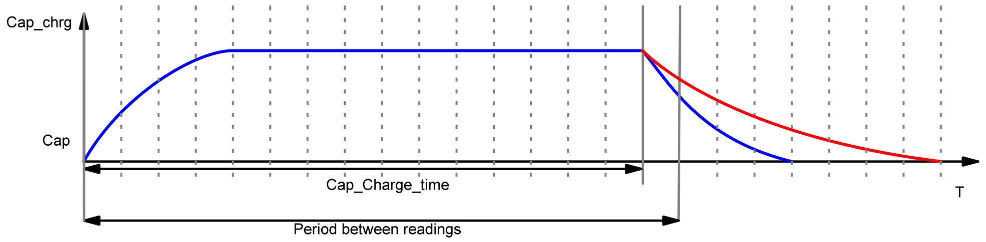

Figure 2. Graph of Capacitor Discharge before Touching (Blue) and during Touching (Red)

4. Capacitive Sensor AnalogPAK Design

This design is divided into five parts:

1. The capacitor charging unit – DLY3 and DLY6 are configured in One Shot mode (Figure 4 (a-b)) with their duty cycle tuned with respect to the ADC readout frequency (Figure 4 (c)) and the RC link charging time.

2. Capacitor voltage readout unit – the ADC reads the voltage values on the capacitors. The interval between readings depends on the oscillator frequency and the delay between ADC channels.

3. During the first cycle, the voltage values across the capacitor are sequentially recorded in Data Buffers 0-3. Subsequently, DFF 10 switches the Load signal for Data Buffers 1-3 to a LOW level, which prevents further data recording. From then on, data will only be written to Data Buffers 0-2 and compared with the static data in Data Buffers 1-3.

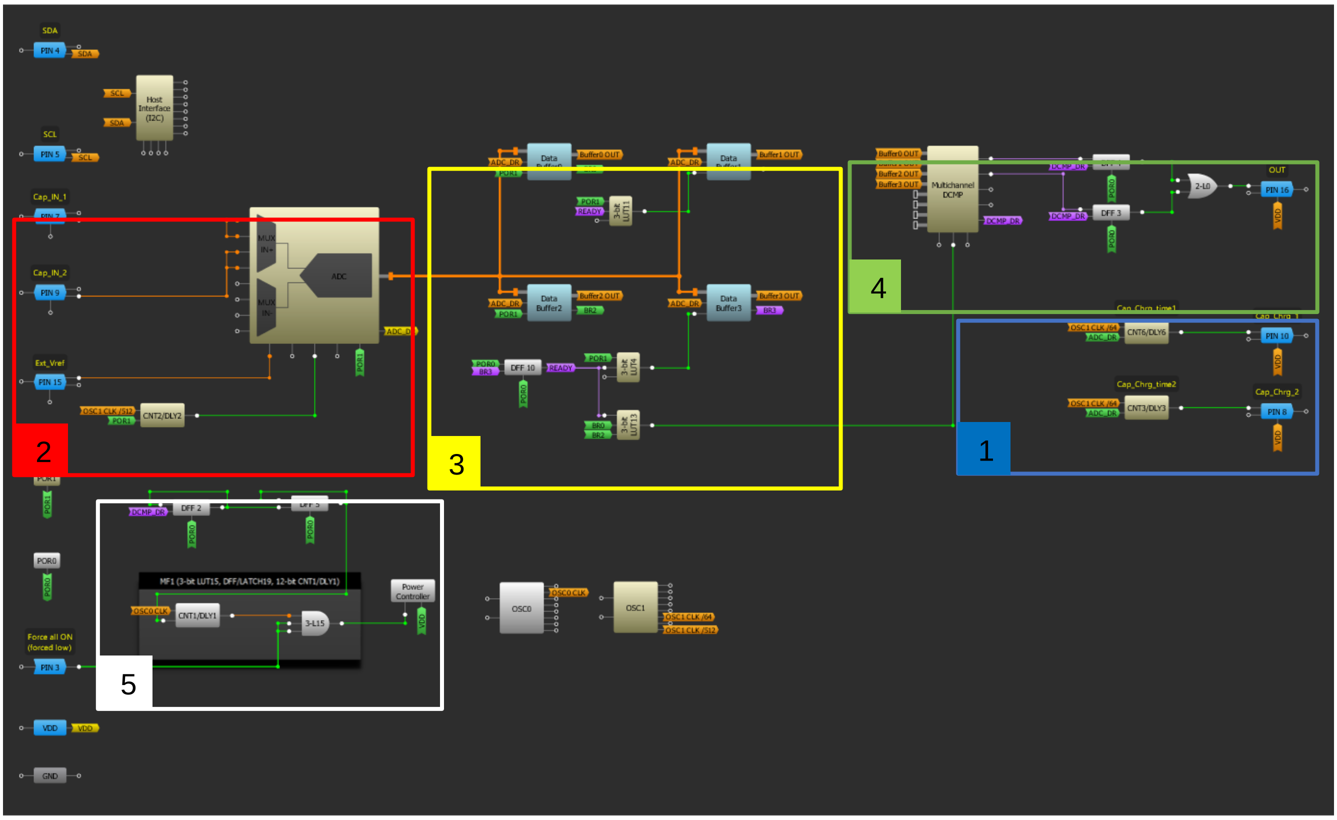

Figure 3. Capacitive Sensor Design Implementation

4. MDCMP compares the values of Data Buffer 0 with Data Buffer 1 and Data Buffer 2 with Data Buffer 3. The value from the MDCMP outputs is written to DFFs 4-3 and displayed on the pin for touch indication.

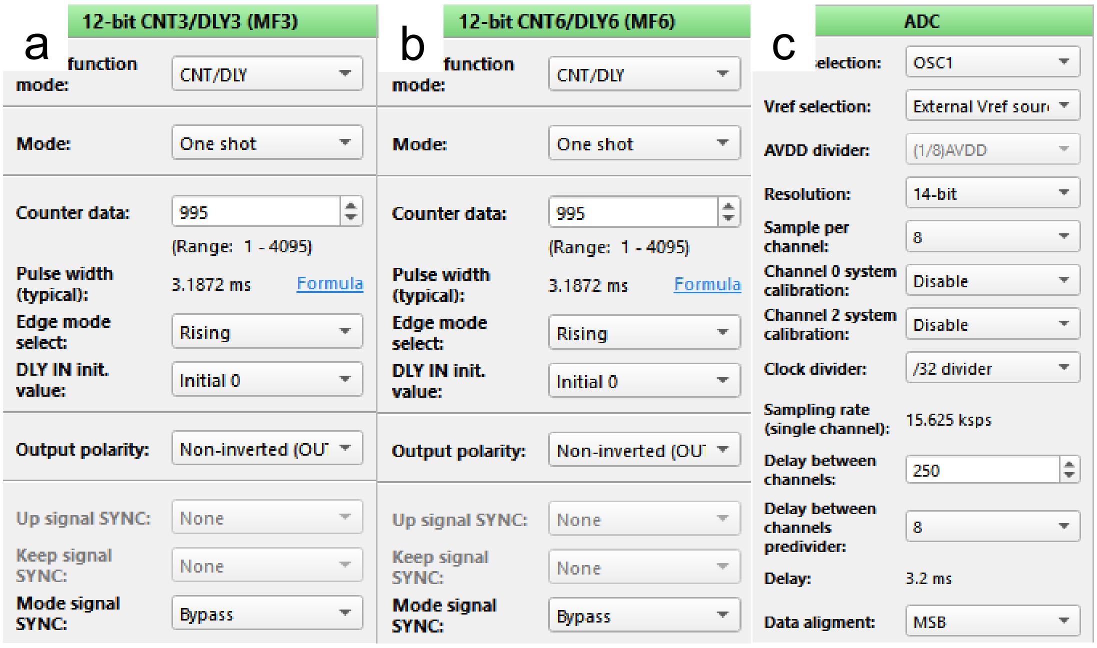

Figure 4. Configuration of Macrocells from Charging Unit

5. The Power Controller is used to turn off the sleep power domain in order to reduce current consumption.

5. Capacitive Sensor Demonstration Board

A demonstration board was created to exhibit the design's capabilities and functionality. The board includes a pre-built Capacitive Sensor circuit with four capacitive pads, two of which can be selected.

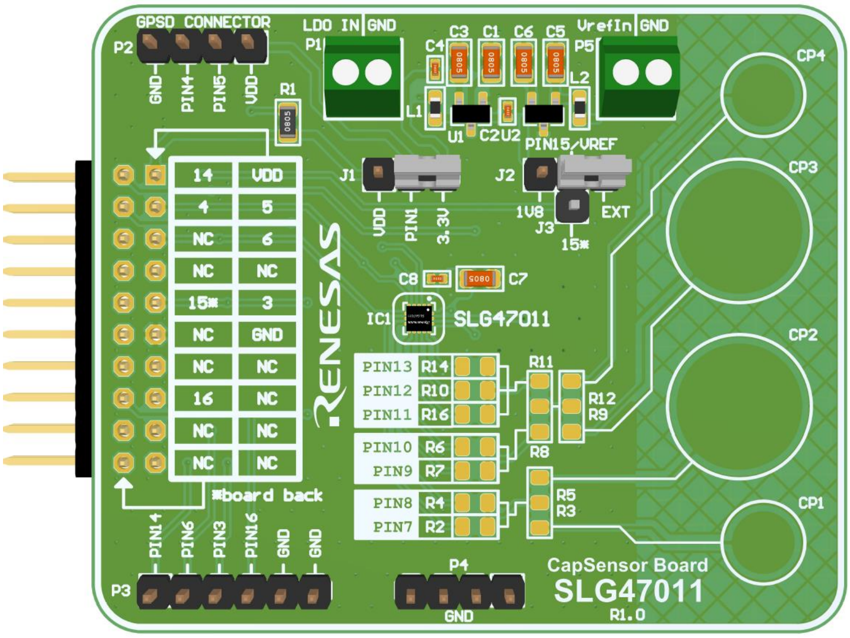

Figure 5. Capacitive Sensor Demonstration Board

6. Results

The design was tested with hardware, and the following results were obtained.

Table 1. Data Buffers Values during and after Touching (Blue Represents Cap1, Green Represents Cap2)

V_{DD}	Buffer 0 (touch)	Buffer 1 (no touch)	Buffer 2 (touch)	Buffer 3 (no touch)
3.3 V	~8526	~8277	~8904	~8301
2.3 V	~6248	~5842	~6424	~5868
1.7 V	~4189	~3547	~5502	~3596

Table 2. Current Consumption

Time retention (ms)	Symbol	Parameter	Condition/Note	Typ.	Unit
50	I_Q	Average Current	Static inputs and floating outputs. PIN3-5 are HIGH	~90	µA
100				~62	
250				~36	

The stability of the output was also tested at different values of the mode retention time, and the following waveforms were obtained:

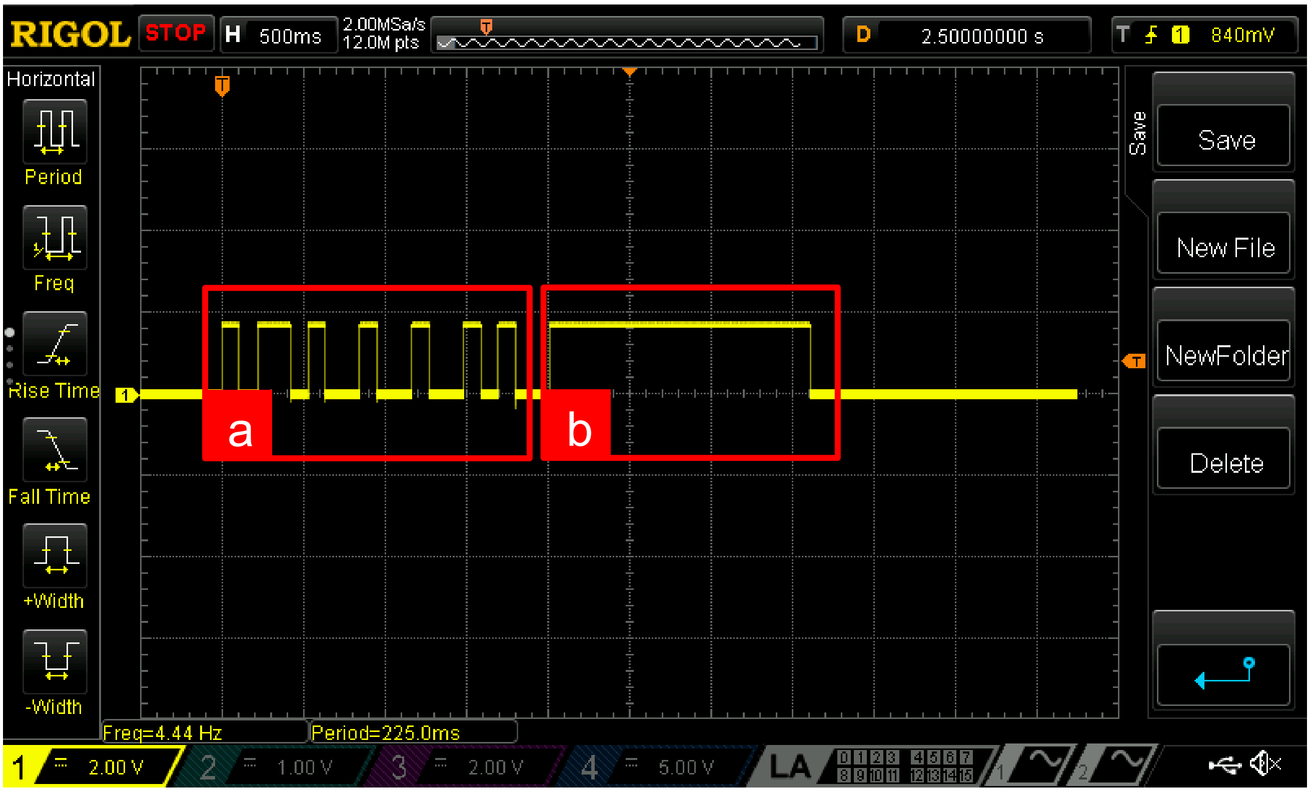

Figure 6.Output Stability Waveform CapacitiveSensor 1 (50 ms Rate)

a – Short Touch; b – Long Touch

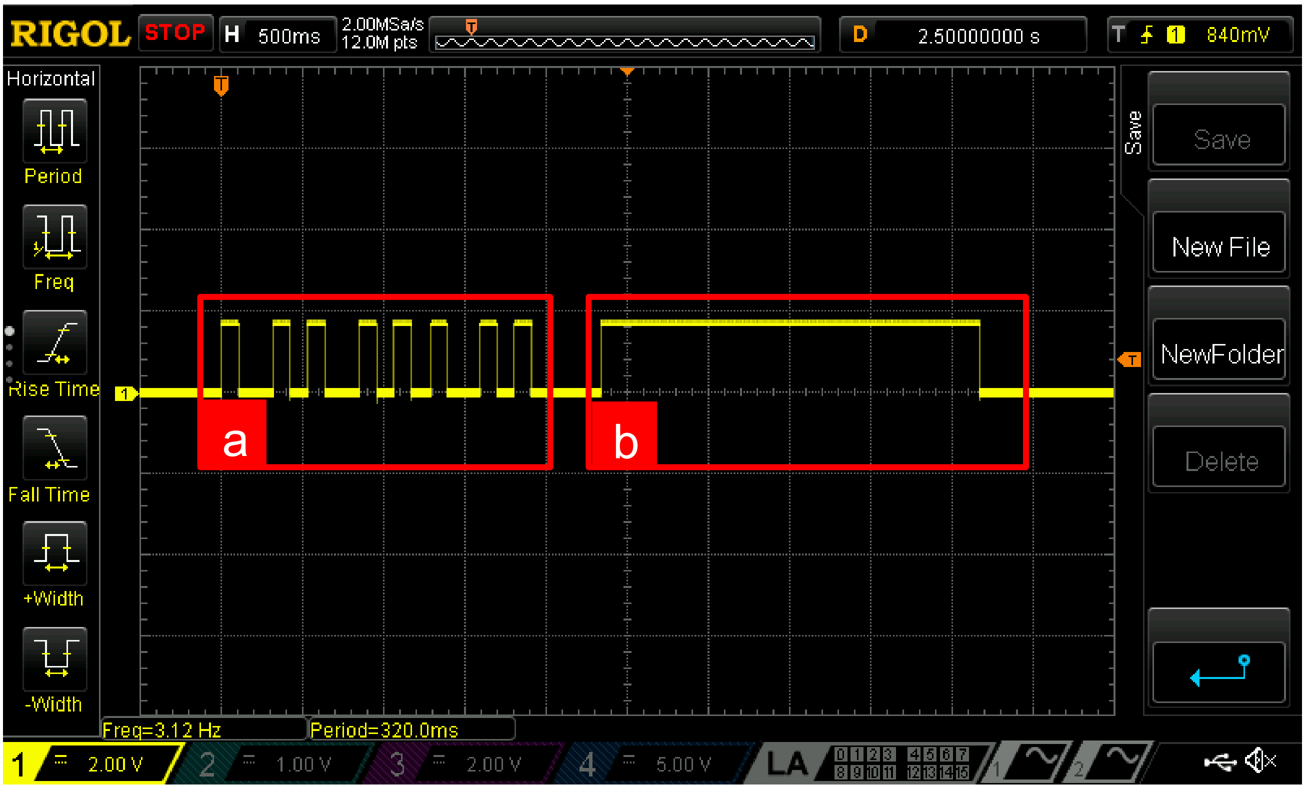

Figure 7. Output Stability Waveform Capacitive Sensor 2 (50 ms Sleep)

a – Short Touch; b – Long Touch

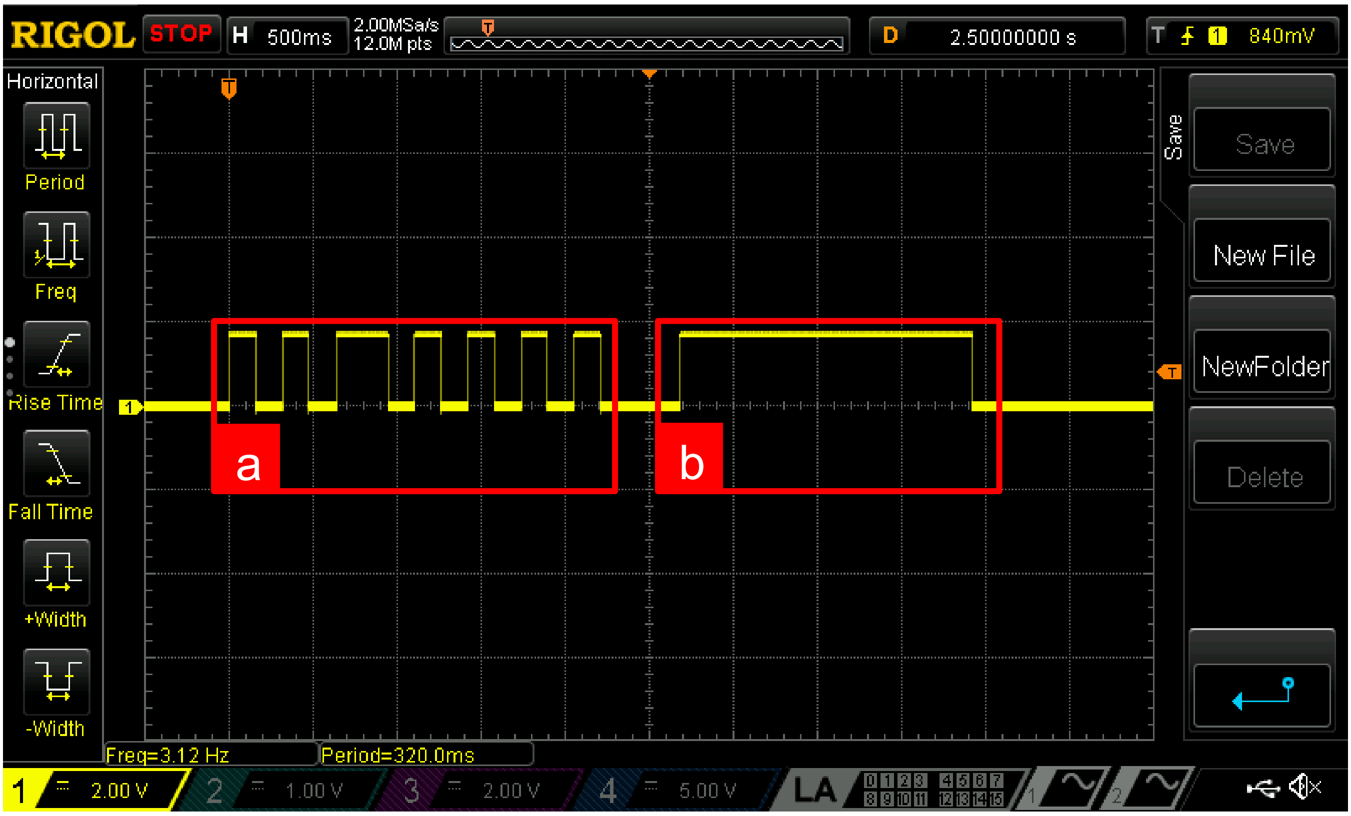

Figure 8. Output Stability Waveform Capacitive Sensor 1 (100 ms Sleep)

a – Short Touch; b – Long Touch

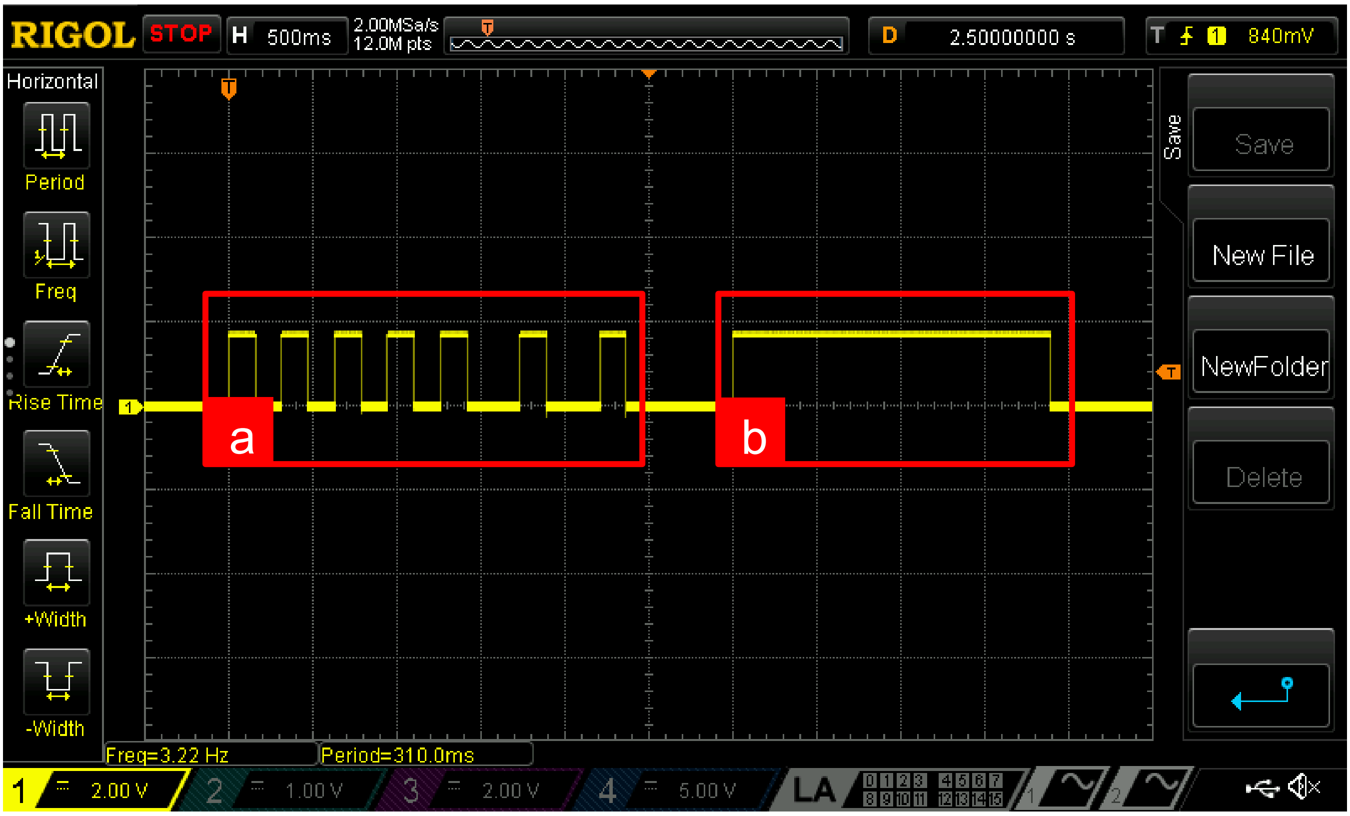

Figure 9. Output Stability Waveform Capacitive Sensor 2 (100 ms Sleep)

a – Short Touch; b – Long Touch

7. Conclusion

After reviewing Results, can be concluded that the design has been successfully implemented on the SLG47011V and operates stably (Figure 6, Figure 7, Figure 8, Figure 9). However, the stability of the output is affected by the value of V_{DD}, the smaller the V_{DD}, the greater the difference between the pressed and unpressed states, and therefore the greater the stability (the difference between the pressed and unpressed states is shown in Table 1). The results also show (Table 2) that depending on the value of the mode retention time, the current consumption changes, so it is recommended not to use a mode retention time of more than 50 ms to maintain good response and low current consumption.

8. Revision History

Revision	Date	Description
1.00	Sep 23, 2024	Initial release.

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