

Low Voltage Bidirectional Level Shifter

SLG47525/28

Contents

1. References.....	1
2. Terms and Definitions	1
3. Introduction	2
4. Design Operation	3
5. Conclusion	7
6. Revision History	8

1. References

For related documents and software please visit [GreenPAK™ Programmable Mixed-Signal Products | Renesas](#)

Download our free Go Configure Software Hub [1] to open configuration (.gp) files [2], review and edit the proposed circuit design. Use GreenPAK development tools [3] to evaluate the configuration on the development board or to program an IC and use it in a circuit. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC. Download SLG47528 [5] and SLG47525 [6] datasheets to get more details on each IC features and parameters.

- [1] [Go Configure Software Hub](#), Software download and user guide
- [2] [AN-CM-382 Low Voltage Bidirectional Level Shifter.gp5](#), GreenPAK design file
- [3] [GreenPAK Development Tools](#), GreenPAK development tools webpage
- [4] [GreenPAK Application Notes](#), GreenPAK application notes library
- [5] SLG47528 Datasheet
- [6] SLG47525 Datasheet
- [7] [Dual Supply GreenPAK](#), Dual supply V_{DD} GreenPAK webpage

2. Terms and Definitions

I2C	Inter-integrated circuit (bus)
IC	Integrated circuit
IO	Input/output
LUT	Look-up table

3. Introduction

Modern systems are increasingly becoming more complex in order to satisfy the needs of the user, to be competitive on the market, and to provide their products with unique functions. In most cases, this leads to the use of various elements, among which there may be those that work in different voltage ranges. This may be due to better technical performance in a particular voltage range, lower current consumption, less noise, lower IC price, etc.

Level Shifters are needed to provide communication between circuit elements operating between different supply voltages. They are based on dual V_{DD} chips that have pins with switching thresholds corresponding to V_{DD1} and V_{DD2} . We remind you the Renesas portfolio includes GreenPAK ICs with dual V_{DD} supply operation. More information about these devices can be found in link [7] in the References section.

A new generation dual supply GreenPAK ICs, which includes the SLG47528 and SLG47525, is characterized by their wide voltage ranges of V_{DD1} : 1.71 V – 5.50 V and V_{DD2} : 0.95 V – 1.98 V. This feature makes them unique, making it possible to work with low voltages.

A block diagram of a level shifter based on SLG47528 or SLG47525 ICs is shown in Figure 1.

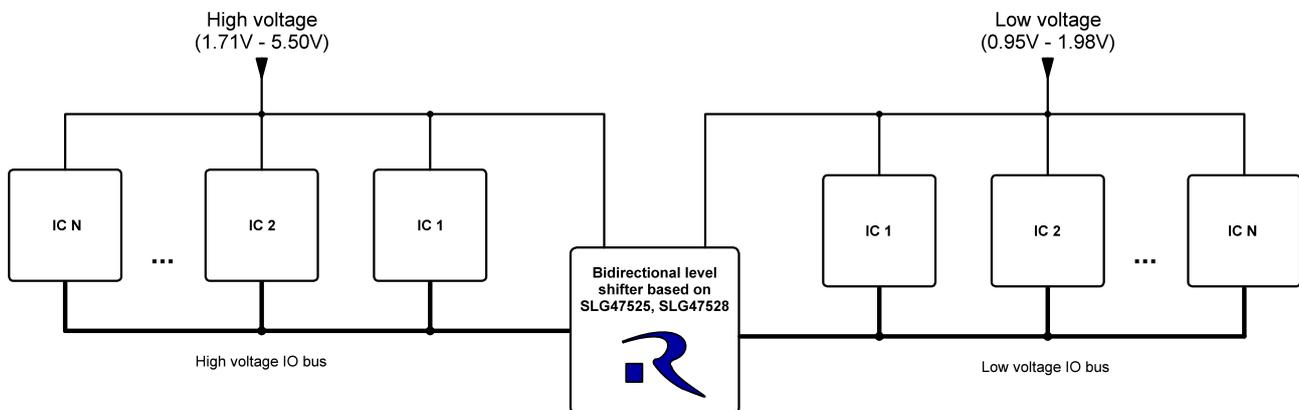


Figure 1: Typical Block Diagram for Bidirectional Level Shifting

The SLG47525 is a smaller version of the SLG47528. These ICs are very similar in terms of functionality and internal components. One of the main differences is the size of the package and number of pins: 2 mm x 2.2 mm 14-pin (SLG47525) and 2 mm x 3 mm 20-pin (SLG47528). The SLG47525, unlike the SLG47528, does not have a temperature sensor. Both chips, in addition to having a 25 kHz / 2 MHz oscillator, also have a built-in 25 MHz oscillator that makes it possible to control short delays. This feature is used to provide high speed for bidirectional level shifting.

The GreenPAK family ICs are completely asynchronous devices and do not require a connected clock to operate. However, external oscillators can be used to provide delay and counter functions when needed.

Level shifters can be used not only to ensure communication (via I²C, SPI, etc.) between ICs with different supply voltages, but also can be used as a device that can disable certain communication lines that are not currently in use.

4. Design Operation

A bidirectional level shifter with enable function, which in our case works with the I²C bus at a frequency up to 1 MHz is shown in the circuit pictured in [Figure 2](#).

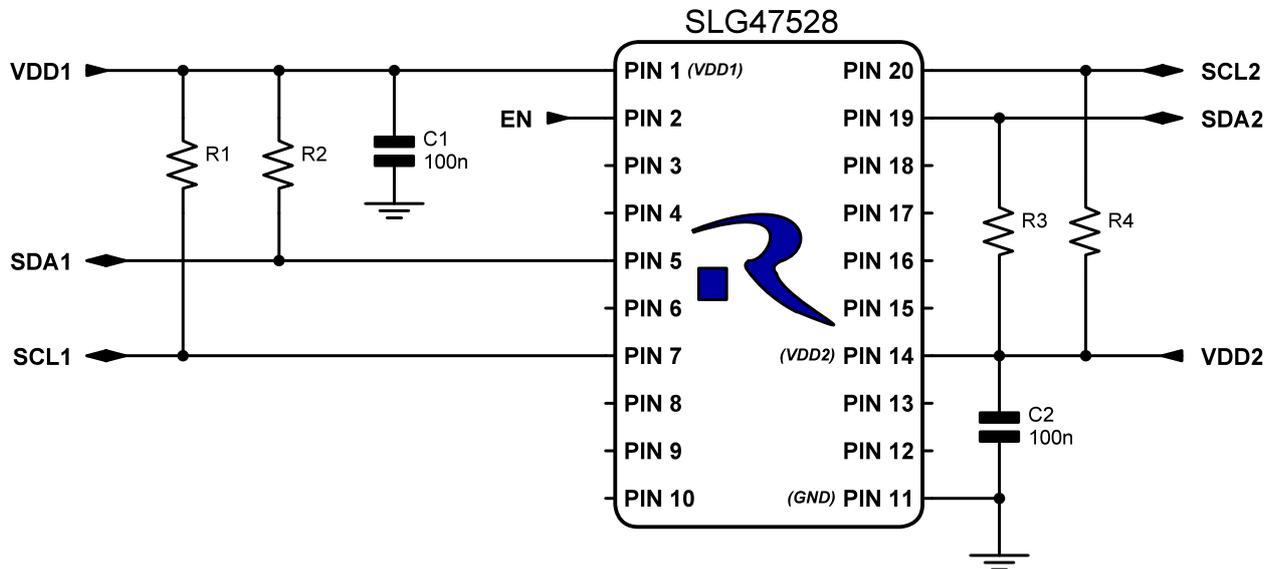


Figure 2: Bidirectional I²C Level Shifter Circuit

Pins associated with V_{DD1} are marked on the design in blue, and pins associated with V_{DD2} are yellow (see [Figure 3](#)). Most pins are universal and can be configured as either as an input, an output, or as bidirectional IO. The last configuration has an additional OE input, which is an output enable. When a logic “0” is connected to this input, the IO operates as an input, when a logic “1” is connected, the IO operates as an output. IOs without an OE input must be preconfigured as either input or output, and dynamic switching between input/output functions is not permitted. Some pins have certain restrictions regarding possible configurations. For example, Pin 2 can only be an input, and pins used in internal I²C slave operations (Pin 8, 9, 16, and 17 of the SLG47528 and Pin 6, 7, 12, and 13 of the SLG47525) do not have a PMOS component in the output configuration. These features must be taken into account when creating a design.

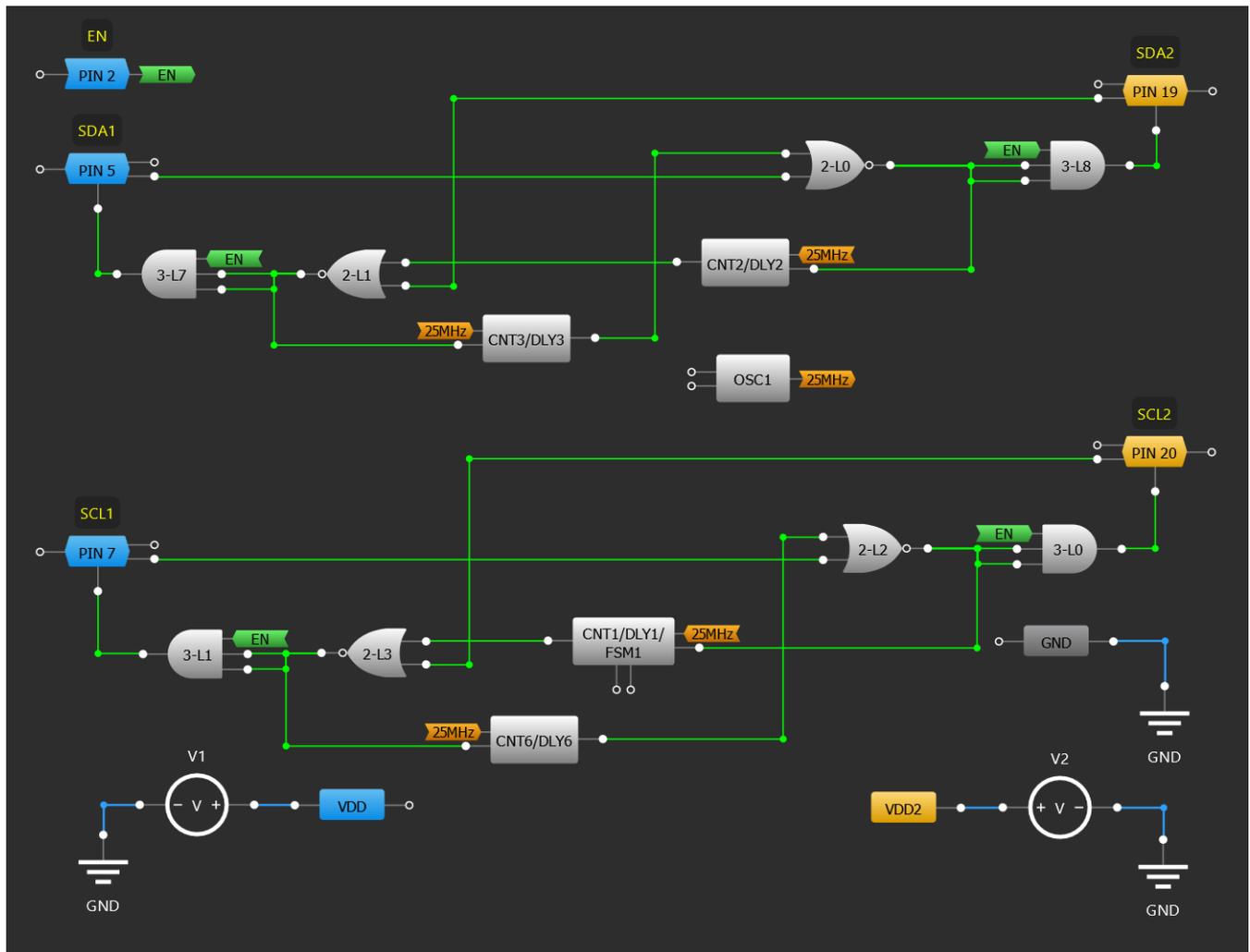


Figure 3: Bidirectional I²C Level Shifter Design

Figure 3 shows the design of the I²C level shifter as seen in the GreenPAK Designer software (Go Configure Software Hub) [1]. Pin 5 and Pin 7 belong to high voltage V_{DD1} , while Pin 19 and 20 belong to low voltage V_{DD2} . They each have a bidirectional configuration for sending data in both directions. In input mode ($OE = 0$) these pins are configured as digital inputs without Schmitt trigger, and configured in output mode ($OE = 1$) as Open Drain NMOS. At the same time, all of the pins mentioned above must have external pull-up resistors to V_{DD1} and V_{DD2} accordingly (see Figure 2). It is critical to have these pull-up resistors because it is not permitted to disconnect the IC from V_{DD} when voltage is applied to other pins, because in this case there will be a voltage higher than V_{DD} on the level shifter pins, and this will cause current to flow through the internal ESD protection diode, which can lead to unpredictable GreenPAK IC operation and damage.

The design also includes 2-bit LUTs which are configured as NOR logic. They control the OE input of pins via 3-bit LUTs configured as logic ANDs where an EN (Enable) input is connected. With $EN = 0$, these 3-bit LUTs output “0” to the OE input of the pins keeping them in a high impedance input configuration.

CNT/DLY blocks are also used and configured as falling edge delays. They are required to avoid instantaneous switching of pins from input mode to output mode. This will be described in more detail below.

At IC power-up, all of the logic blocks’ outputs are initially set to “0”, meaning $OE = 0$ and the pins will be configured as inputs. At the same time, the level shifter pins are pulled to the corresponding V_{DD} and will have a value of “1”. This “1” transmitted from each pin to the 2-bit LUTs (NOR) will support “0” at the outputs of these LUTs, which through the 3-bit LUTs will transmit a “0” to the OE of the pins, keeping them in input mode.

Suppose at some point a logic “0” is applied to Pin 5. At the same time, it is an input at that moment and the output of 2-bit LUT1 is “0”. This “0” from 2-bit LUT1 is sent to the input of CNT/DLY3 (falling edge delay) and maintains “0” at the output of CNT/DLY3, which then goes to one of the inputs of 2-bit LUT0. The other input of this LUT is connected to Pin 5, which is also currently “0”. The output of 2-bit LUT0 becomes “1”, which puts Pin 19 in output mode ($OE = 1$). Since output mode dictates that all of the level shifter pins are configured as NMOS outputs and their inputs are not connected (which means that they are connected to GND), that results in Pin19 being in a logic “0” state. At the same time, its input to the matrix also becomes “0”. CNT/DLY2 transmits a “1” from 2-bit LUT0 to 2-bit LUT1, but considering that CNT/DLY2 has a certain propagation delay, the signal will not pass through it instantly. Therefore, a situation may occur that both inputs of 2-bit LUT1 will become “0” for a short period of time, which will give “1” at the output of 2-bit LUT1 and set Pin 5 from input mode to output mode.

This situation is called a race condition. To avoid this, the design uses 3-bit LUT0, 1, 7, and 8. In addition to the AND gate function, they provide an additional delay in a range of several ns, which makes it possible to avoid the race condition and ensure that the “1” from the 2-bit LUT0 output goes to the input of the 2-bit LUT1 via CNT/DLY2 first. This “1” at the input of 2-bit LUT1 will provide a “0” at its output and keeps Pin 5 in input mode.

After some time, “0” is removed from Pin 5 and its corresponding resistor pulls it up to V_{DD1} . At some point, the voltage on Pin 5 will cross its threshold and Pin 5 will change to a logic “1” state. This “1” will cause a “0” to appear at the output of 2-bit LUT0, which after a few ns will set Pin 19 to input mode. The resistor on Pin 19 will start to pull it up to V_{DD2} , but some time is required for the voltage on this pin to reach a threshold value and be considered as a logic “1”. During this time, Pin 19 will be in logic “0” state, which will be transmitted to 2-bit LUT1.

We remember that the output of 2-bit LUT0 is also “0”, and if we did not have CNT/DLY2 (falling edge delay) in our circuit, then this “0” would be transferred immediately to the input of 2-bit LUT1, which results in a “1” at its output and sets Pin 5 to output mode with a logic level of “0”. It is CNT/DLY2 that holds the “1” at the input of 2-bit LUT1 for a certain time, enough time for the resistor to pull Pin 19 to a voltage higher than its threshold, which transfers a “1” to one of 2-bit LUT1 inputs and keeps Pin 5 in input mode.

Therefore, for the correct operation of the bidirectional level shifter, it is necessary to select the values of the pull-up resistors and the delays for CNT/DLY1, 2, 3, and 6 in such a way that the delay time is greater than the time of the voltage rise (t_{RISE}) on the pins to reach the needed threshold level (see [Figure 4](#)).

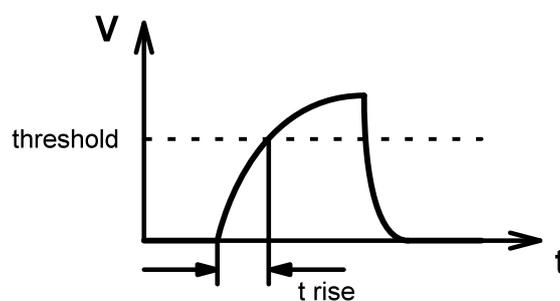


Figure 4: Pin Voltage Rise Time Definition

The following scope shots show the result of the bidirectional I²C level shifter operation at a frequency of 1 MHz in cases where the Master is connected to the high voltage V_{DD} (3.3 V), and the Slave to the low voltage V_{DD} (1.2 V) and vice versa (see [Figure 5](#) to [Figure 8](#)).

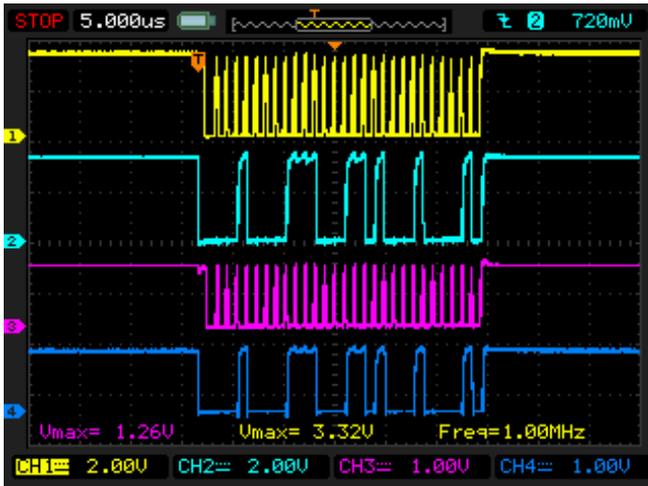


Figure 5: High to Low Voltage Level Shifting

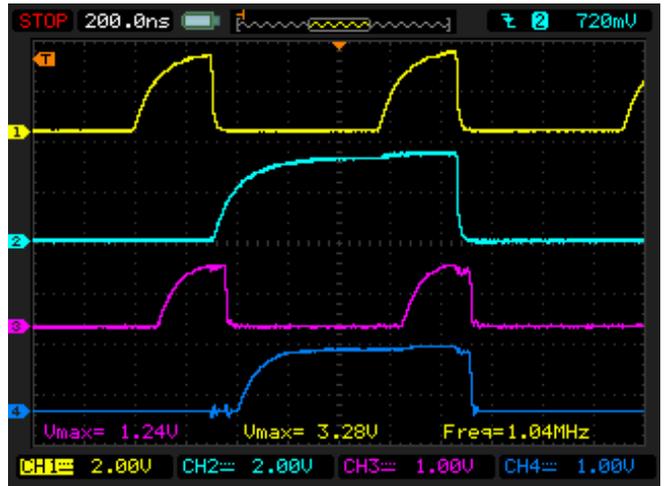


Figure 6: High to Low Voltage Level Shifting Zoomed

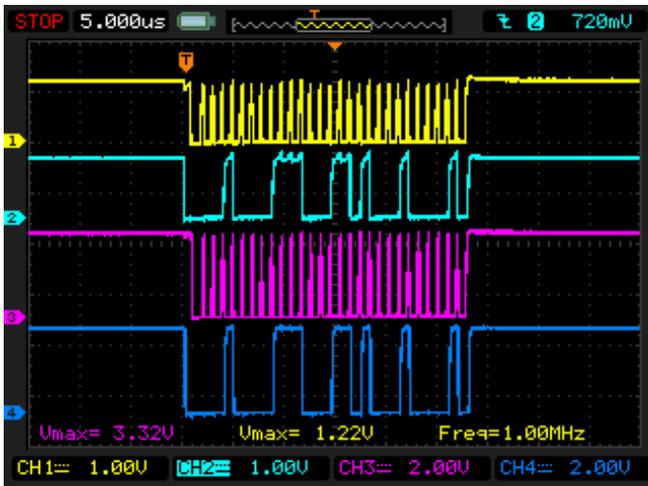


Figure 7: Low to High Voltage Level Shifting

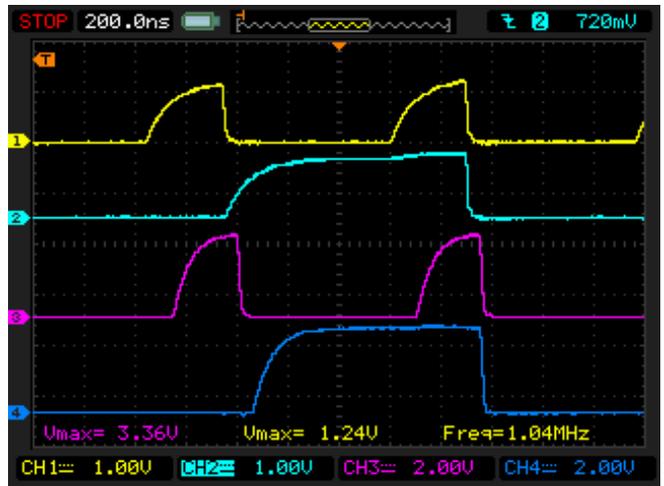


Figure 8: Low to High Voltage Level Shifting Zoomed

5. Conclusion

Based on the contents provided in this Application Note we can conclude that the SLG47528 and SLG47525 GreenPAK ICs are perfect devices for single and bidirectional, high speed voltage level transitions for communications between components powered with different power domains.

6. Revision History

Revision	Date	Description
1.00	Aug 14, 2024	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.