Signal Conditioner for a Pressure Sensor
SLG47011

The application note describes the Signal Conditioner design for Wheatstone bridge sensors. A unique set of the ADC, DAC, Memory Table, Multichannel DCMP, Math Core, and additional internal logic of the SLG47011 is used to achieve the best precision of this analog interface. The application note contains a complete schematic of an analog front end for a low-cost pressure sensor with offset and gain error compensation over temperature.

The application note comes complete with design files which can be found in the Reference section.

Contents

Figures

Tables

1. Terms and Definitions

DFF	D Flip-Flop
FS	Full Scale
GBWP	Gain Bandwidth Product
LUT	Look-up Table
MF	Multi-Function
OSC	Oscillator

2. References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .app files [2] and view the proposed circuit design. Use the AnalogPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-373 Signal Conditioner for a Pressure Sensor.aap, Design file, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

[5] SLG47011 Datasheet, Renesas Electronics

[6] NTC Thermistors Datasheet, Murata Manufacturing Co

Authors:

Irena Zhuravchak, Technical Documentation Apps Engineer, Renesas Electronics

Bohdan Kholod, Sr. Product Development Engineer, Renesas Electronics

3. Introduction

In the following application note, the AnalogPAK SLG47011 is used as the Signal Conditioner for a Wheatstone bridge pressure sensor with offset and gain error compensation over temperature.

The PGA within the SLG47011 is used to create a 32x instrumentation amplifier.

Multichannel DCMP, Memory Table, Buffer, and additional internal logic are used to select a corresponding temperature range. Then Memory Table, Buffer, and Math Core are used for gain error tuning and offset compensation and allow to save hardware resources, as well as minimizing the cost of the AFE.

The SLG47011 allows two different ways of interfacing sensors with and without internal reference sources:

- The common way is to supply all analog blocks (sensors, ADC, DAC for compensating offset) from one voltage source. The measurements are ratiometric. Variations in supply voltage don't affect accuracy. An external temperature sensor could be used. This way is used in this application note.
- The supply voltage for the sensor and DAC must be stable and constant. That's why, for this case, an external high-precision voltage source should be used. In this case, an internal buffered Vref and Temp Sensor of the SLG47011 could be used.

4. Input Parameters

This section shows the specifications of the SLG47011, pressure sensor, and thermistor used in this application note.

SLG47011 Characteristics

Parameter	Possible Value	Value in this Design
V_{DD} Input Range	1.71-3.63 V	3.3 V
ADC	12/14-bit	12-bit
DAC	12-bit	12-bit
Compensation (T - temperature, K – gain error, B - offset)	12-bit	12-bit
ADC Vref	V_{DD}/2, 1.62 V	V_{DD}/2
Diff FS of the ADC input	-Vref/2 to +Vref/2	-825 mV to +825 mV
DAC Vref	V_{DD}/2, 1.62 V	1.62 V

Pressure Sensor Characteristics

Parameter	Value
V_{DD}	3.3 V
Vdiff	-10 mV to +10 mV
Gain Error	±1% @ dT = 12.5℃
Offset	±15 mV @ FS

Thermistor NTC XH103 10 k Characteristics ([6] above)

Temperature	Thermistor Resistance
T, °C	R, kOhm
-40	195,65
-35	148,17
-30	113,35
-27,5	100,45
-25	87,56
-20	68,24
-15	53,65
-10	42,51
-5	33,89
-2,5	30,56
0	27,22
5	22,02
10	17,93
15	14,67
20	12,08
22,5	11,04
25	10
30	8,32
35	6,95
40	5,83
45	4,92
47,5	4,54
50	4,16
55	3,54
60	3,01
65	2,59
70	2,23
72,5	2,08
75	1,93
80	1,67

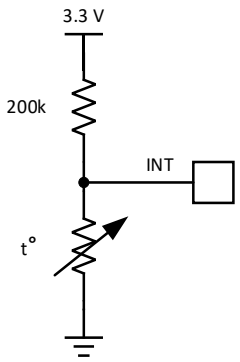

Figure 1. Voltage Divider

5. Operating Principle

The Simplified Block Diagram is shown in Figure 2.

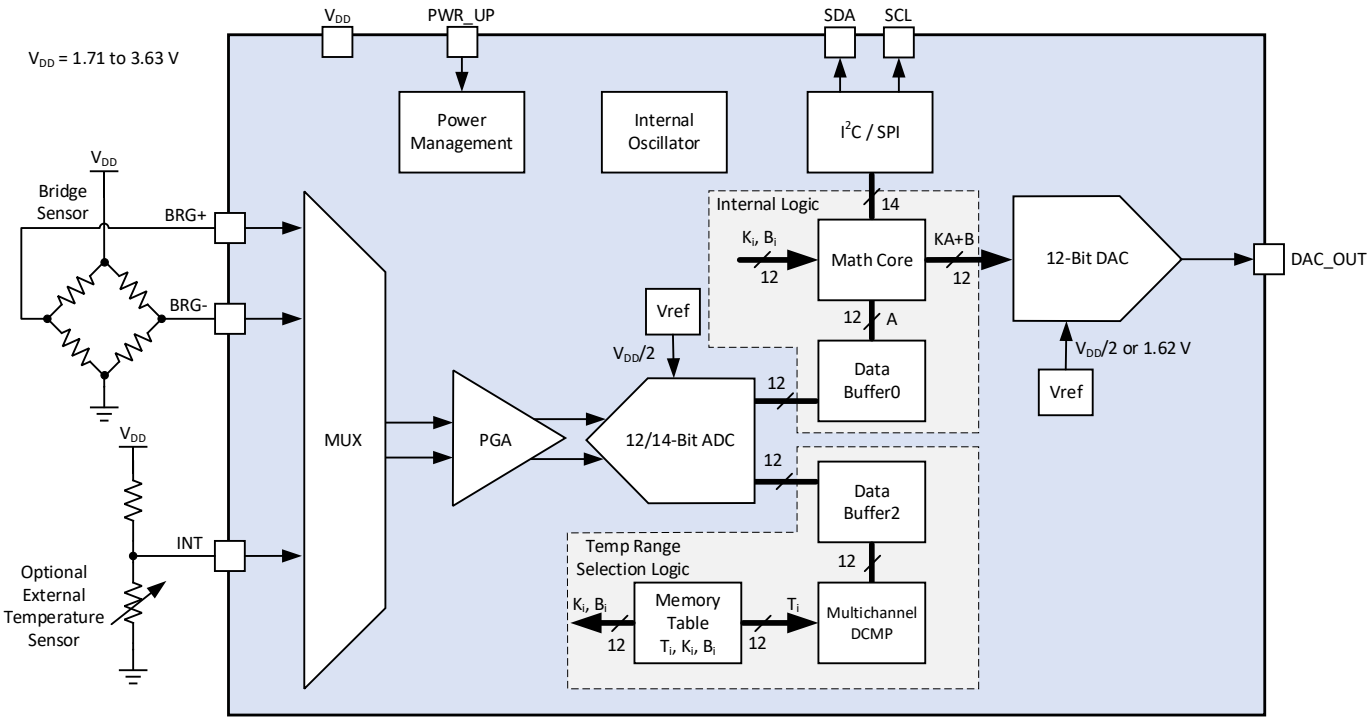

Figure 2. Simplified Block Diagram

Signals BRG+ and BRG- come to PGA, the differential voltage on the sensor is measured and multiplied by 32, and then this signal goes to Channel 1 of the ADC.

The output of the voltage resistive divider with a thermistor (NTC XH103 10 k) goes to PGA (1x gain) and Channel 0 of the ADC. It is necessary to compensate for the temperature impact on the gain error and offset errors, as they change with temperature.

During the sampling of the Channel 1 (pressure sensor), the corresponding temperature threshold is selected. For each threshold T, there are corresponding gain error K and offset B* (B – corrected value) coefficients.

Then this sampled data “A” (from the pressure sensor) is compensated in the Math Core, and the output is K x A + B*. In our case (A + B) x K, where B = B*/K.

After compensation, data goes to a 12-bit DAC which outputs analog voltage to the physical PIN (GPIO8) directly.

6. Tuning of Gain Error and Offset Compensating of the System

6.1 Calculation of Gain and Offset Coefficients. Transfer Function of the System

Firstly, there is a need to determine the coefficients K (gain error) and B* (offset) / B (corrected offset) for compensation of the output signal of the pressure sensor. Since the gain error and offset of the sensor also depend on temperature, it is necessary to add temperature compensation. In this application note, 10 temperature thresholds from -40 to 85 ˚C are considered. So, there are 10 values of temperature thresholds and 10 corresponding values of K and B.

Note: coefficients will be written to the Memory table. One coefficient corresponds to one word. One word is 4096 bits. All coefficients (temperature threshold, offset, and gain error) should be recorded so that the maximum value does not exceed 4095.

We have calculated values of the temperature thresholds (INT). The maximum voltage INT should be not higher than Vref of 1.65 V (half of V_{DD} = 3.3 V / 2).

Note: in this case, Vref = 1650 mV, dec code = 4095 for all following calculations.

So, the resistor value was selected 200k to obtain 1650 mV (see Range 1 in Table 1). This maximum value of the resistor divider output corresponds to the code 4095 (dec) or FFF (hex). The code (T) for all the following temperature threshold voltages will be calculated relative to this maximum value using the formula:

$$T_{dec} = INT_{\ i} \cdot \frac{4095}{Vref}$$

In our case:

$$T_{dec} = INT_{\ i} \cdot \frac{4095}{1650},$$

where INT – temperature threshold in mV.

Table 1. Temperature Threshold

Range	Temperature	Thermistor Resistance	Temp Threshold		
	T, °C	R, kOhm	INT, mV	T, dec	T, hex
1	+72,5 to +85	2,08	33,91	84	54
2	+60 to +72,5	3,01	48,99	122	7A
3	+47,5 to +60	4,54	73,23	182	B6
4	+35 to +47,5	6,95	110,79	275	113
5	+22,5 to +35	11,04	172,64	428	1AC
6	+10 to +22,5	17,93	271,45	674	2A2
7	-2,5 to +10	30,56	437,35	1085	43D
8	-15 to -2,5	53,65	697,99	1732	6C4
9	-27,5 to -15	100,45	1103,32	2738	AB2
10	-40 to -27,5	195,65	1631,87	4095	FFF

Note: all calculated dec codes for T (temperature thresholds), K (gain error), B* (offset), and B (corrected offset) should be rounded to an integer.

Then we could calculate using the pressure sensor characteristics, or measure offset voltage (B*) in mV for each temperature range. For each offset B* calculate the rounded to integer dec code using the formula (see Table 2).

$$B^{*}Code_{dec} = PGA\ gain \cdot B^{*}_{\ i} \cdot \frac{4095}{Vref}$$

In this case:

$$B^{*}Code_{dec} = 32 \cdot B^{*}_{\ i} \cdot \frac{4095}{1650},$$

where B^{*}_{i} – calculated offset voltage, mV.

As the measured differential voltage (diffV) of the pressure sensor could be both negative and positive, the middle point (mid_p_ADC) of 0 V was added with the 2048 Dec code (12-bit ADC). Thus, negative diffV is between 0 and 2047, and positive diffV is between 2048 and 4095. So, our rounded integer ADC output is:

$$ADC\ output_{dec} = \frac{diffV}{K_i} - B^{*}_{\ i} + mid\_p\_ADC$$

Desired DAC input:

$$DAC\ input_{dec} = diffV + mid\_p\_DAC$$

As DAC is 12-bit as well, *mid_p_ADC* = *mid_p_DAC* = *mid_p* (2048).

If we divide the desired DAC input (the last equation) by K and subtract B, we should get the ADC output:

$$\frac{diffV}{K_i} + \frac{mid\_p}{K_i} - B_i = \frac{diffV}{K_i} - B^*{}_i + mid\_p$$

As we can see, the offset B* must be adjusted according to the derived formula:

$$B_{\ i} = B^*{}_i + mid\_p \cdot (\frac{1}{K_i} - 1)$$

$$B_{\ i} = B^*{}_i + 2048 \cdot (\frac{1}{K_i} - 1)$$

Now this value should be converted to hex. Please note that the obtained B value should not exceed 4095.

See Table 2.

Table 2. Offset and Gain Error

Range	B* (offset)		B (corrected)		K (Span)		
	mV	dec	dec	hex		dec	hex
1	14	1112	1106	451	1,003	2054	806
2	12	953	948	3B4	1,00225	2053	805
3	10	794	453	1C4	1,2	2458	99A
4	8	635	449	1C1	1,1	2253	8CD
5	5	397	397	18D	1	2048	800
6	7	556	577	240	0,99	2028	7EC
7	9	715	757	2F4	0,98	2007	7D7
8	11	874	937	3A8	0,97	1987	7C3
9	13	1032	1118	45D	0,96	1966	7AE
10	15	1192	1299	513	0,95	1946	79A

There is a need to represent each K as a 12-bit number coefficient using the formula:

$$K_{idec} = K_i \cdot 2^{right\ shifting\ value}$$

This formula is a floating-point trick. We represent a floating-point number K_i as a division of a 12-bit number K_{idec} by 2 to the power from 0 to 31 (right shifting value).

For example, range #10 (K = 0.95, right shifting value =11):

$$K_{dec} = 0.95 \cdot 2^{11} = 1946$$

The right shifting value should be the same for all K_i. In Math Core configuration set the right shifting value to the determined one. In this case, the right shifting value = 11. See Table 2 for the result.

After determining the coefficients, they must be recorded in the memory table (see Table 3). The recording rules are as follows:

- The Values in the first two addresses must be 0, they are not used.
- Next, we write down the value of the temperature threshold, the corresponding value of B, and the value of K.

- We repeat this for all 10 temperature ranges in the order indicated in point 2 (temperature threshold, value of offset B, and gain error K).
- The ranges should be in order of increasing temperature threshold value (from lower to higher). The last temperature threshold must be FFF.

Table 3. Example Filling the Memory Table

#	Register	Memory table values, hex	Description
1	4096:4107	0	0
2	4112:4123	0	0
3	4128:4139	54	temp threshold
4	4144:4155	452	coefficient B
5	4160:4171	806	coefficient K
6	4176:4187	7A	temp threshold
7	4192:4203	3B4	coefficient B
8	4208:4219	805	coefficient K
9	4224:4235	B6	temp threshold
10	4240:4251	1C5	coefficient B
11	4256:4267	99A	coefficient K
12	4272:4283	113	temp threshold
13	4288:4299	1C1	coefficient B
14	4304:4315	8CD	coefficient K
15	4320:4331	1AC	temp threshold
16	4336:4347	18D	coefficient B
17	4352:4363	800	coefficient K
18	4368:4379	2A2	temp threshold
19	4384:4395	240	coefficient B
20	4400:4411	7EC	coefficient K
21	4416:4427	43D	temp threshold
22	4432:4443	2F4	coefficient B
23	4448:4459	7D7	coefficient K
24	4464:4475	6C4	temp threshold
25	4480:4491	3A9	coefficient B
26	4496:4507	7C3	coefficient K
27	4512:4523	AB2	temp threshold
28	4528:4539	45E	coefficient B
29	4544:4555	7AE	coefficient K
30	4560:4571	FFF	temp threshold
31	4576:4587	513	coefficient B
32	4592:4603	79A	coefficient K

Note: if the offset B* is small enough, the design could be done on 14-bit ADC.

The transfer function for the full scale of the ADC input (from -825 mV to + 825 mV for this example) is shown below in Figure 3.

Red line - ADC output, transfer function before the gain error and offset error compensation.

Green line – DAC input, calculated ideal transfer function after gain error and offset error compensation.

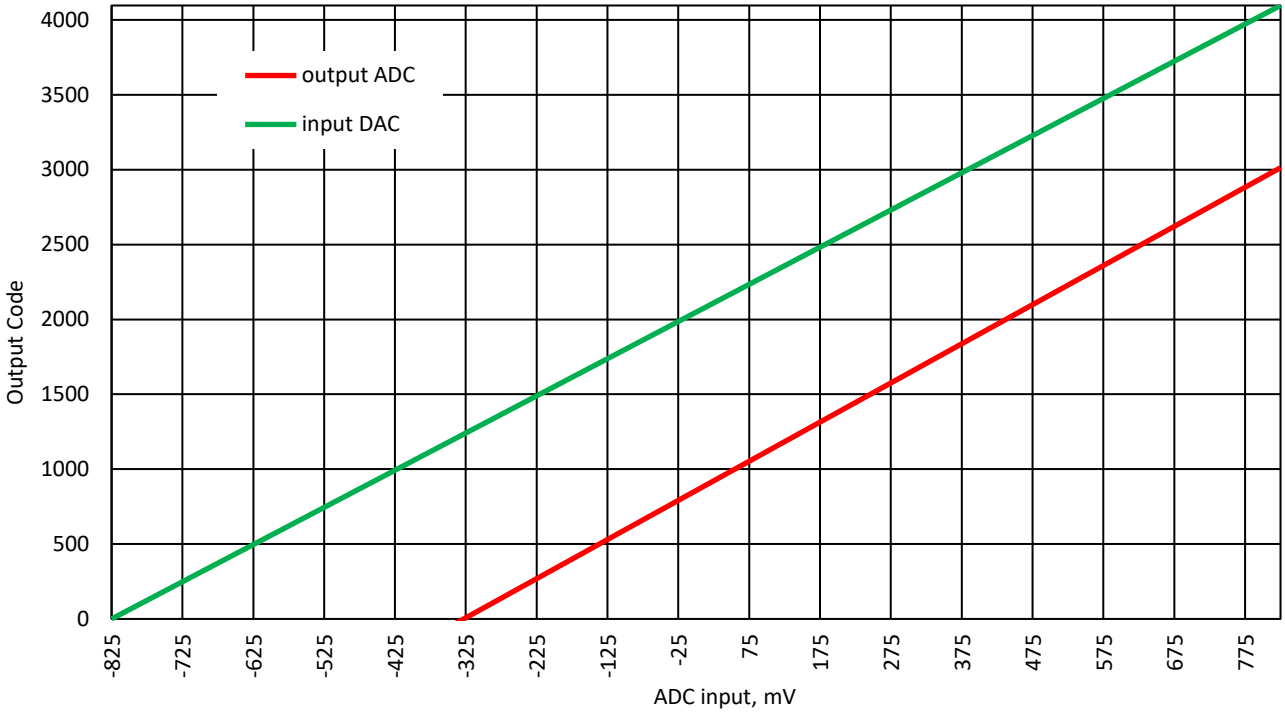

Figure 3. Transfer Function, FS = ADC input, Temperature Range 10

6.2 Algorithm for Tuning Gain and Offset of the System

In practice, a simple tuning algorithm can be used to avoid complex calculation of offset and gain error coefficients.

1. Set the first five values of the Memory Table as follows:

#	Register	Memory table values, hex	Description
1	4096:4107	0	0
2	4112:4123	0	0
3	4128:4139	FFF	temp threshold
4	4144:4155	0	coefficient B
5	4160:4171	800	coefficient K

Set the Right Shifting Value of the Math Core to 11.

In this case the Math Core output = A (data from pressure sensor without compensation) as B = 0, and K after right shifting = 1.

2. For each temperature range, tune the corrected offset B of the pressure sensor with no load via I2C/SPI (Registers -> Bytes 16B and 16C, see Figure 4).

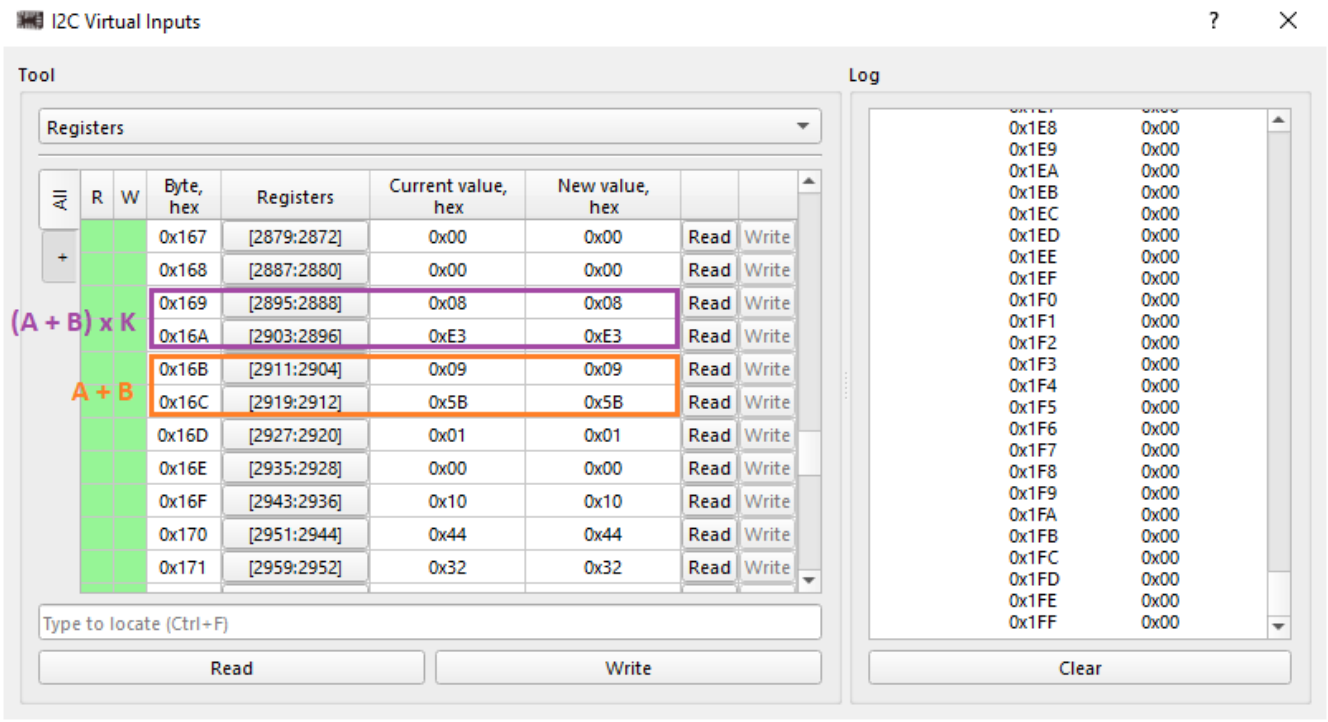

Figure 4. Math Core Values

3. Load the sensor with a known load and compare the obtained value with the predicted one. Tune the gain error K (Bytes 169 and 16A, see Figure 4).
4. Measure and tune the corrected offset B again with no load.
5. Steps #3 and #4 could be repeated several more times for greater accuracy.
6. Fill the Memory Table with obtained values of temperature thresholds T, corrected offset B, and gain error K as was shown in Table 3.

7. GreenPAK Design

The GreenPAK Design is shown in Figure 5.

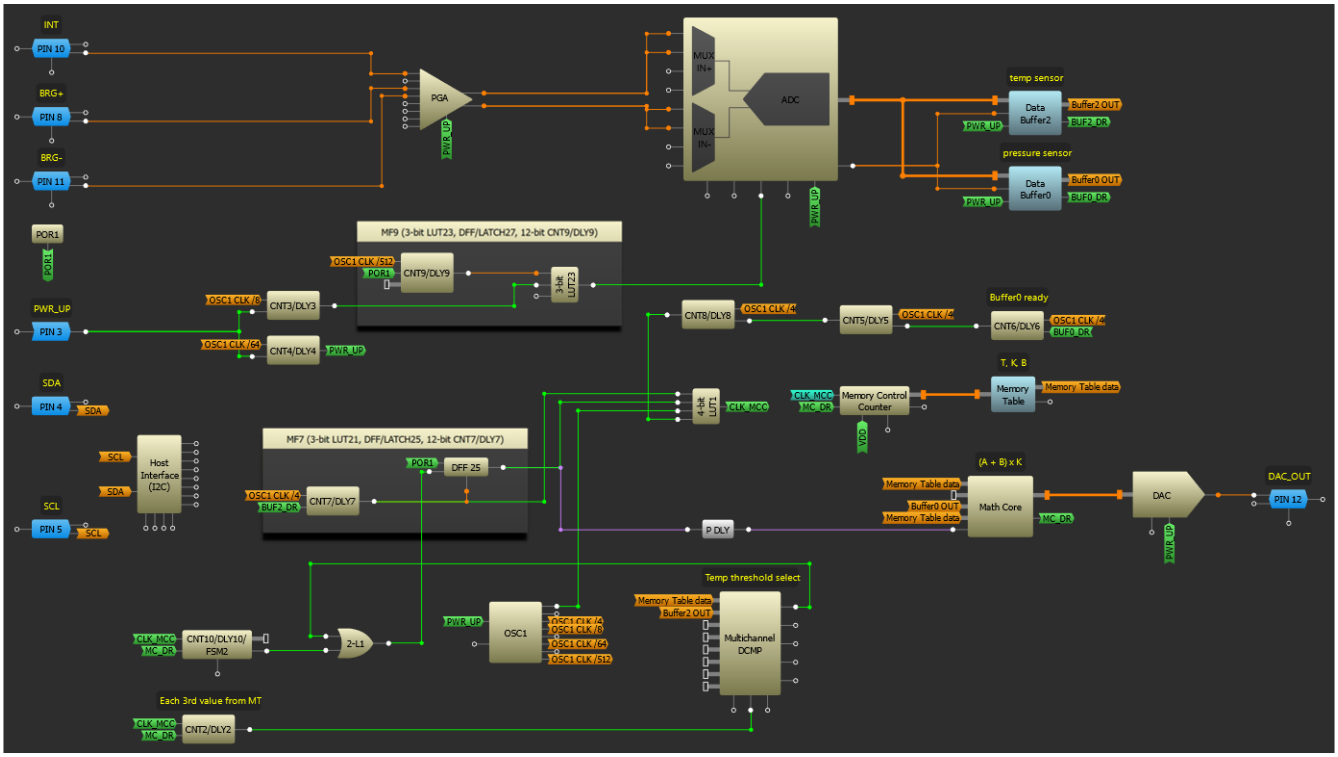

Figure 5. GreenPAK Design

DLY3, DLY4, and DLY9 are used to correctly turn on the ADC after the first turn on when the POR arrives, as well as in further work when turning on and off the ADC from the PIN 3 (PWR_UP).

The signal from the thermistor (NTC XH103 10 k) resistive divider comes to the single-ended input of the PGA Channel.

Signals from the pressure sensor outputs come to the differential input of the PGA Channel 0 with 32x gain.

Then these signals go to ADC, which measures 7 samples of Pressure Sensor. Between 7 and 8 samples of the pressure sensor measurements, the temperature range selection occurs.

CNT7 is responsible for scanning all eight samples for temperature. Thus, the delay time between channels in the ADC must be longer than the time in the CNT7. Also, consider the closed-loop bandwidth (GBWP/Gain) when setting the delay time. See more in datasheet section 3.8 Programmable Gain Amplifier Specifications.

The data from the temperature sensor is written to Buffer2 and from the pressure sensor is written to Buffer0. Both Buffers are set to Moving Average Mode (8 words). Averaging allows to filter of input noise.

The data-ready signal will be “0” until the temperature range and its corresponding compensation coefficients are determined.

In other words, the ADC must process the signal from the pressure sensor for a longer time in order to have time to determine the temperature range, so that when the data is ready, the coefficients for this data correction are known as well.

The values of One Shot CNT7 data, Upper Limit of Memory Control Counter, and Memory Table size are the same and equal to (3 x number of ranges) + 2.

For example, in our case for 10 ranges: 3 x 10 + 2 = 32 – the value of CNT7 Data, Upper Limit of Memory Control Counter, and Memory Table size.

The value for counter CNT10 Data is (CNT7 Data - 3). For our case with 10 ranges CNT10 Data = 32 – 3 = 29.

CNT2 is used to turn on Multichannel DCMP at times when the temperature threshold value is in memory, its CNT2 data = 2 (every third value), and it does not need to be changed. When CNT2 output is LOW (k and b in the Memory Table), MDCMP is turned off. When the CNT2 output is HIGH (the temperature threshold is in the Memory Table), the Enable signal of the Multichannel DCMP is HIGH, and the Multichannel DCMP starts comparing data from the temp sensor (Buffer2 OUT) and temperature threshold from the Memory Table.

If the required threshold is found, the DCMP output0 is HIGH, there are no clocks on DCMP, Data Ready (MC_DR) is HIGH -> the Memory Control Counter clocks two times to write B and K to the Math Core. CNT5, CNT6, and CNT8 are used to generate 2 pulses that will write the values of B and K to the Math Core.

Math Core is configured as “Adder/Subtractor -> Multiplier” with the output formula:

$$\text{Math Core OUT} = (A + B) \times K,$$

Where A – Buffer0 OUT (pressure sensor data),

B – corrected offset value, coefficient from the Memory Table

K – gain error, coefficient from the Memory Table.

Note 1: if the measured offset is positive, the “Adder / Subtractor enable” of Math Core should be set to “Subtractor”. If the measured offset is negative, the “Adder / Subtractor enable” of Math Core should be set to “Adder”.

Note 2: Math Core has a feature of automatic selection of Adder / Subtractor functionality by analyzing the MSB of memory table word. See more in the SLG47011 Datasheet section Mathematical Core Macrocell.

The Math Core right shifting value is set to 11.

In the **DAC** settings, the user chooses which data to take from the Math Core depending on the predicted bit rate at the Math Core output after its addition and multiplication. Since we had a 12-bit ADC configuration in this case, we should choose Math OUT [11:0]. If ADC is set to 14-bit, DAC out should be set to Math OUT [13:2].

Also, it is possible to choose the Vref – AVDD divider (1.65 V in our case) or internal Vref 1.62 V.

The DAC output voltage is equal:

$$V_{DAC\_OUT} = \text{DAC input code} * \text{Vref} / 4095,$$

where DAC input code = Math Core OUT.

The software window I2C Virtual Inputs allows to check the Buffer0, Buffer2, Math Core Adder out, Math Core Multiplier out:

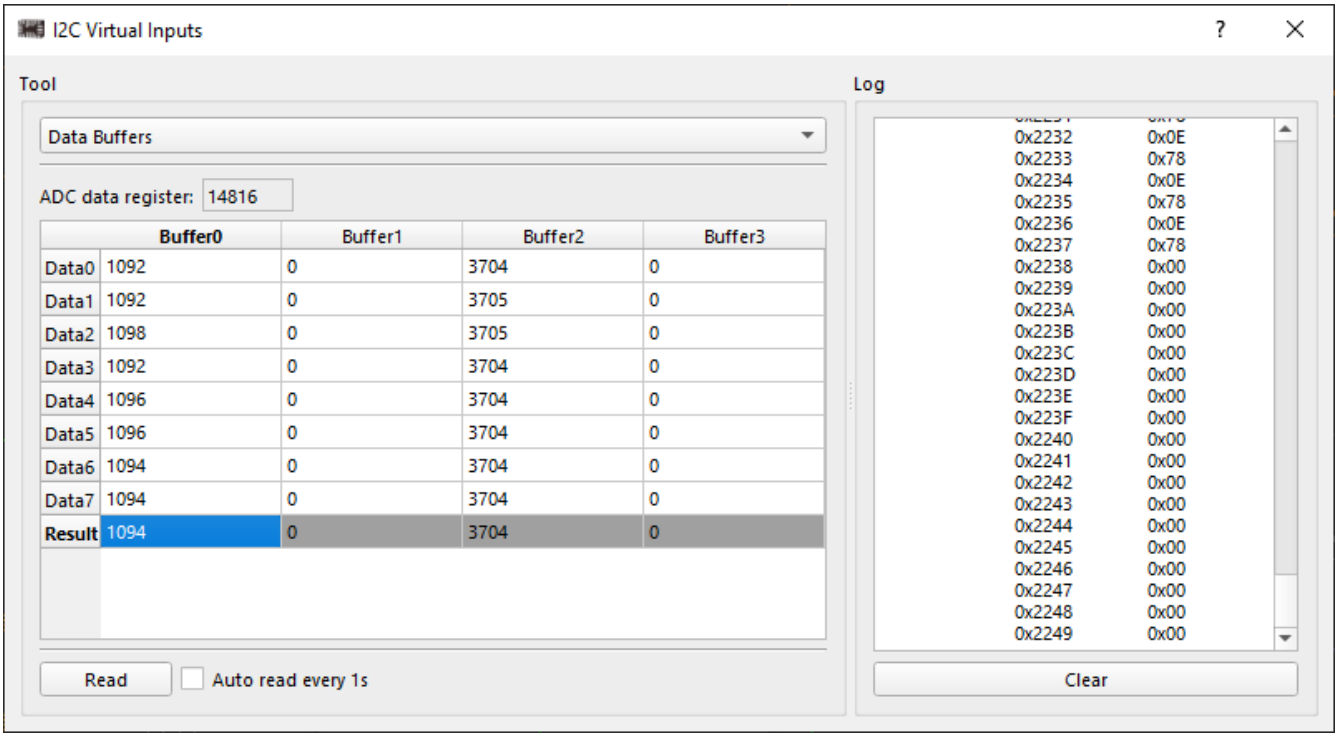

Figure 6. Buffers Values

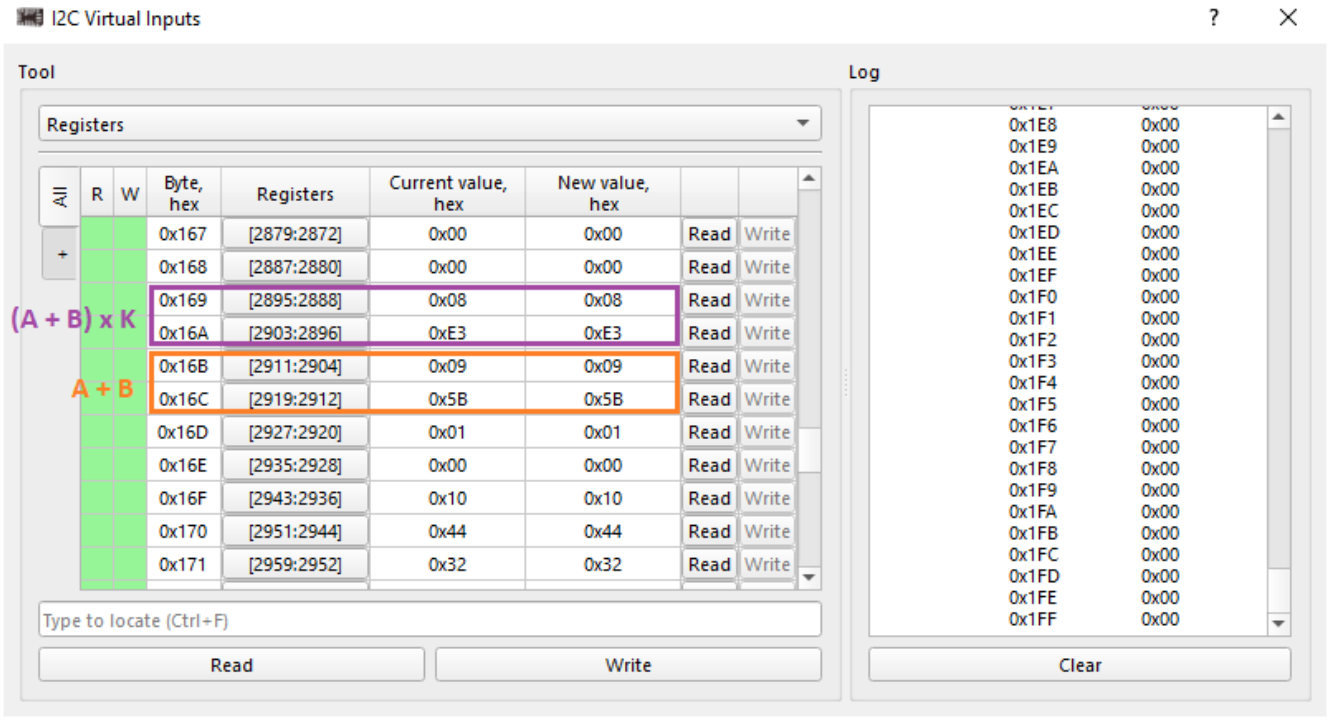

Figure 7. Math Core Values

7.1 How to Customize My GreenPAK Design

Some macrocells' settings depend on the number of ranges.

The values of One Shot CNT7 Data, Upper Limit of Memory Control Counter, and Memory Table size are the same and are defined as follows:

$$value = (3 \times number\ of\ ranges) + 2$$

For example, if you need 15 ranges:

$$value = 3 \times 15 + 2 = 47$$

The value for counter CNT10 data is (CNT7 data - 3). For our case with 10 ranges CNT10 data = 47 – 3 = 44.

8. Conclusion

This application note describes how to configure the AnalogPAK SLG47011 to create a signal conditioner for a Wheatstone bridge pressure sensor with offset and gain error compensation over temperature. The application note contains step by step guide for tuning the offset and gain error compensation coefficients. The design precision is 12/14-bit input, 12/16-bit output (16 is Math Core registers allowable via I2C/SPI). This design also provides ratiometric measurements and temperature compensation with internal or external temperature sensor.

The PAK's internal resources, including the Memory Table, ADC, buffers, Math Core, Memory Control Counter, DAC, oscillators, logic, and GPIOs are easy to configure to implement the desired functionality for this design.

9. Revision History

Revision	Date	Description
1.00	Sep 23, 2024	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.