Power Profile for Advanced Sensor Applications
SLG51002

This application note explores how to use the SLG51002 as a highly stable dual camera power system. The system incorporates two independent power sequencers with high LDO characteristics. The SLG51002 contains eight compact and customizable low dropout regulators, and it is designed for high performance camera modules and other small multi-rail applications.

Contents

1. References

For related documents and software, please visit:

https://www.renesas.com/eu/en/products/power-power-management/multi-channel-power-management-ics-pmics/low-power-portable-pmics/slg51002-pmic-high-psrr-low-noise-multi-output-ldos-and-integrated-load-switches#overview

Download our free Go Configure Software Hub [1] to open the .ppak files [2] and view the proposed circuit design. See the full specifications of SLG51002 in the datasheet [3].

[1] Go Configure Software Hub, Software Download and User Guide
[2] AN-CM-357 Power Profile for Advanced Sensor Applications.ppak, Design File
[3] SLG51002 Datasheet, SLG51002 Datasheet

2. Introduction

Modern electronic devices often have at least a few analog rails in their power profile. This is true for consumer electronics, automotive, medicine, smart home devices, and more. Building an optimized power profile requires devices to be space constrained and efficient both in functionality and current consumption.

It is important to select advanced sensors or other analog power components at the design phase. It is also important to select a clear power supply to achieve desired system performance. Examples of such building blocks include:

- MCU (ADC, DAC, COMP)
- Wireless interface (Fast CLK supply, LNA, filtering cascades)
- Display sensor (analog circuit supply)
- Image sensor (analog supply)

- Other advanced sensors as LIDAR, IR-camera, etc.

Power management integrated circuits (PMIC) can be used for this purpose. A PMIC is used to provide high-quality power while saving PCB area. One example is Renesas's SLG51002C chip with a large number of high-performance LDOs, built-in power sequencer, GPIOs, logic elements, temperature sensor, a variety of protection and much more enabling it to replace several other ICs at once. This makes the final product more compact and the development process easier.

3. PMIC-based Solution for Image Sensor Application

An image sensor is a typical power consumer used with a PMIC. It is common for applications such as mobile phones, robotics or AR segments.

Image sensors have a complex power profile both in terms of power consumption (see Table 1), and other qualitive characteristics (such as output noise and PSRR).

Table 1: Power profile of a typical image sensor

Name	Description	Min. Voltage	Max. Voltage	Typ. Current
IOVDD	Input/Output rail VDD	1.6 V	3.0 V	~30 mA
DVDD	Digital rail VDD	0.8 V	1.5 V	~140 mA
AVDD	Analog rail VDD	2.6 V	3.5 V	~40 mA
VDD	VDD (optional)	1.2 V	4.8 V	~12 mA

Proper sequencing is one of the requirements to avoid sensor malfunction and guarantee system reliability. PMICs managed by a power sequencer is a solution often used for applications with image sensors onboard. The sequencer can either be a physical IC or part of a main controller. In any case, they provide proper timings for both power up and power down. Typical image sensor delays between rails are within the range of 10 µs to 10 ms.

Applications with multiple image sensors onboard are popular, and they also require a clear power supply and proper sequencing. This can be covered by dedicated PMICs per sensor and a power sequencer. Although this solution occupies less space than a discrete LDO approach, it takes up space. This is also true for host controller code complexity since sequencing is often handled by its own resources.

A single PMIC solution such as the configurable SLG51002 is an efficient solution for these limitations. You can make effective use of the SLG51002's Power Sequencer thanks to its high flexibility. It covers the functionality of most discrete power sequencers that are timing-based only. It can also provide event-triggered sequencing.

Event triggers can be sourced from a variety of inputs, including: 6 GPIOs, the I2C line, and flags (temperature, VOUT_OK, current limits). Combinational logic elements allow users to create a specific design. For more information about the SLG5100x power sequencer, please refer to AN-CM-356 SLG5100X Power Sequencer.

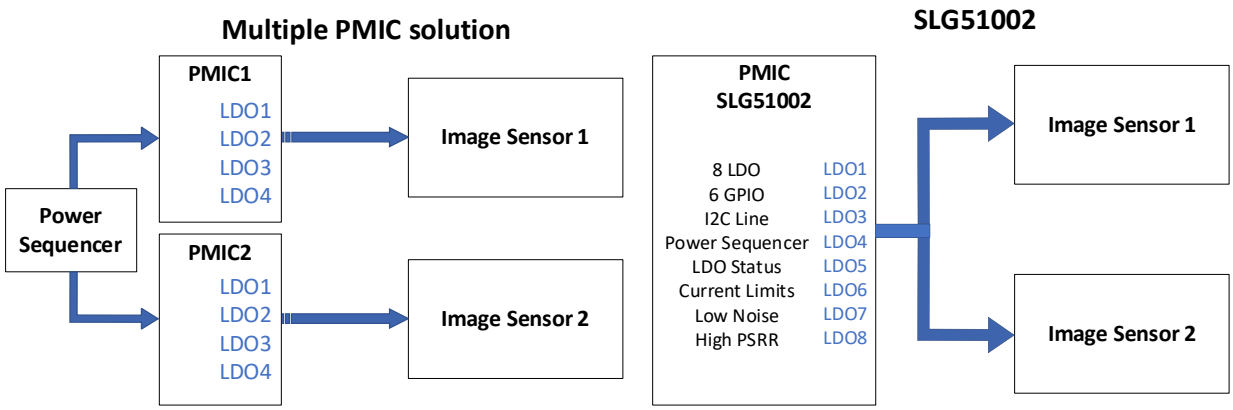

Figure 1: Comparison of multiple PMIC solution with SLG51002 – a single chip one

SLG51002 is a PMIC with 8 LDOs onboard and a variety of benefits, including:

- User configurable settings via I2C interface and OTP (Including output voltage, power sequencing, soft-start timing, and current limit thresholds)
- Soft start and soft shutdown
- Configurable temperature alerts
- PSRR of 83 dB at 1 kHz and 47 dB at 1 MHz (3 x HV LDO)
- Low dropout voltage of 10 mV per 100 mA of load (3 x LV LDO)
- (2 x HC LDO) and (3 x LV LDO) channels have Bypass Mode

With SLG51002, you can save on circuit elements and significantly save space on the board.

4. Scenario of Two Independent Sequence Using SLG51002

This section and any following sections contain the body of the document. Subsections can be added as required. Quick Parts are available for numbered equations, landscape pages, notices, and tables.

Let's show a typical PMIC use case for two image sensors with independent power sequences. Each of these sequences is expected to be triggered by external control signals. The SLG51002 chip is used as a single chip solution for this scenario.

Configuration example: The main task is to reduce the load on MCU (its firmware complexity). The power supply (enable/disable) sequence for image sensor 1 is triggered by a signal on GPIO3. Similarly, image sensor 2 is triggered by GIPO4. The power supply for image sensors 1 and 2 can be controlled independently from each other. As an additional feature, the MCU can check LDO status using GPIO1 for image sensor 1 and GPIO2 for image sensor 2, as well as read them through I2C.

Sensor 1 Sequence includes: 4 power supply rails and an optional status flag (GPIO1 is used). The optional status flag can be implemented at GPIO1—raised if all voltages are VOUT_OK for mentioned power rails.

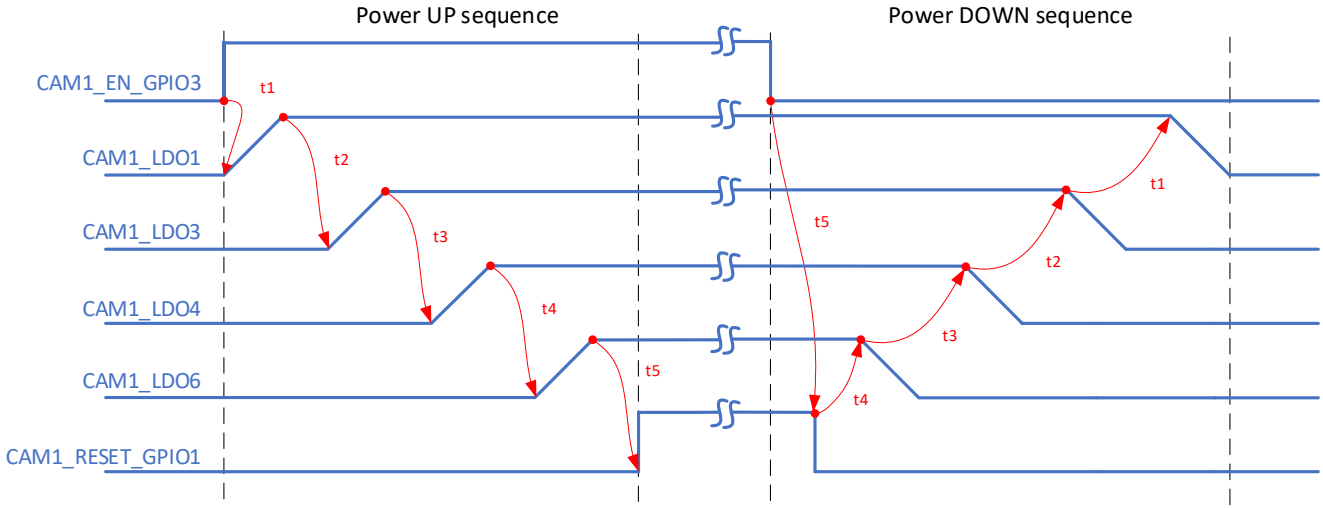

Figure 2: Desired Power – UP and Power – DOWN Sequences for Image sSnsor 1

Sensor 2 Sequence includes: 3 power supply rails and an optional status flag (GPIO2 is used). Optional status flag can be implemented at GPIO2—raised if all voltages are VOUT_OK for mentioned power rails.

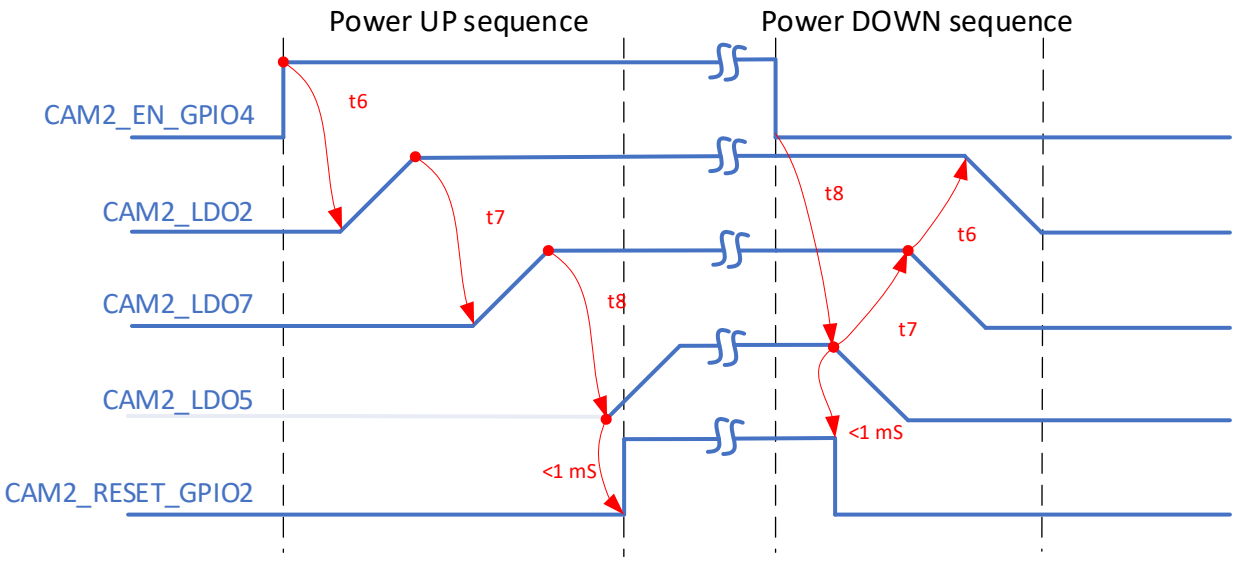

Figure 3: Desired Power – UP and Power – DOWN Sequences for Image Sensor 2

5. Creating the Design

In order to create the design, open Go Configure Software Hub and select the part number SLG51002. A newly created workspace allows users to create the design file for their own project.

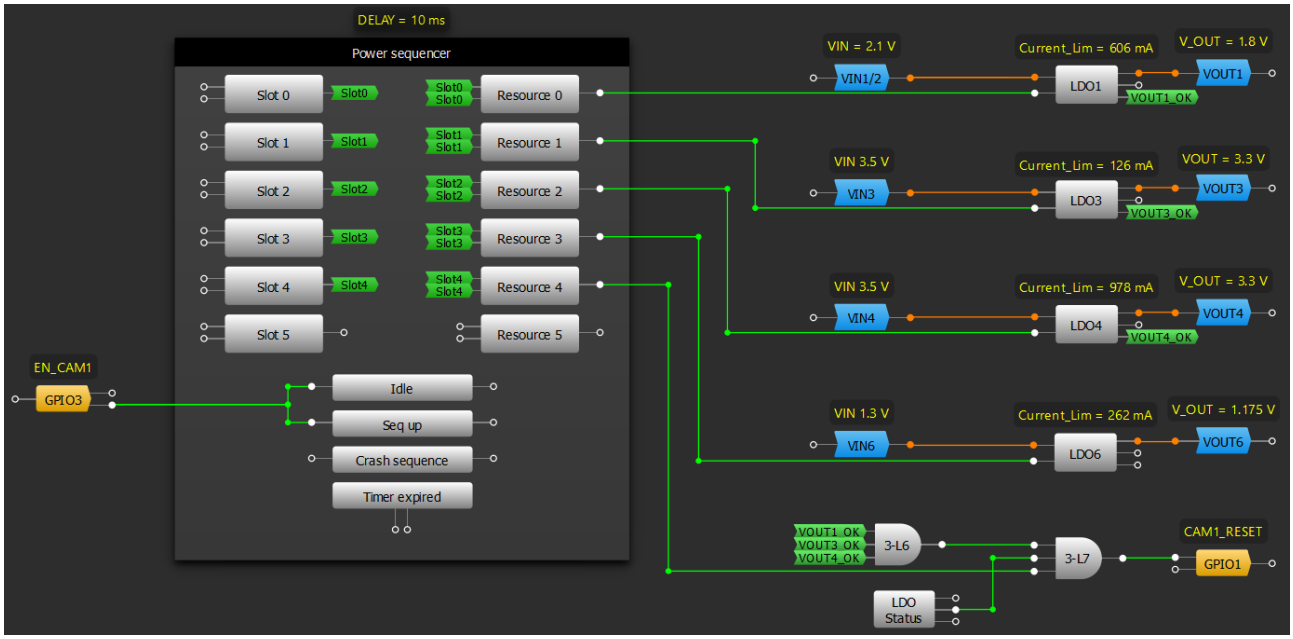

Figure 4: Power Sequencer Design Configuration for Sensor 1

Figure 4 shows internal routing of a chip. Sensor 1 control signal from GPIO3 triggers "Power Sequencer". This unit will perform both Power UP and Power DOWN sequences for Sensor 1. Outputs from Resource 0-4 are connected in the desired order and routed to the LDO regulators. Figure 5 shows preconfigured delay time between LDOs. To open this menu, double-click the Power Sequencer block. In case all LDOs are properly enabled, the LUTs will form the GPIO1 signal that will go to a high level.

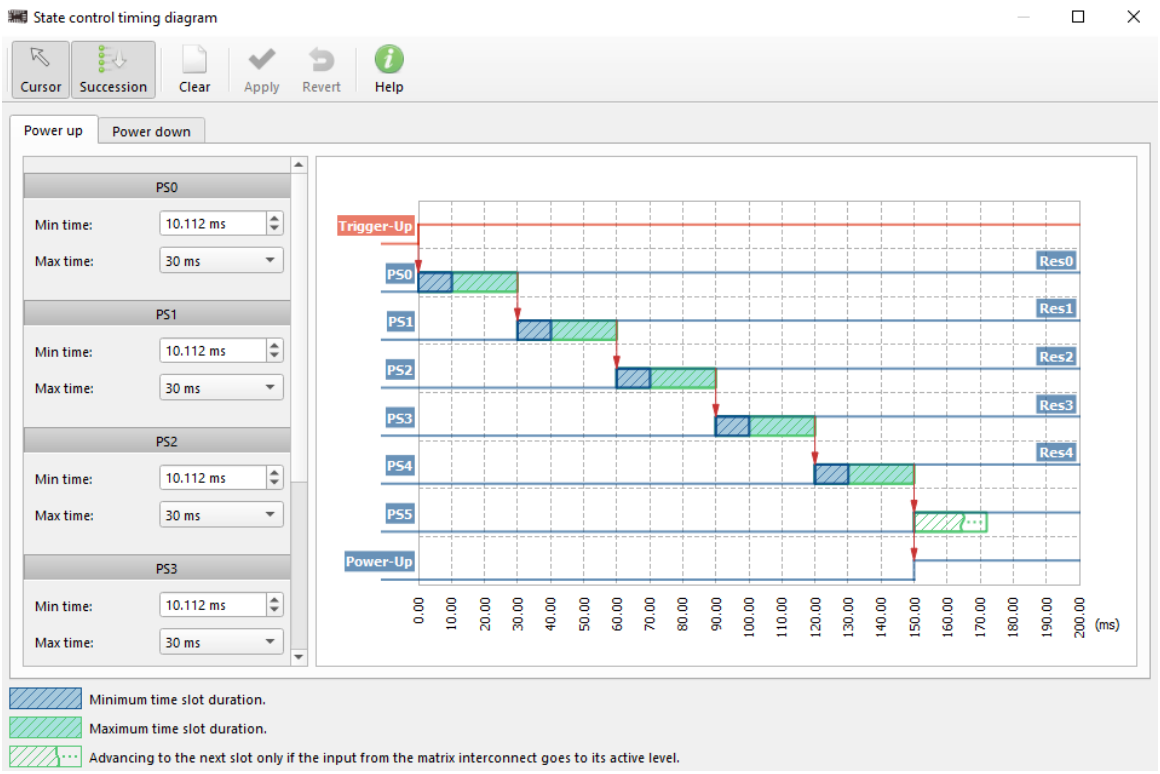

Figure 5: State Control Timing Diagram (Power - Up)

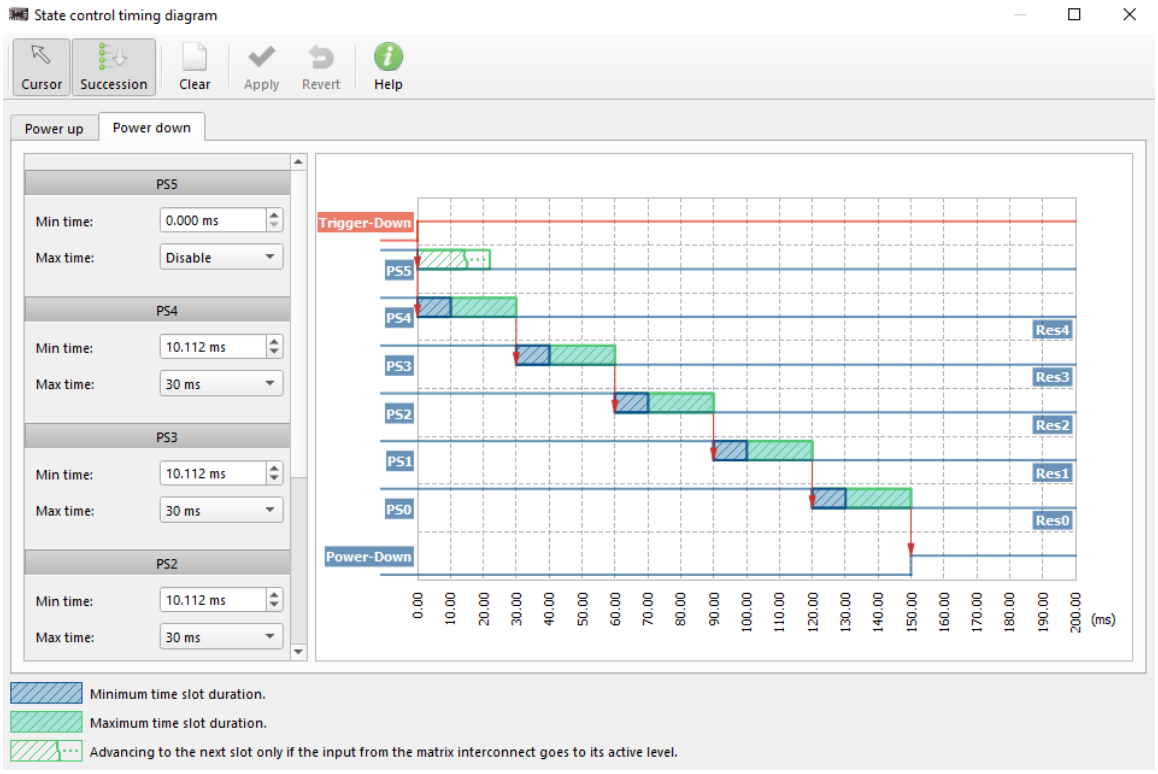

Figure 6: State Control Timing Diagram (Power - Down)

Figure 5 and Figure 6 shows the configuration window of Power Sequencer block. The power slot delay time can be set both for power-UP and power-DOWN. The design is presented configured with a delay of 10 ms per each LDO.

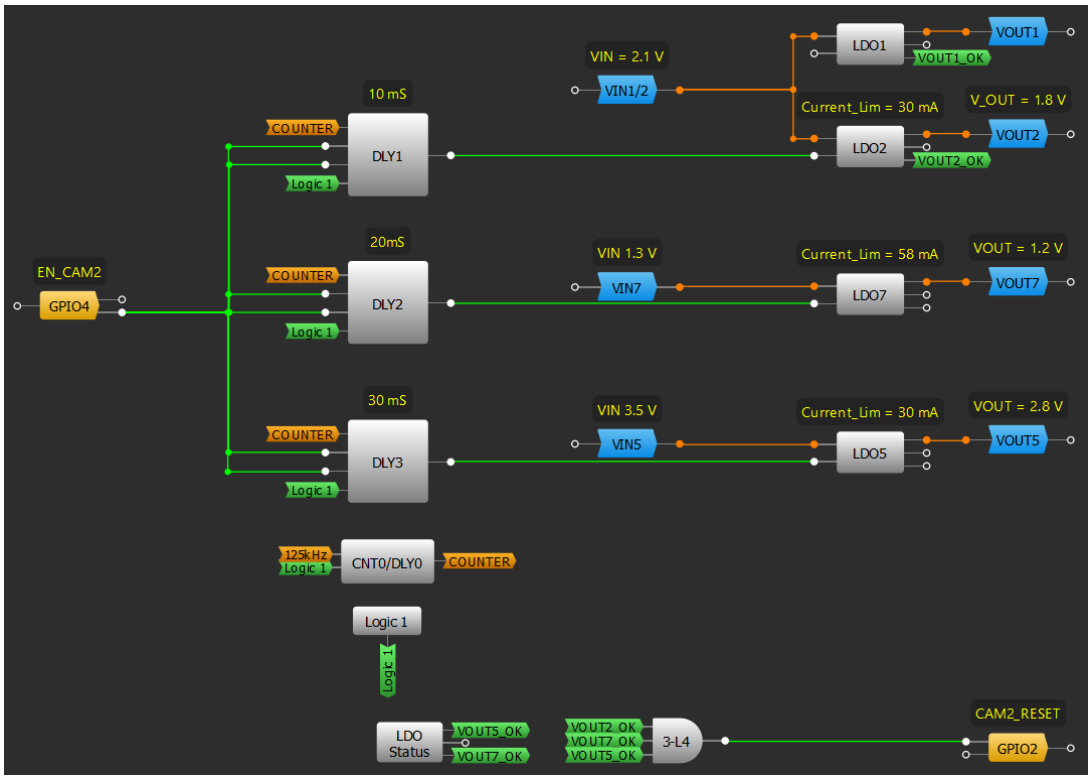

Figure 7: Delay Blocks Design Configuration for Sensor 2

Similar to Figure 4, Figure 6 shows the internal routing of a chip. The Sensor 2 control signal from GPIO4 is routed on DLY1, DLY2 DLY3 blocks. Delay of each block can be set independently both for power on and off. The presented design has delay between rails equals to 10 ms. GPIO2 will raise a flag after all listed LDOs are properly enabled.

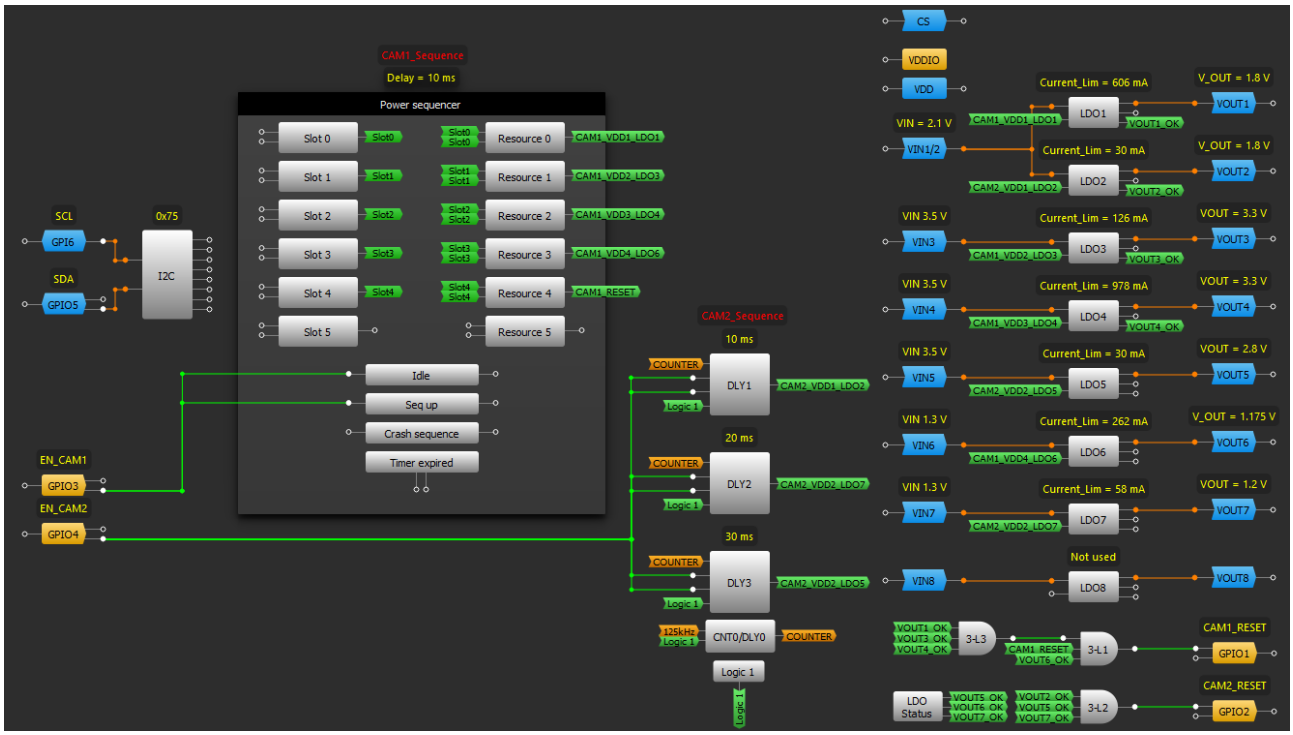

Figure 8: Full Chip Design Configuration

6. Measurement Result

The full chip design shows two independent power sequencers each controlled by an external signal. The resulting waveforms are presented below.

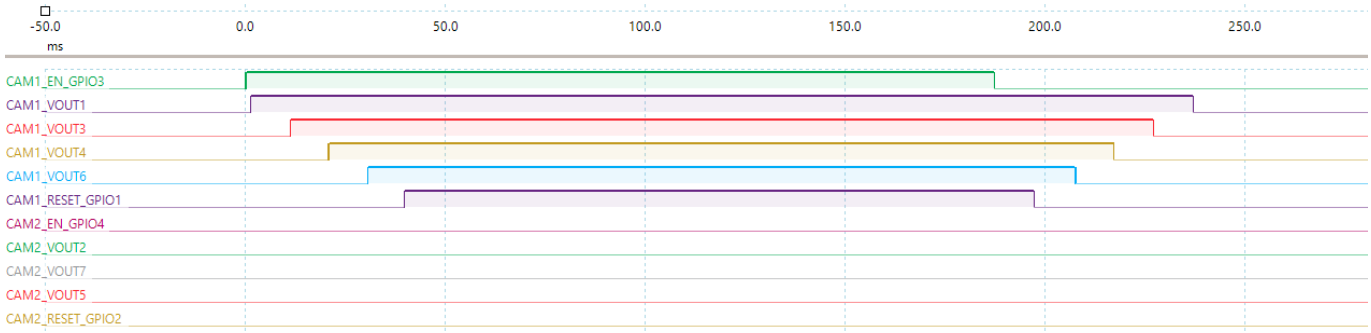

Figure 9: Turn-on and Turn-off only Sensor 1 (CAM1)

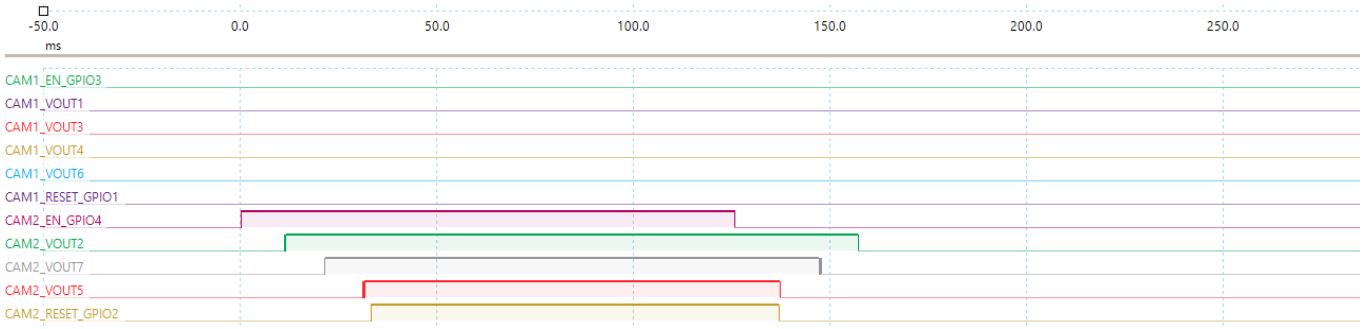

Figure 10: Turn-on and Turn-off only Sensor 2 (CAM2)

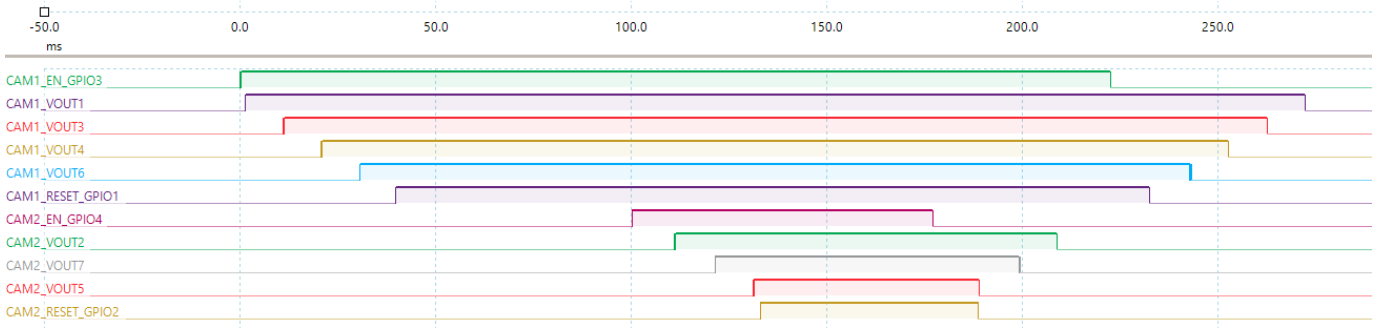

Figure 11: Turn-on Sensor 1 (CAM1) and Sensor 2 (CAM2), Turn-off Sensor 2 (CAM2) and Sensor 1 (CAM1)

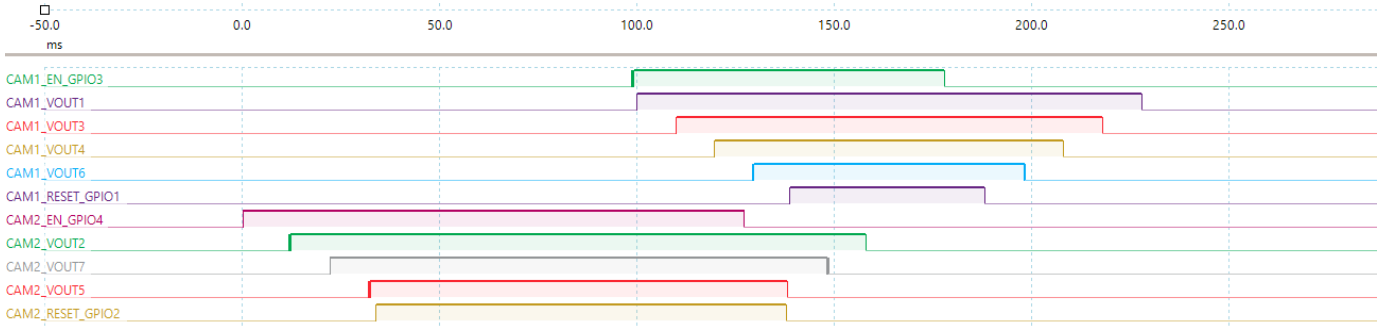

Figure 12: Turn-on Sensor 2 (CAM2) and Sensor 1 (CAM1), Turn-off Sensor 2 (CAM2) and then Sensor 1 (CAM1)

7. Conclusion

This application note presents how complex sequencing with multiple independent scenarios can be handled by the SLG51002, a single chip solution for advanced sensor applications. Using this chip will take up less space on the board, will reduce current consumption and make the final product cheaper.

8. Revision History

Revision	Date	Description
1.00	Feb 20, 2022	Initial release.

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