Power Saving Solenoid Driver
SLG47105

A DC solenoid requires a significant current to activate and pull in its plunger. The current required to hold the plunger is much lower than the current for the pull-in. In a simple transistor driver, the hold current is as high as the activation current, wasting power in the solenoid resistance as heat. This application note shows how to design a smart solenoid driver with current regulation that saves more than 60 percent of the power used in a typical solenoid.

Contents

1. References

For related documents and software, please visit:

https://www.renesas.com/us/en/products/programmable-mixed-signal-asic-ip-products/greenpak-programmable-mixed-signal-products/hvpak

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-342 Power Saving Solenoid Driver.hv, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47105 Datasheet

[6] https://www.electronics-tutorials.ws/io/io_6.html

[7] https://www.sparkfun.com/products/11015

[8] https://www.adafruit.com/product/1512

2. Solenoid Principles

Solenoids are electromechanical actuators with a freely moving magnetic core called a plunger. In general, solenoids consist of a helicoidal coil of wire with a moving core made of iron.

When current is applied through the solenoid coil it generates a magnetic field inside it. This magnetic field generates a force to pull in the plunger. When the magnetic field generates enough force to pull in the plunger, it moves inside the solenoid until it reaches a mechanical stop position. When the plunger is already inside the solenoid, the magnetic field generates force to hold the plunger in place. When the current is removed from the solenoid coil, the plunger will return to its original position, pushed by a mounted spring in the solenoid.

Figure 1 shows the structure of a solenoid.

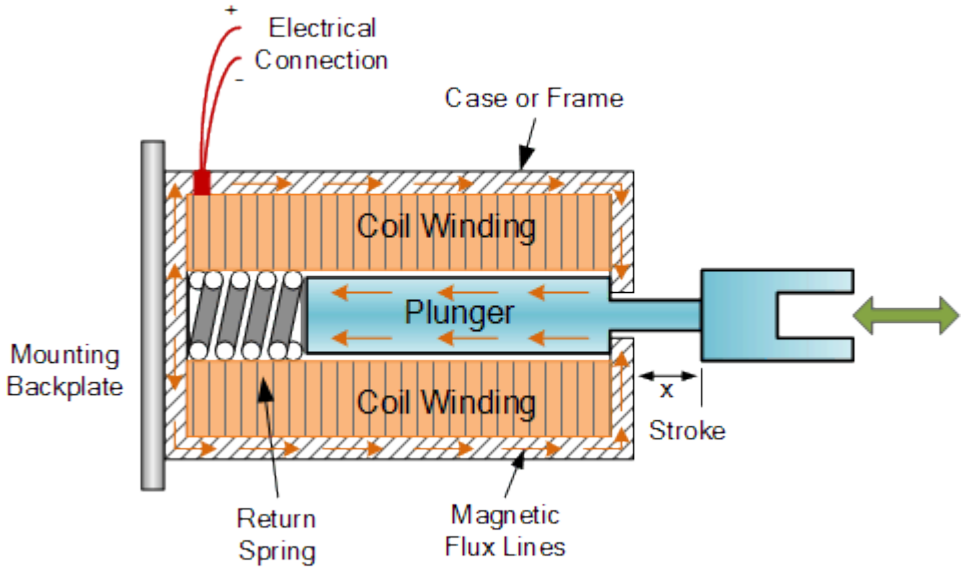


Figure 1. Solenoid structure diagram.

The most common approach to drive a solenoid is to apply the required voltage in the solenoid coil, typically done using a single power transistor configured on the high side or on the low side. The power transistor requires a flywheel diode in parallel with the solenoid as the solenoid coil has a high inductance that will try to

push a current into the transistor. Although this approach is simple and cheap, it is not power efficient. This is because solenoids usually require a significant current to pull in the plunger, but once the plunger is pulled in, it does not require the same amount of current to hold it in place. In this simple driver approach, when the plunger is pulled in and holding the plunger, the extra current applied to the solenoid mainly generates heat through its internal resistance. The power dissipated due to this internal solenoid resistance is given by Equation 1.

$$P_{Dissipated} = Resistance * Current^2 \ (Watts) \quad Equation\ 1$$

An alternative approach which can overcome this issue is to use a current regulated driver to activate and deactivate the solenoid. This driver can apply a peak current value to the solenoid until the plunger is completely pulled in and after that, the driver can reduce the current to a hold value. This strategy greatly reduces the power wasted (released as heat) in the internal solenoid resistance. Another advantage of this approach is the possibility to use a solenoid in a higher voltage range. This means that the driver makes it possible to use a solenoid designed to operate with a lower voltage (for example, 5 V) to operate with a higher power voltage (for example, with a 12 V power supply) without damage.

The following sections will describe the implementation of the current regulated driver for two solenoids with the SLG47105 GreenPAK device.

3. GreenPAK Design Concept

This application note demonstrates how to independently drive two different solenoids using a single SLG47105 device. The SLG47105 device controls the current through the solenoids and informs the user about each solenoid's status (on, off, or in a fault state). A conceptual block diagram showing its internal construction is shown in Figure 2.

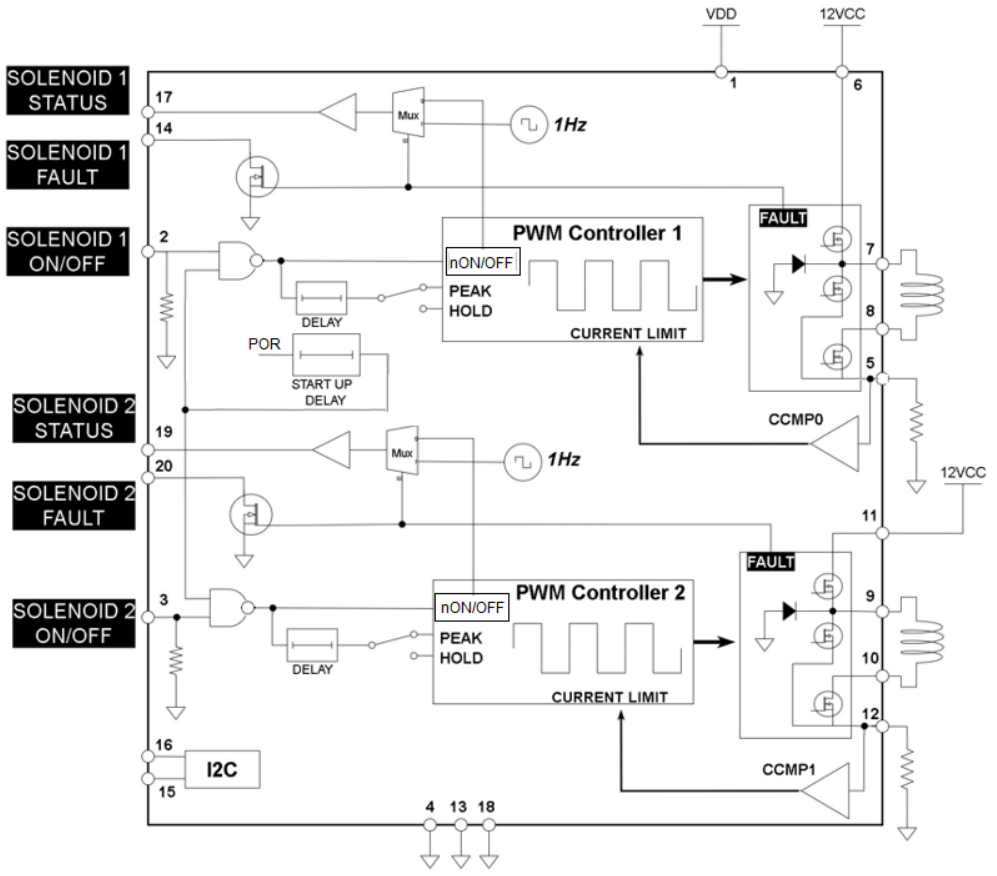


Figure 2. Block diagram of a power-saving solenoid driver with the SLG47105.

The block diagram (Figure 2) shows how the High Voltage Output (HVOUT) blocks are configured along with their connections to the external solenoids. The outputs connected to Pin 7 and Pin 9 are configured as push-pull outputs and the outputs connected to Pin 8 and Pin 10 are configured as open-drain outputs. These open-drain outputs are always remain turned on after startup delay.

Pin 5 is internally connected to the source of the low side N-Mosfets of Pin 8 and the internal current amplifier. Pin 5 is used to detect the solenoid current and compare it with an internal reference (V_{REF}), the V_{REF} values are selected by PWM Controller1. PWM Controller1 generates two V_{REF} values for the CCMP0 comparator, one value for the solenoid peak current and another for the solenoid hold current. The nOn/Off input of PWM Controller1 (Sleep_HV_OUT1 in the design) is activated by the NAND connection to the left. The input of the NAND gate is connected to a startup delay block and Pin 2, which is used as the external interface to turn the solenoid On and Off. The startup delay block is used to guarantee that all internal blocks initialize properly during IC power-up. When PWM controller1 is turned On (output of the NAND gate is LOW) it is configured to regulate the solenoid current at its peak current value. After a delay of 50 milliseconds, the delay block switches the configuration of PWM Controller1 to regulate the solenoid current at its hold current value.

The nOn/Off input (Sleep_HV_OUT1 in the design) of the PWM block is also connected to one of the inputs of a mux. The other MUX input is connected to a square wave signal with a frequency of 1 Hz. The MUX output is controlled by the FAULT signal from the HVOUT block. When the FAULT signal does not indicate any failure, the nOn/Off input is buffered through the MUX to Pin 17 (SOLENOID1 STATUS). When the FAULT signal indicates a failure, the square wave signal is driven on this output. SOLENOID1 STATUS is designed to drive an external LED and indicate the solenoid status to the user. This status can be turned on, turned off, or in a fault state, causing the LED to blink at a frequency equal to the square wave output frequency.

An additional FAULT output is provided as an open-drain output on Pin 14. This output is designed to drive an external device, such as a microcontroller.

As can be seen in Figure 2, the control structure surrounding PWM Controller2 is identical to the control structure of PWM Controller1.

The two FAULT outputs can be connected externally, since they are open-drain outputs, and supply a single FAULT signal to an external device if any of the outputs fail.

There is also an I^2C block in the design that is used to reconfigure peak and hold current setups.

4. Typical Application Circuit

The typical application circuit of this design is shown in Figure 3. Figure 3 shows a schematic of a typical application of driving two different solenoids, identified as SL1 and SL2. The driver is controlled by two push buttons connected to a 5 V power supply. The solenoids are connected to the respective HVOUT outputs. For current measurements, the SLG47105 has two resistors of 0.11 Ω are connected to Pin 5 and Pin 12. The solenoid status outputs are connected to green LEDs and the fault outputs are connected to red LEDs.

In this application note we use two solenoids with completely different specifications. Table 1 shows the main specifications for solenoids SL1 and SL2.

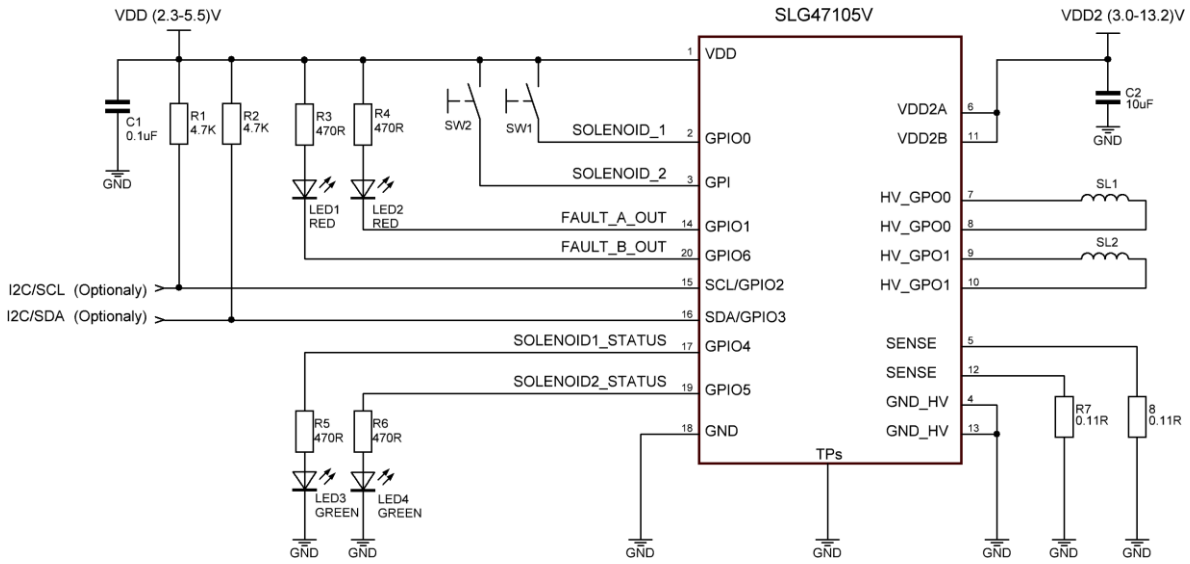


Figure 3. Schematic of the electronic circuit for a typical application

Table 1. Solenoids SL1 and SL2 Specifications and picture.

Part Number	Schematic Reference	Nominal Voltage (Volts)	Nominal Current (mA)	Nominal Internal Coil Resistance (Ω)	Picture
Tomasetto 10r-03 6564	SL1	12	1000	12	
Adafruit 1512	SL2	12	650	18.46	

5. Solenoid Current Setup

The solenoid current will start with a regulated peak current value and after an initial delay, will decrease to a hold current value. The hold current is arbitrarily defined to be 20 percent of the nominal peak current. Based on this definition, it is possible to calculate the power dissipated in the hold current and its respective voltage at the sense resistor. The ideal solenoid current, dissipated power, and voltage at the sense resistor for each solenoid are shown in Table 2. The peak current value equals the solenoid nominal current at the nominal voltage and the hold current value is calculated by multiplying the peak current by 0.2 (20 percent). The peak and hold currents are calculated as the power dissipated over the internal solenoid resistance. The sense resistor is calculated using Ohm's Law through the sense resistor with 0.11 Ω. The nominal coil resistance for SL2 is calculated using its nominal solenoid voltage along with its peak current values.

Table 2. Currents, dissipated power, and sense resistor voltages for an ideal configuration.

Solenoid	Peak Current (mA)	Hold Current (mA)	Nominal Coil Resistance (Ω)	Peak Current Power (mW)	Hold Current Power (mW)	Sense Resistor Voltage - Peak (mV)	Sense Resistor Voltage - Hold (mV)
SL1	1000	200	12	12000	2400	110	22
SL2	650	130	18.46*	7799	312	71.5	14.3

It is important to note that the reference voltage for comparison with the sense resistor voltage in SLG47105 is supplied by an internal 6-bit DAC. The regulated current must be adjusted to the nearest SLG47105 internal reference voltage. Considering this, the following of voltage reference values shown in Table 3 are selected. Table 3 shows the internal voltages and their respective currents. All internal values are 8 times the desired sense resistor voltage because the external voltage is amplified by 8 internally (described in more detail in later sections). The peak and hold current values are calculated using Ohm's Law through the sense resistor.

Table 3. Internal voltage references and their respective currents along with dissipated power.

Solenoid	Internal / External voltage reference for peak current (mV)	Internal / External voltage reference for hold current (mV)	Peak Current (mA)	Hold Current (mA)	Peak Solenoid Power (mW)	Hold Solenoid Power (mW)
SL1	864 / 108	160 / 20	982	182	11784	2184
SL2	2016 / 252	128 / 16	2290.9*	145.5	96.88*	390.8

The values marked with an (*) in Table 3 are calculated values, but these values are theoretical and do not represent the actual values. For SL2, the peak current does not require current regulation because the solenoid's internal resistance will limit the current. Considering this, reference is set up for the maximum current value.

6. GreenPAK Design

The complete internal SLG47105 design is shown in Figure 4. The following sub-sections will explain each part of this design.

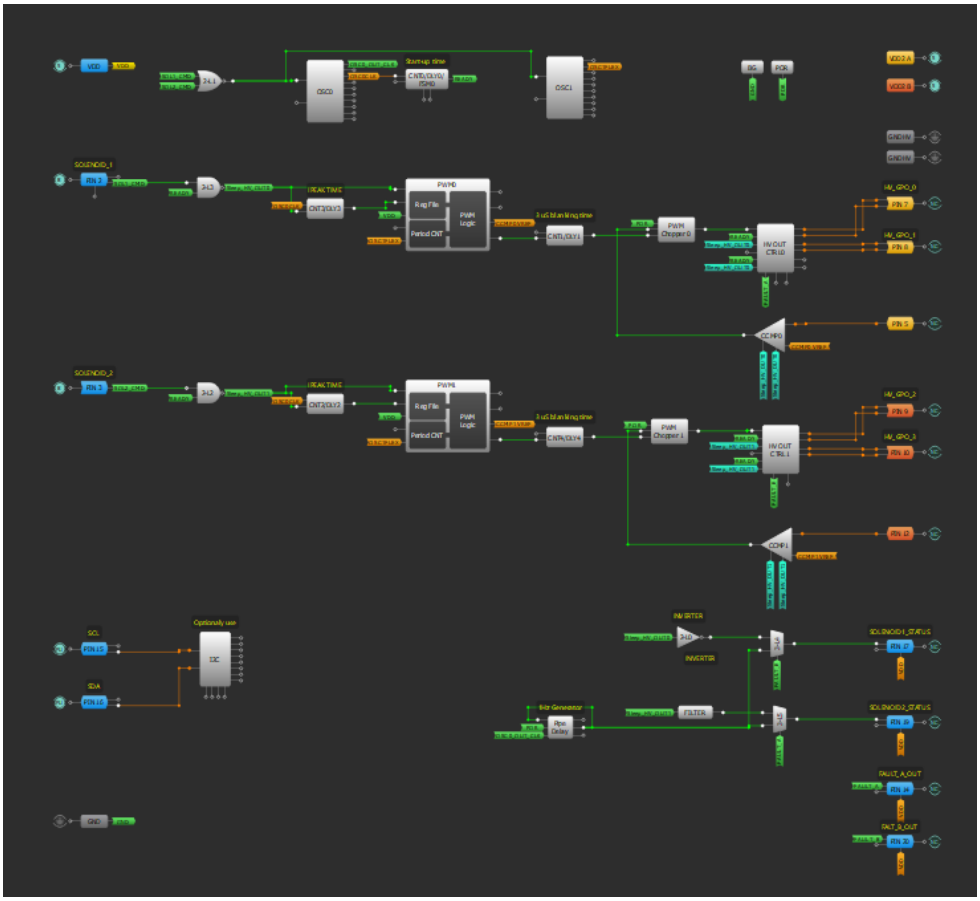


Figure 4. Overview of the complete SLG47105 internal design.

6.1 OSC0

Figure 5 shows the OSC0 block along with its internal configuration. OSC0's frequency is 2.048 KHz. OSC0 is used to generate an $I_{PEAK\ TIME}$ of 50 ms and is used as a low-frequency square wave generator. The default clock frequency of OSC0 is used for the $I_{PEAK\ TIME}$ and a clock frequency of OSC0 /64 is used for the low-frequency square wave generator. This block is turned on when Pin 2 (SOLENOID_1) or Pin 3 (SOLENOID_2) is at a high level.

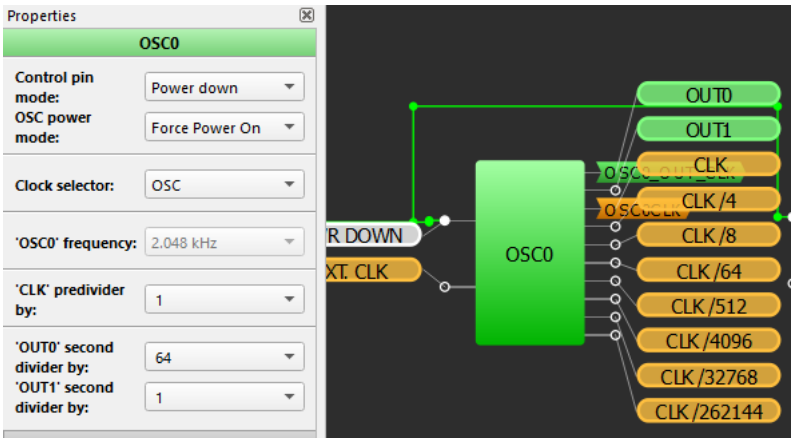


Figure 5. OSC0 block signals and internal configuration.

6.2 OSC1

Figure 6 shows the OSC1 block along with its internal configuration. OSC1's frequency is 25 MHz. OSC1 is used to generate a 3 µs blanking time, a 2 ms start-up time, and to clock the charge pump of the HV out pins. The default clock frequency OSC1 is used for the 3 µs blanking time and a clock frequency of OSC1 /4 is used for the 2 ms start-up time. This block is turned on when Pin2 (SOLENOID_1) or Pin3 (SOLENOID_2) is at a high level.

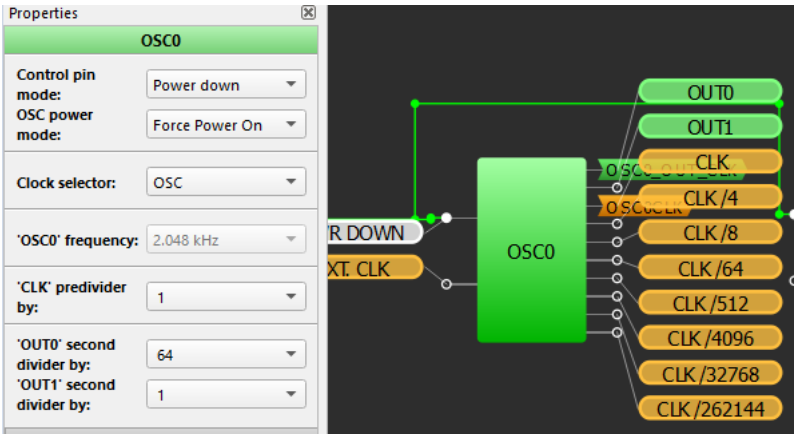


Figure 6. OSC1 block and its internal configuration.

6.3 Start-up Time Delay Block

Figure 7 shows all the blocks used for the start-up time delay functionality. The main functionality of this block is provided by the CNT0/DLY0/FSMO component. Its configuration is shown in Figure 7.CNT0 will delay the POR signal for almost 2 ms, raising a positive edge in the READY signal connection after this initial time has passed. This initial start-up time is required to guarantee that all internal and external components (power supply and capacitors) are ready to properly drive the power outputs and regulate the solenoid current.

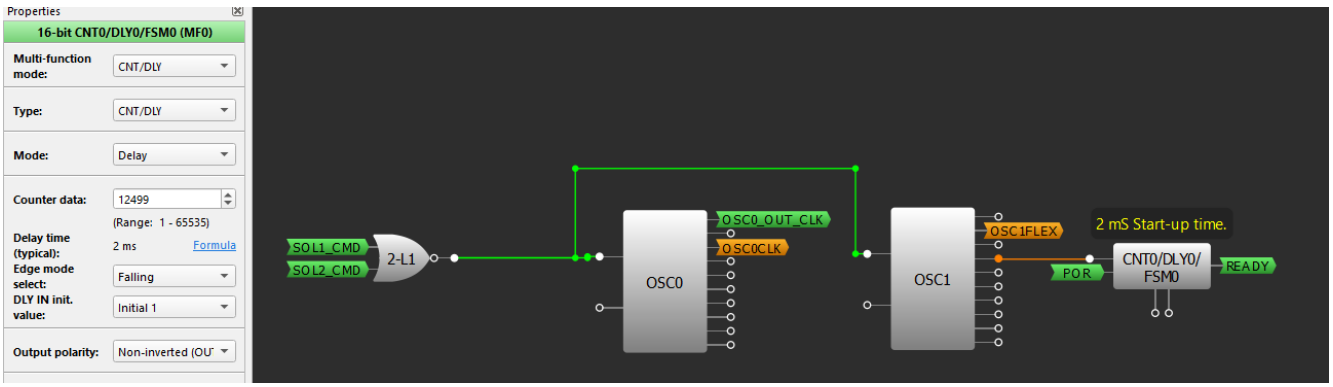


Figure 7. Start-up time delay block. The CNT0/DLY0/FSM0 configuration is shown on the left side.

6.4 HVOUT

Figure 8 shows the HVOUT CTRL0 connections and its internal configuration. HVOUT CTRL0 is the block that controls the SLG47105's internal power transistors. This block controls the power transistors connected to the SL1 solenoid. When Pin 2 (SOLENOID_1) is LOW, the block is de-activated and is activated when a High level is detected on the SOLENOID_1 signal, and the output NAND gate goes Low. This causes HVOUT CTRL0 to wake from Sleep mode. HVOUT CNTR0's OE0 and OE1 connections activate the output HV transistors when a high level is detected on the READY signal. The Pin 8 output is always set to activate the push-pull on the low side by GND connected to input IN1 The push-pull output of Pin 7 is entirely controlled by the PWM Controller block (who's operation will be explained later).

Furthermore, the HVOUT CTRL0 block supplies the FAULT_A signal to indicate when a fault condition occurs on this power output.

The HVOUT CTRL1 block is configured identically to the HVOUT CTRL0 block. Its connections behave similarly and have similar purposes. The HVOUT CTRL1 block is connected to the SL2 solenoid through Pin 9 and Pin 10. This block is connected to the PWM Controller 2 block, and it supplies the FAULT_B signal for any fault in its operation.

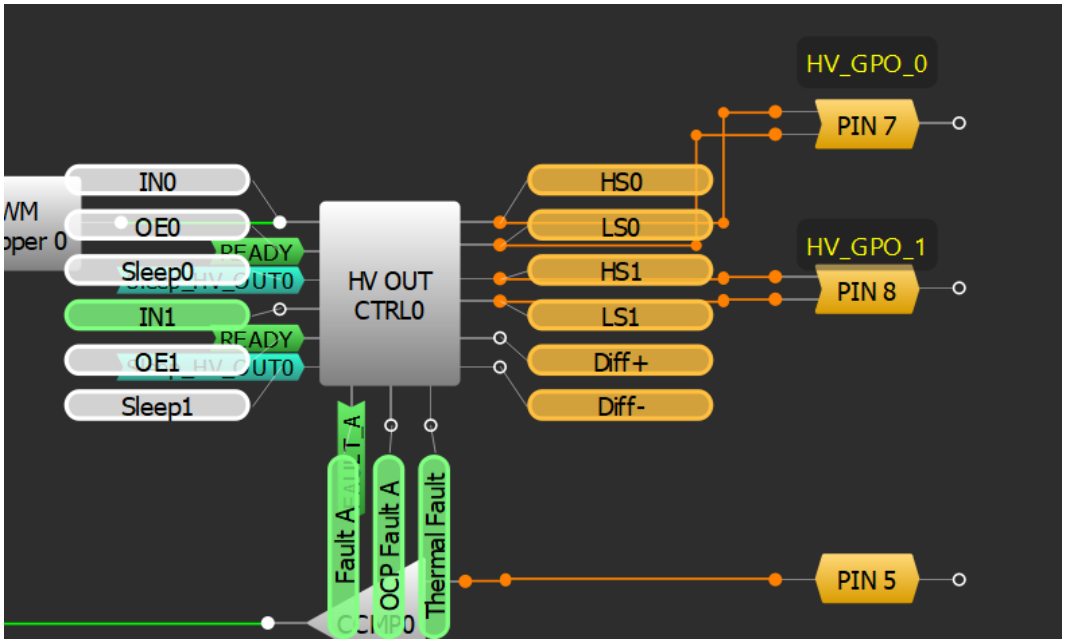


Figure 8. HV OUT CTRL0 block connections and configuration.

6.5 PWM Controller and Current Regulation

Figure 9 shows the PWM Controller 1 block (inside the yellow box). This block is formed by four components: PWM0, PWM Chopper 0, CNT1/DLY1, and CCMP0 (current comparator). These four components create the PWM signal at the output of the PWM chopper for solenoid SL1 corresponding to the signal applied to the current comparator CCMP0 (depending on the current sent through the Sense resistor).

On the left side of Figure 9 is the internal configuration of the PWM0 block. The main function of the PWM0 block is to select the V_{REF} value for CCMP0 from the Register File and generate a positive strobe to create a 3 µs blanking time from CNT/DLY1. The POR (High level) is connected to PWM Chopper 0 to be chopped by the current comparator CCMP0 signal. PWM Chopper 0 has its blanking input connected to CNT1/DLY1. CNT1/DLY1 will generate a short pulse of 3 µs to the blanking time input, allowing a minimum PWM on time. The output of PWM Chopper 0 is connected to the IN0 input of the HV OUT CTRL0 block, controlling the push-pull output of HV GPO0. As seen in Figure 9, the PWM0 block supplies a dynamic reference for the current comparator CCMP0. PWM0 is configured to use the Register File Data in which only two values are used, the first one for the peak current (byte 8), and the second one for the hold current (byte 9). The configuration change happens when a positive edge is raised in the duty cycle clock on the PWM0 input.

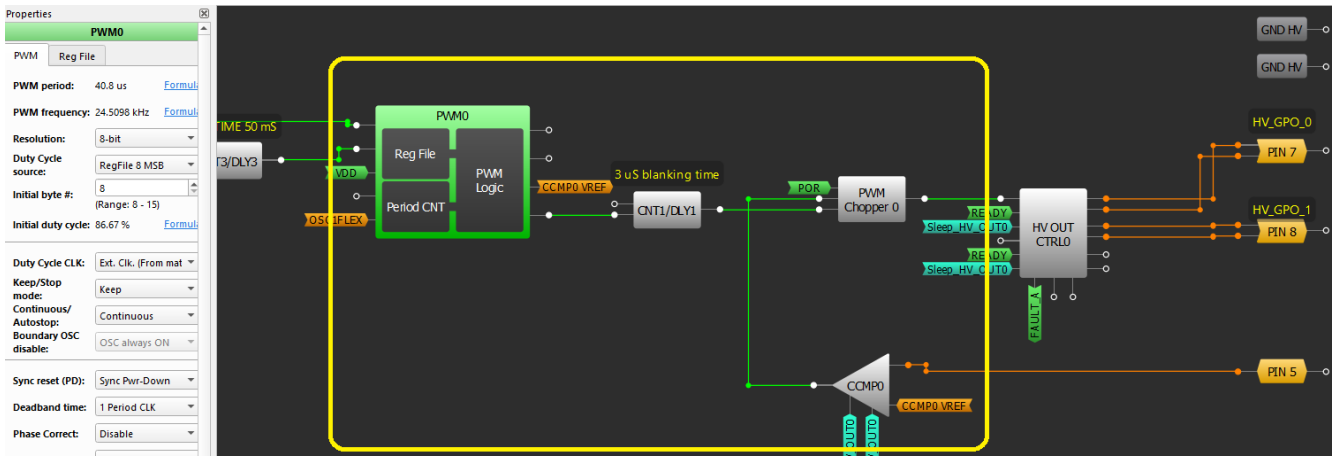


Figure 9. PWM Controller 1 block.

The components connected to the input of the PWM0 block are shown in Figure 10. The components consist of a NAND gate connected to the PWR DOWN input of PWM0 and CNT3/DLY3 connected to the duty cycle clock input of PWM0. The NAND gate is used to enable SL1's On/Off pin signal. The signal from this pin turns on the PWM0 block just after the start-up delay time has passed once the READY signal is at a high level. The output of the NAND port turns on the PWM0 block after a delay of 50 ms set by the $I_{PEAK\ TIME}$ delay component. The delay of this block controls how long the PWM will regulate the solenoid current while at its peak value. After this time, a positive edge is generated on the duty cycle clock input of PWM0, and the reference register byte is increased, changing the reference voltage for current comparator CCMP0. When SOL1_CMD is at a high level, the PWM0 and the HV OUT CTRL0 blocks are turned on (Sleep_HV_OUT0 is Low Level) and when SOL1_CMD is at a low level, the PWM0 and HV OUT CTRL0 blocks are immediately turned off (Sleep_HV_OUT0 is High Level).

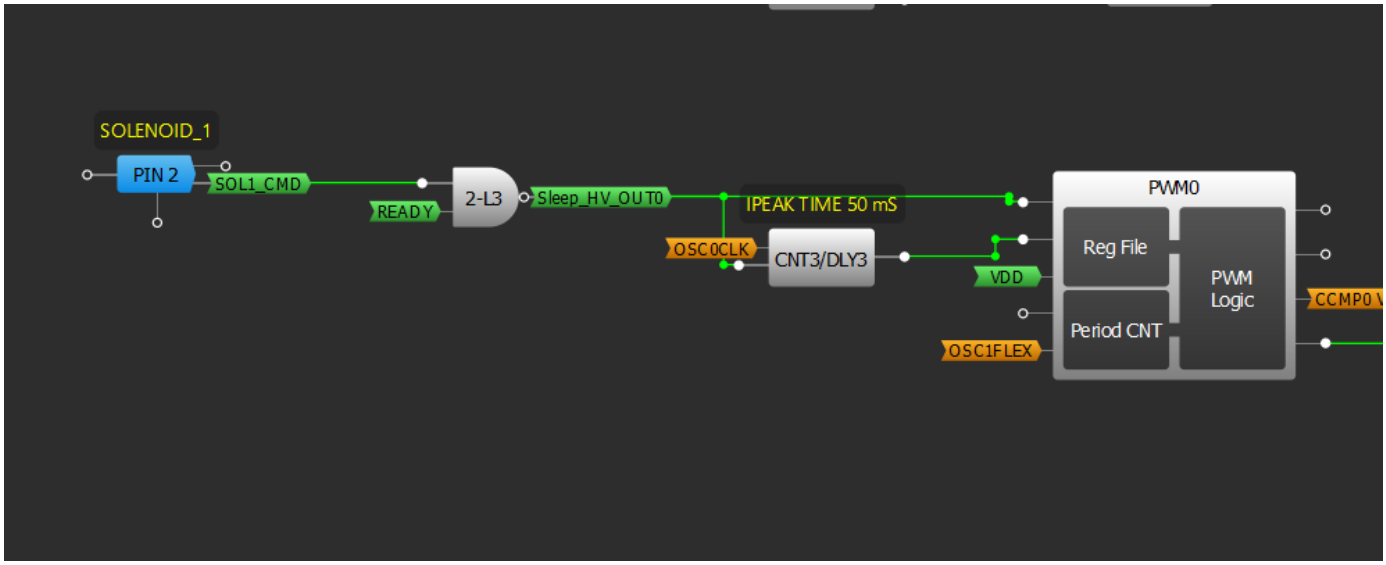


Figure 10. Input connections for the PWM0 component.

Current comparator CCMP0 is used to regulate the solenoid current, and the configuration of this component is shown in Figure 11. The current comparator internally amplifies the voltage in Pin 5 by 8x (see IN+ gain in Figure 11). This multiplier factor must be considered when setting the reference voltages for comparison. The component is turned on by the Sleep_HV_OUT0 signal and it is always on when Pin 2 (SOLENOID_1) and READY are High level. The IN- input of CCMP0 is connected to the PWM0 CCMP0 VREF output. This output will supply the voltage references of defined by byte 8 and byte 9 of the Register File Data. The Register File Data is shown in Figure 12.

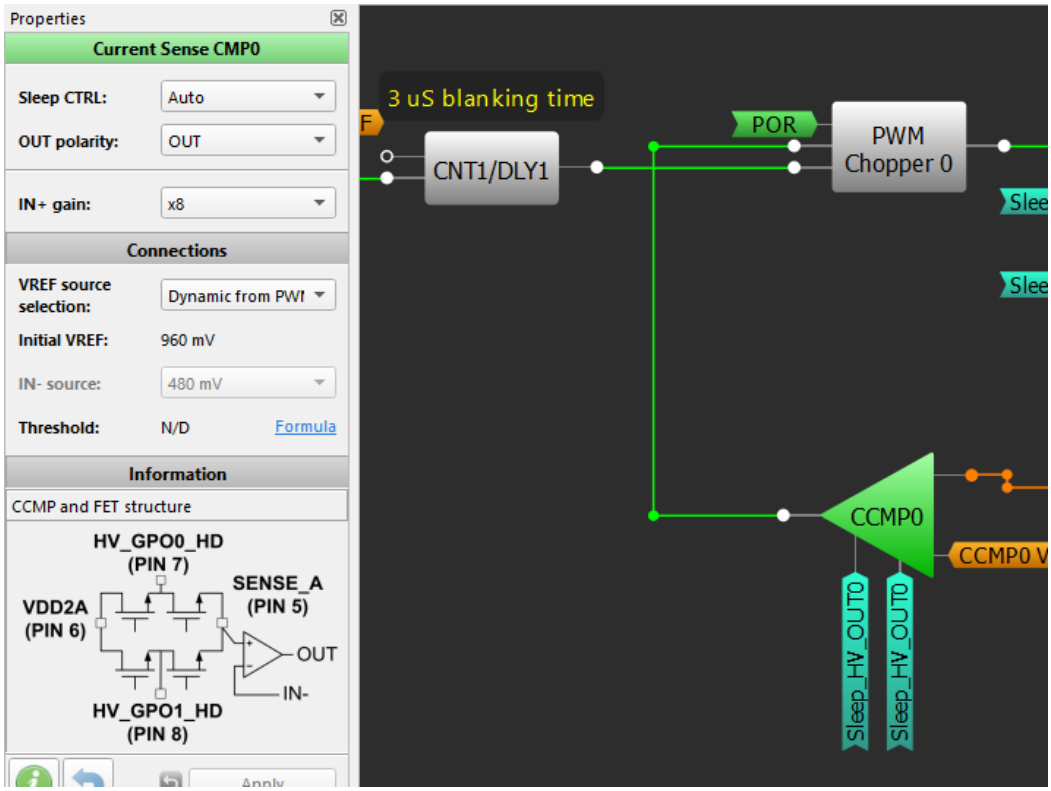
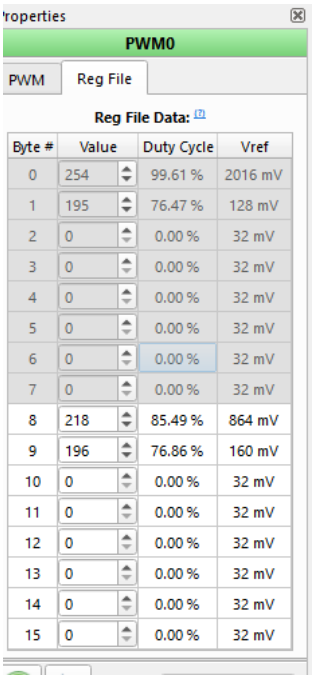


Figure 11. CCMP0 configuration and connection to PWM Chopper 0.



Byte #	Value	Duty Cycle	Vref
0	254	99.61 %	2016 mV
1	195	76.47 %	128 mV
2	0	0.00 %	32 mV
3	0	0.00 %	32 mV
4	0	0.00 %	32 mV
5	0	0.00 %	32 mV
6	0	0.00 %	32 mV
7	0	0.00 %	32 mV
8	218	85.49 %	864 mV
9	196	76.86 %	160 mV
10	0	0.00 %	32 mV
11	0	0.00 %	32 mV
12	0	0.00 %	32 mV
13	0	0.00 %	32 mV
14	0	0.00 %	32 mV
15	0	0.00 %	32 mV

Figure 12. Register Data File configuration.

The structure of PWM Controller 2 is similar to the structure of PWM Controller 1. The register bytes used for current regulation are located at byte 0 and byte 1. The components of PWM Controller 2 are shown in Figure 13. It is important to note that the solenoid current settings are different for PWM Controller 1 and PWM Controller 2. The current regulation is independent, as are the PWM values.

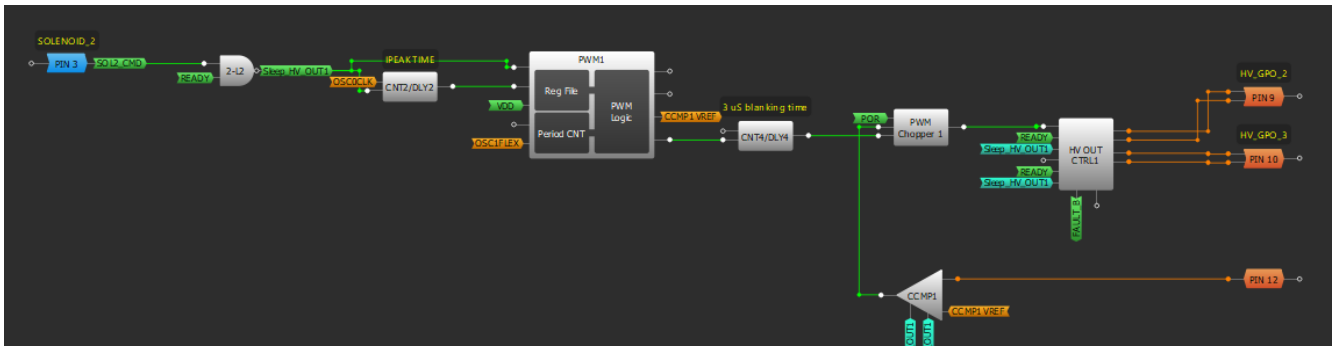


Figure 13. PWM Controller 2 structure and connections.

6.6 Solenoid Status Indication and Fault Signal

Figure 14 shows the components used for solenoid status indication and the fault output signal. The Pipe Delay component is used to generate the 1 Hz square wave signal. This component divides the OSC0 output clock to generate this square wave signal. The FAULT_A and FAULT_B signals are the fault signals for their respective solenoids SL1 and SL2. These signals are registered to avoid glitches in the output pins. Their respective pins are configured as open-drain outputs while output pins connected to the solenoid status indicators are configured as push-pull outputs.

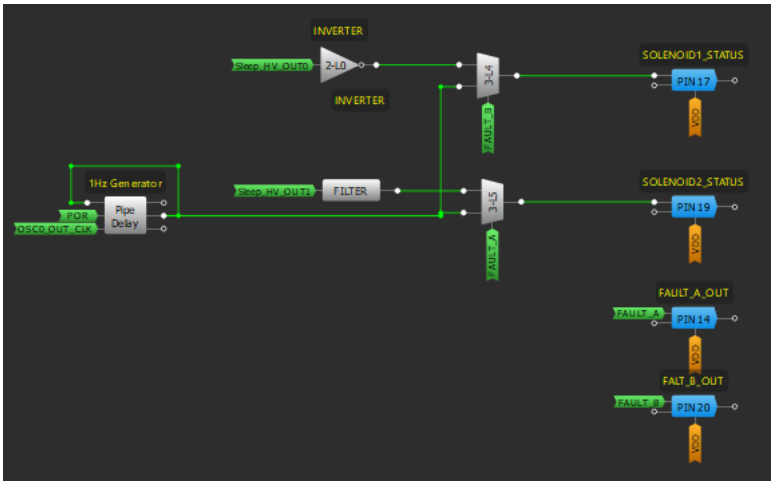


Figure 14. Solenoid status indication and fault output signal.

6.7 I²C

I²C remains available in the design, which makes it possible to set PWM values via an external device. There are no internal signals connected to the I²C block, just the respective external pins connected to it.

7. Verification Prototype

Figure 15 shows a picture of the verification prototype built to test this design. The prototype is assembled on a breadboard using the SLG47105 DIP Board.

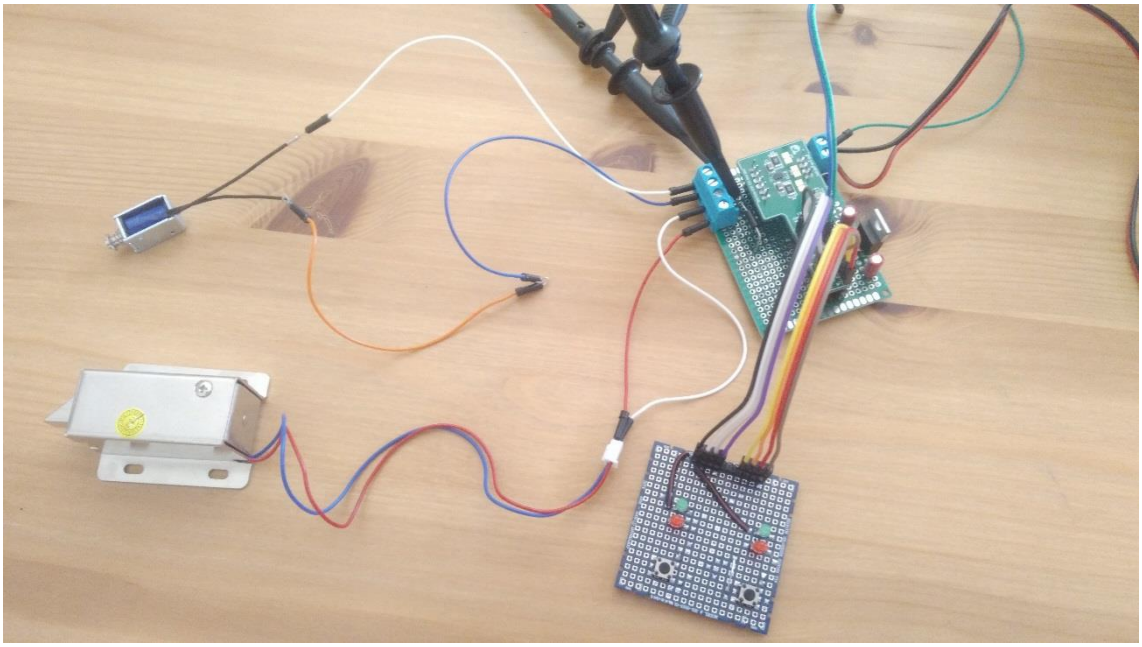


Figure 15. Verification prototype.

8. Tests

8.1 Test Procedures

The prototype testing procedure consists of pressing the respective solenoid pushbutton and then verifying the operation of the following components:

- Plunger movement and position: The solenoid plunger must be pulled-in when it is activated by the driver. The driver must hold the plunger in the pulled-in position while it is active. The driver must release the plunger from its pulled-in position and return it to the de-energized position when the driver is deactivated.
- LED indicators: When the solenoid is deactivated its green LED indicator must turn off. When it is activated its green LED indicator must be turned on. When the respective solenoid output has a fault condition (such as a short circuit) the solenoid green indicator must blink at a frequency of 1 Hz. The red fault LED indicator must be on when there is a fault condition and off otherwise.
- Current measurement: the maximum peak current and hold current must be measured and should comply with the specified values (see Table 3 in section 5).

To measure the current through the solenoids we used a SOGLENT Current Probe CP6000 and RIGOL MSO1104 oscilloscope.

8.2 Test Results for Solenoid SL1

All waveforms were done at V_{DD2} = 12 V.

Figure 16 shows the measured current when activating solenoid S1. The figure shows the initial peak current through the solenoid and the decrease in current until it reaches the hold value after 50 ms.

Channel 1 (yellow/1st line) – PIN# 2 (SOLENOID_1)

Channel 2 (light blue/2nd line) – $I_{PEAKTIME}$ of 50 ms (DLY3 out), Internal signal

Channel 3 (magenta/3rd line) – Solenoid 1 current, V_{REF} of CCMP0 dynamically changing.

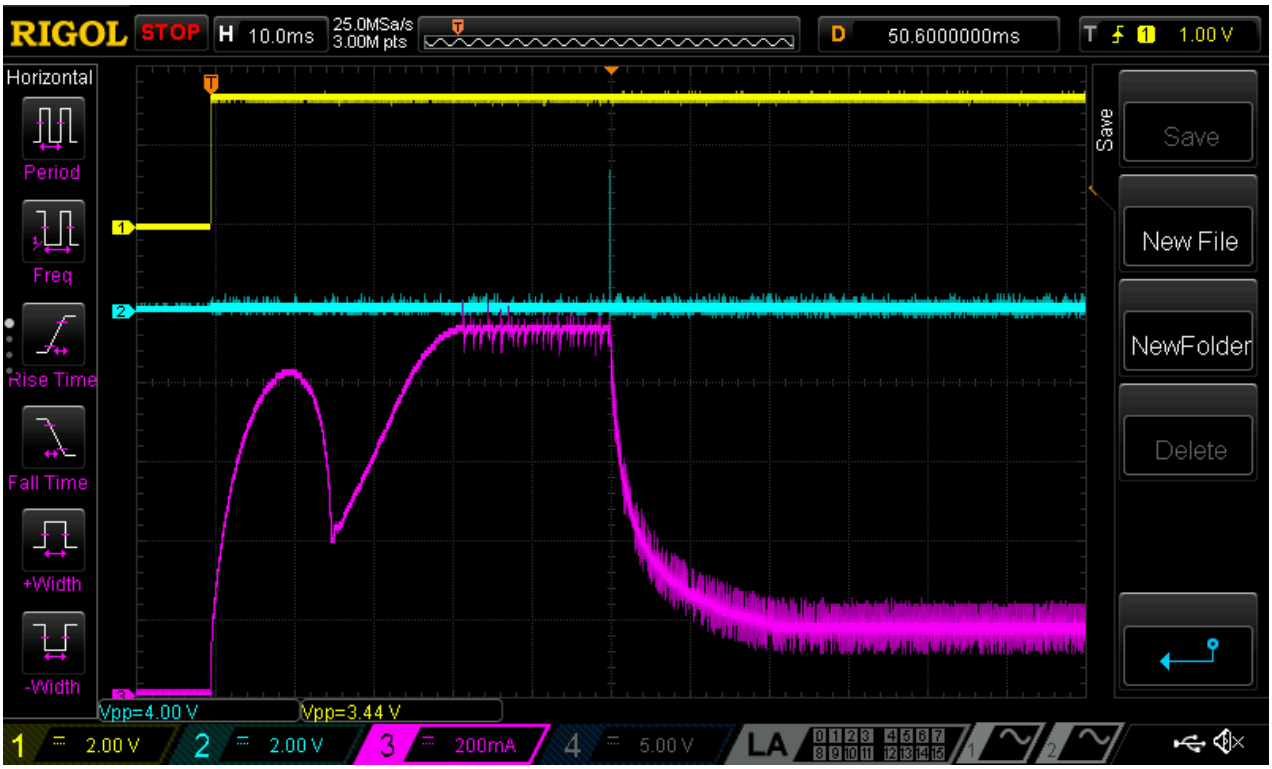


Figure 16. Solenoid SL1 current measurement.

Figure 17 shows the states of the three main periods of time for SL1.

Channel 1 (yellow/1st line) – PIN# 2 (SOLENOID_1)

Channel 2 (light blue/2nd line) – $I_{PEAKTIME}$ 50 ms (DLY3 out), Internal signal

Channel 3 (magenta/3rd line) –Solenoid 1 current, V_{REF} of CCMP0 dynamically changing. T1, T2, and T3

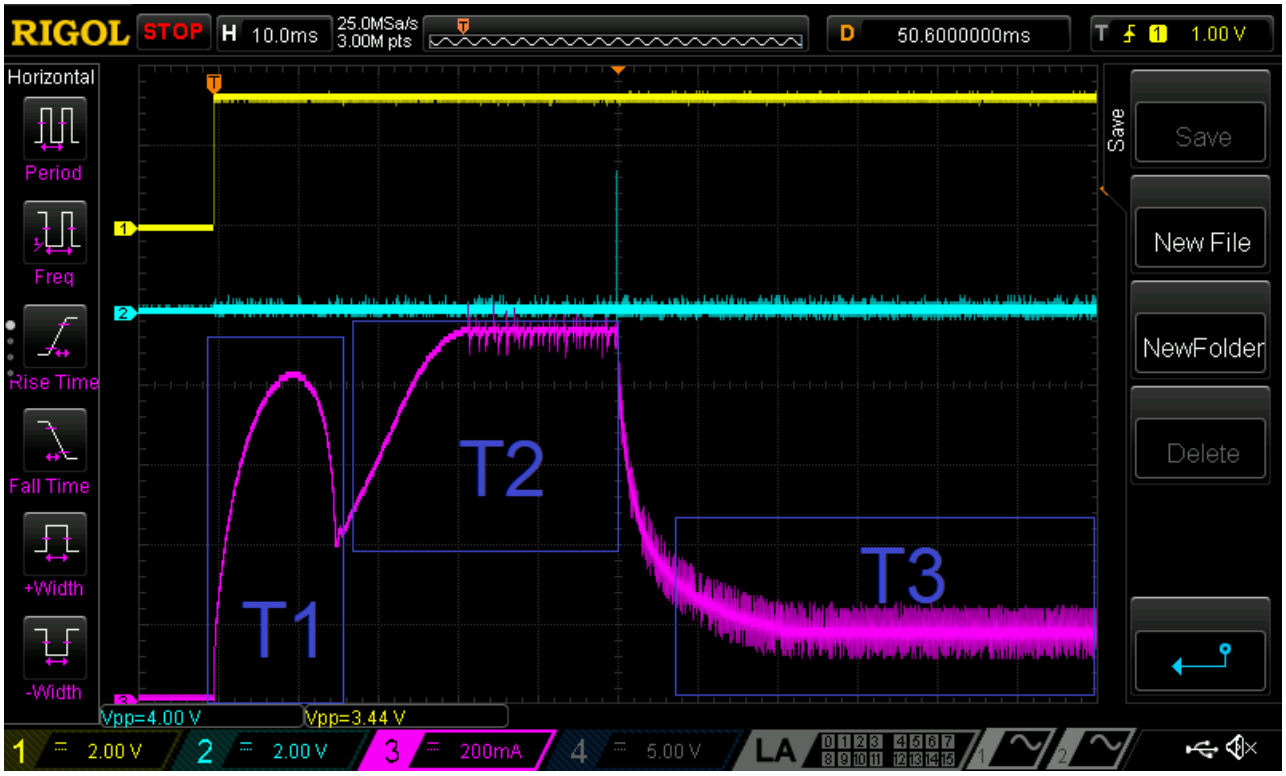


Figure 17. Main of Solenoid SL1 states.

T1 – The period where the plunger of solenoid SL1 is moving.

T2 – After the plunger reaches the mechanical stop, the current SL1 increases to the peak SL1 current value (982 mA), then the SLG47105 stabilizes the peak current.

T3 – The state during which the SL1 current (182 mA) stabilizes to the hold current after 50 ms, Channel 2 (light blue/2nd line) shows a positive impulse indicating that the V_{REF} value of CCMP0 changes.

Figure 18 shows the PWM generated in Pin 7 (HV_GPO0) during the activation of solenoid SL1 (peak current setting). Figure 18 displays the reduction of the PWM duty cycle over time.

Channel 2 (light blue/1st line) – Blanking time of 3 µs (DLY1 out), Internal signal

Channel 3 (magenta/2nd line) –Solenoid 1 current, V_{REF} of CCMP0 = 864 mV

Channel 4 (blue/3rd line) – Pin 7 (HV_GPO0), PWM out for Solenoid 1

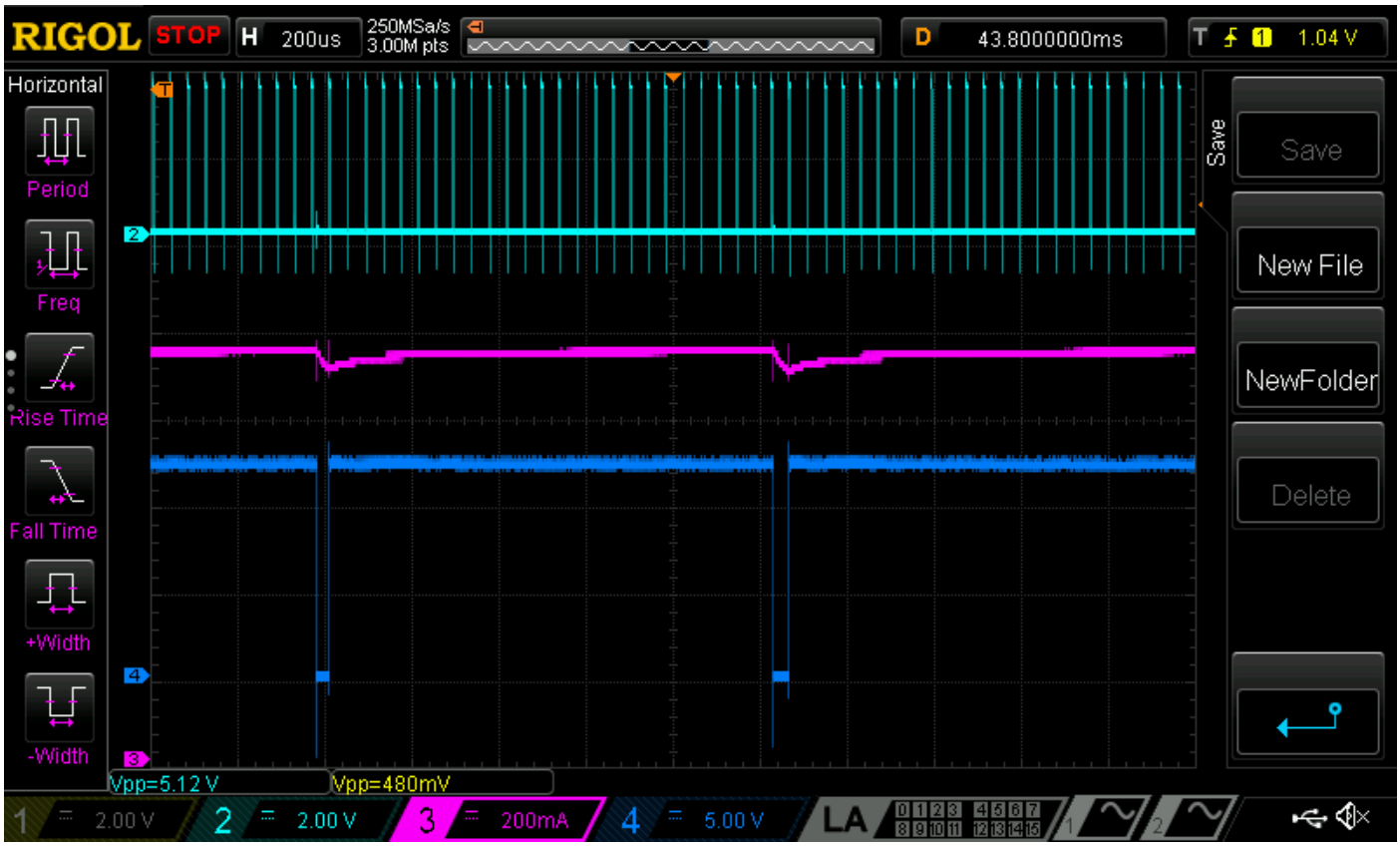


Figure 18. Solenoid SL1 peak current regulation, PWM applied.

Figure 19 shows the PWM applied to the solenoid SL1 when it is in its hold current regulation state. In this waveform the SL1 current is increasing only during blanking time, therefore the PWM signal is a copy from Blanking time signal. To see the current regulation process please see Figure 20.

Channel 2 (light blue/1st line) – Blanking Time of 3 µs (DLY1 out), Internal signal

Channel 3 (magenta/2nd line) –Solenoid 1 current, V_{REF} of CCMP0 = 160 mV

Channel 4 (blue/3rd line) – Pin 7 (HV_GPO0), PWM out for Solenoid 1

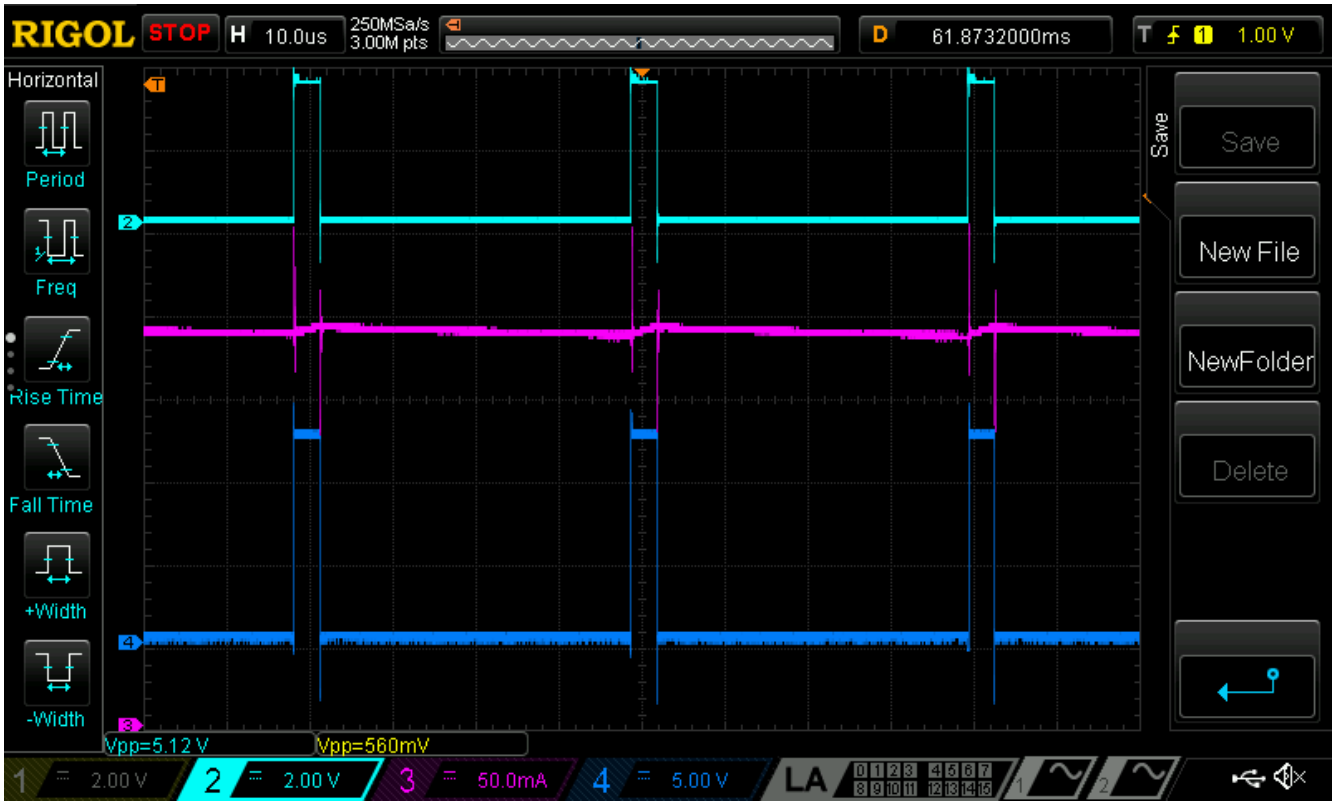


Figure 19. Solenoid S1 PWM generated during hold current regulation.

Figure 20 shows the current regulation process with another V_{REF} CCMP0 value. Until blanking time (3 µs), Pin 7 (HV_GPO0) is at a High level, then the current through the solenoid is increased to the I_{TRIP} value. The I_{TRIP} value for V_{REF} CCMP0 = 448 mV and the sense resistor R sense = 0.11 Ω is:

$$I\ trip\ = \frac{\text{U sense}}{\text{R sense}}$$

$$I\ trip\ = \frac{\text{Vref}\ /8}{0.11}$$

$$I\ trip\ = \frac{448\text{mV}/8}{0.11\ \text{Ohm}} = \frac{56\text{mV}}{0.11\ \text{Ohm}} = 509\ mA$$

Channel 3 of Figure 20 shows the PWM signal for constant current 0.5 A through the solenoid.

Channel 1 (light blue/1st line) – Blanking TIME 3 µs (DLY1 out), Internal signal

Channel 2 (magenta/2nd line) –Solenoid 1 current, V_{REF} CCMP0 = 448 mV.

Channel 3 (blue/3rd line) – Pin 7 (HV_GPO0), PWM out for the Solenoid

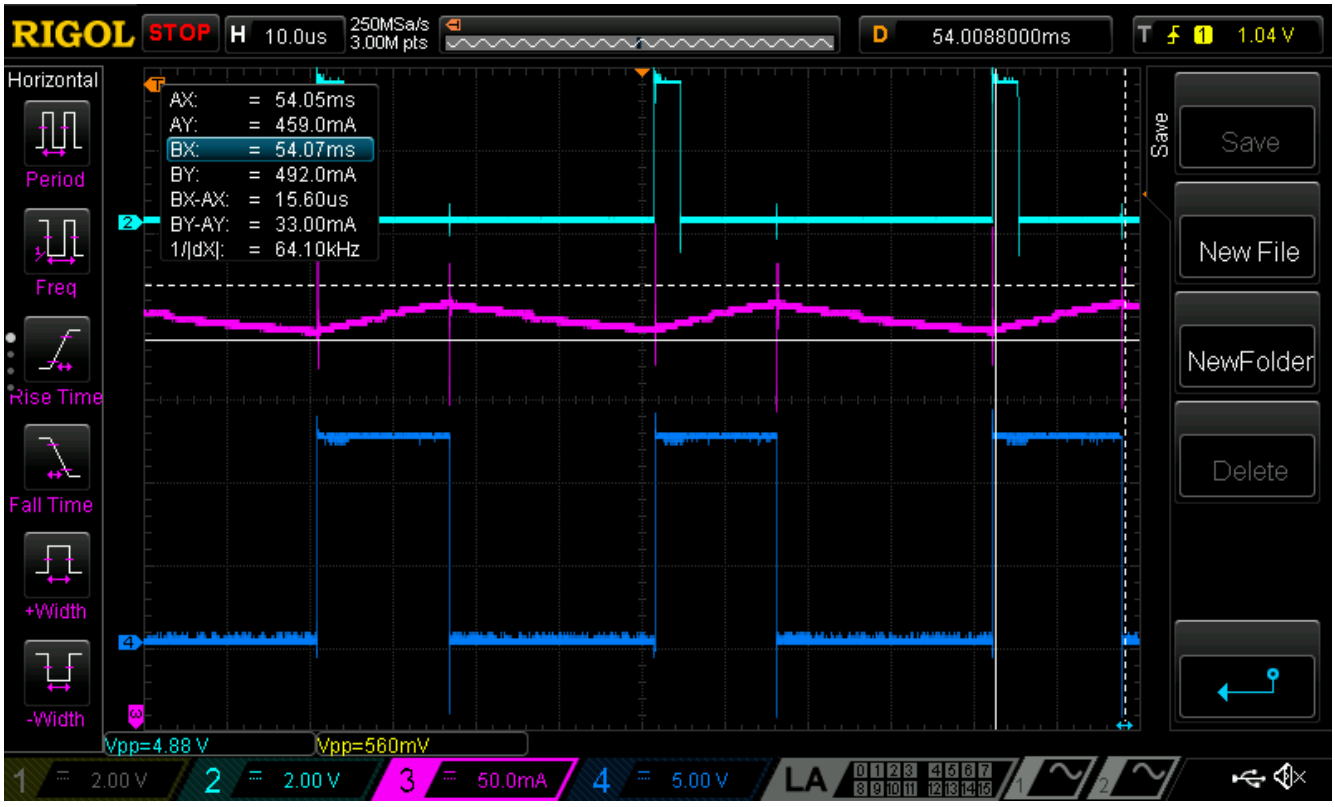


Figure 20. Current regulation process.

8.3 Summary of Current Measurements

Table 4 shows a comparison between the calculated and measured peak and hold currents for each solenoid.

Table 4. Comparison of measured and calculated currents. All current values are in mA.

Sol.	Calculated peak current (mA)	Measured peak current (mA)	Peak current Error (mA)	Peak current Error (%)	Calculated hold current	Measured hold current	Hold current Error	Hold current Error (%)
SL1	982	930	50	-5.0%	182	160	22	-12.0%
SL2	650	665	15	+2.31%	145.5	167	21.5	+14.8%

Table 5 shows a comparison between the calculated and measured (considering the measured current and nominal resistance) power of each solenoid.

Table 5. Comparison of measured and calculated power dissipations. All power values are in mW

Sol.	Calculated peak power (mW)	Measured peak power (mW)	Peak power difference (mW / %)	Calculated hold power (mW)	Measured hold power (mW)	Hold power difference (mW / %)
SL1	11784	11160	-624 / -5.3%	2184	1920	1264 / -12.0%
SL2	7799	8163	+364 / +4.67%	390.8	514.8	+124 / +31.7%

Table 6 shows the calculated and measured power savings achieved with the power saving solenoid driver. The nominal power consumption is considered for this calculation.

Table 6. Comparison of calculated and measured power saving

Solenoid	Nominal Power (mW)	Calculated power saving (mW / %)	Measured power saving (mW / %)	Power saving difference (mW / %)
SL1	12000	9816 / 82.0%	10080 / 84.0%	264 / 2%
SL2	7800	7409.2 / 94.99%	7285.2 / 93.4%	-124 / -1.59%

9. Conclusion

This application note describes the implementation of a dual power-saving solenoid driver. It illustrates that huge power savings can be obtained by using this design, depending on the hold current to peak current ratio. The higher the ratio, the higher the power savings. However, it is important to note that the ratio depends on the application. Reducing the hold current will reduce the force needed to keep the plunger pulled in the solenoid.

It is important to consider the results shown in the comparison between the calculated currents and the actual measured currents in the tested prototype. The hold current has a significant error, > 10 %, for both solenoids. From the analysis of the absolute current and percentage current errors it is plausible that there are side effects to the gain and offset errors.

As shown in Table 4, the absolute error increases depending on the current setpoint, which is a sign of gain error. This gain error can be due to limitations in the sense resistor accuracy. Meanwhile, the increase in the percentage error when the current is reduced to the hold value indicates an offset error. This implies an almost constant error, which will be more relevant at lower values. Meaning that the offset error may be more relevant than the gain error.

Unfortunately, is not possible to identify the source of this error. Some of the hypothetical reasons for the error could be due to error in the SLG47105 current comparator or an error in the current measurement made with the oscilloscope.

10. Revision History

Revision	Date	Description
1.00	Sep 27, 2022	Initial release
1.01	Jul 24, 2024	Updated design

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