Application Note

Digital Stereo Volume and Balance Controller with Mute Function

AN-CM-331

Abstract

This application note describes how to design and build a digital stereo volume and balance controller with mute function.

The application note comes complete with a design file that can be found in the Reference section.

Digital Stereo Volume and Balance Controller with Mute Function

Contents

Figures

Tables

1 Terms and Definitions

GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input / Output
OPAMP	Operational Amplifier
OSC	Oscillator
VREF	Voltage Reference

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/products/greenpak/analog-greenpaks

Download our free GreenPAK Designer software Ref. [1] to open the .aap file and view the proposed circuit design. Use the GreenPAK development tools Ref. [3] to freeze the design into your own customized IC in a matter of minutes.

Find out more in complete library of application notes Ref. [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download, and User Guide
[2] AN-CM-331 Digital Stereo Volume and Balance Controller.aap
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47004 Datasheet
[6] AN-CM-320 Potentiometer Controlled by an Encoder

3 Introduction

This application note describes how to design and build a digital stereo volume and balance controller with mute function.

It is possible to design a fully functional cost-effective digital stereo volume control circuit using only one SLG47004 IC with a very low external components count. Figure 1 shows a simplified schematic diagram of such a device. For the full circuit diagram refer to Figure 2. The device has the following features:

- Three push-button interface
- 0 to -60 dB volume regulation (can be changed in the design)
- ±30 dB balance regulation
- Mute function
- Enable pin
- Very low power consumption (0.6 mA @ VDD = 5 V)
- Extremely low quiescent current when disabled (0.01 mA)
- Suitable for connecting to an external remote controller circuit
- Using single SLG47004 IC

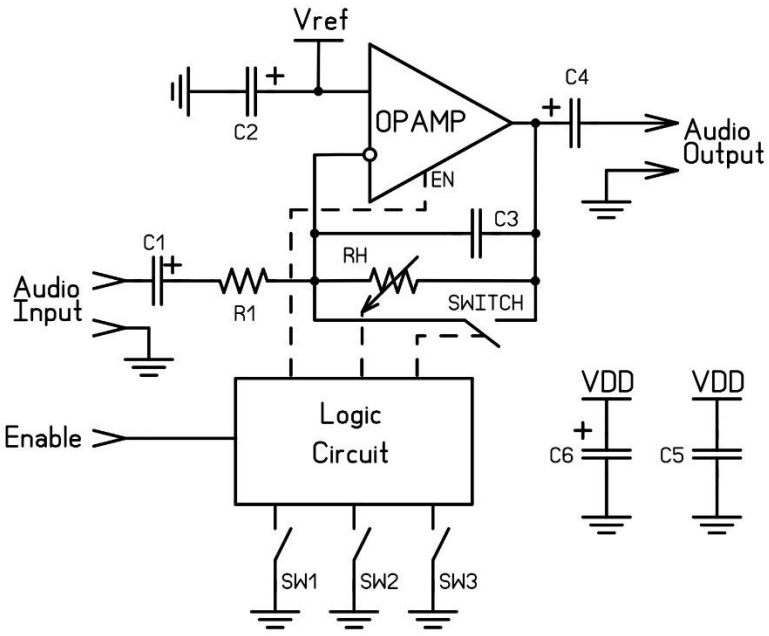

Figure 1: Simplified Schematic Diagram. One Channel

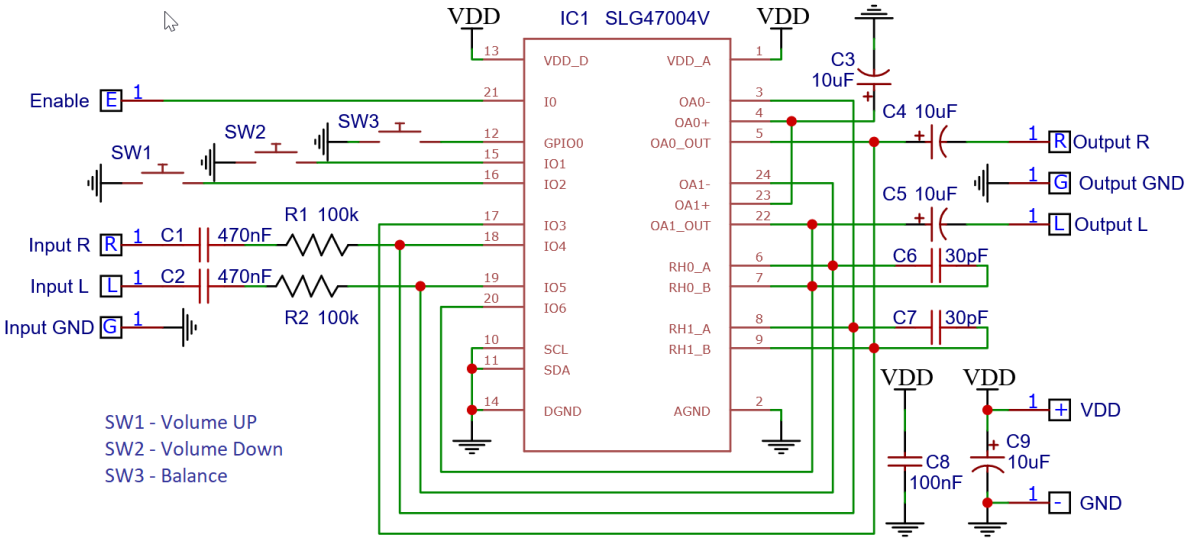

Figure 2: Full Schematic Diagram

4 Design Operation

4.1 Schematic Design

As previously mentioned, only one chip is used in this design. The SLG47004 IC combines all necessary analog and digital macrocells in a tiny 3 x 3 mm STQFN-24 package. See Figure 3 for a complete schematic diagram in the GreenPAK Designer project.

Analog Part

Since the SLG47004 contains only rheostats as opposed to potentiometers, it is impossible to make a fully functional volume control circuit. But the IC also has two OPAMPs suitable for audio applications. Figure 1 shows a simple solution how to design a signal attenuator using the rheostat and not sacrificing any gain or linearity. The circuit is an inverting amplifier with an adjustable feedback resistor. Using an input resistor equal to the maximum rheostat resistance (100k) the maximum gain is 0. According to the datasheet minimum rheostat resistance is 100 Ohm, which makes the minimum gain of -60 dB.

One of the benefits of using the SLG47004 is the internal voltage reference, which can be set to ½ of the power supply voltage. That eliminates the need for a bipolar power supply, so the device is powered from a single supply of 2.7 to 5 V, which is perfect for battery-powered applications.

The capacitors C6 and C7 are optional and are placed parallel to the negative feedback loop to reduce the bandwidth higher than 20 kHz. This makes the circuit more stable and reduces the high-frequency noise.

Another benefit of the IC is two analog switches on board. They allow implementation of the Mute function. Connected parallel to the rheostat when engaged the switch shortens the negative feedback loop thus instantly reducing the gain to even less than -60 dB.

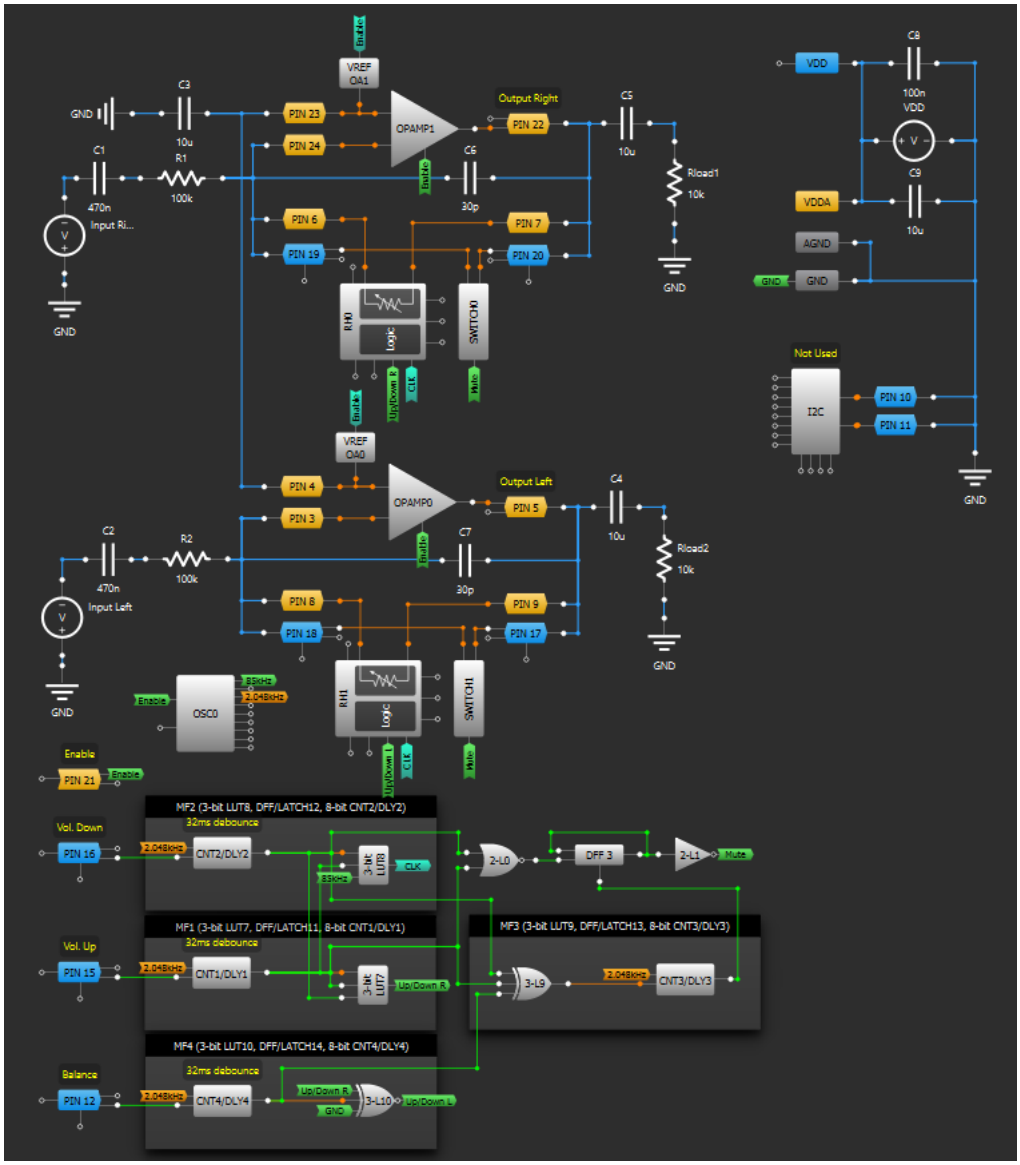

Figure 3: Digital Stereo Volume and Balance Controller Project

Digital Part

The Digital Stereo Volume and Balance Controller described in this paper is operated by three buttons: Volume Up, Volume Down, and Balance (see Figure 2). All button inputs are active Low and have pull-up resistors to the VDD. This should be kept in mind when connecting to an external controller for the remote-controlled operation. Also, the device has the Enable input which is active High. It must be connected to VDD when not used. It should be noted that when the Enable pin is Low, the device is in an idle state, the OPAMPs are disconnected from the pins internally. This means the signal will go through even though the volume was down or muted before.

All button inputs go through a 32 ms delay, which serves as a debounce, thus eliminating any external RC filters.

4.2 Using the Device

The Digital Stereo Volume and Balance Controller is typically connected in between the signal source and the power amplifier. The Enable pin is active High, so to start operating it must be pulled up externally. The default gain is set in the design to about -12 dB (can be set to any value in the range of 0 to -60 dB in the design).

All buttons have a built-in debounce of 32 ms. Any signal shorter than that will be filtered out.

To increase the volume the button «Volume Up» must be pressed. The volume will keep rising until the button is released or the maximum level is reached. The button «Volume Down» works the same way but with the opposite result.

To shift the balance to the right or left channel, the button «Balance» must be pressed and held. At the same time, one of the buttons «Volume Up» or «Volume Down» must be pressed. In the first case, the volume will increase in the left channel and decrease in the right one panning to the left. In the second case, the volume will be panned to the right. If the volume is turned all the way up or down, the balance (panning) will be set to the center.

To activate Mute both «Volume Up» and «Volume Down» buttons must be pressed simultaneously. To deactivate Mute any of the three buttons can be pressed.

Some modern audio applications do not require balance regulation, for example, Bluetooth speakers or other low-budget or mono devices. In this case, Pin12 can be left unconnected or pulled up to VDD. Or balance regulation function can be deleted from the design. Either way, this will not affect any other functionality.

4.3 Macrocell Configuration

Table 1: PIN settings

Properties	PIN 3 to 9, and 17 to 24	PIN 10 and 11	PIN 12, 15, and 16	PIN 21
I/O selection	Analog input/output	Digital input	Digital input	Digital input
Input mode OE=0	Analog input/output	Digital in without Schmitt trigger	Digital in with Schmitt trigger	Digital in with Schmitt trigger
Output mode OE=1	Analog input/output	None	None	None
Resistor	Floating	Floating	Pull Up	Floating
Resistor value	Floating	Floating	100k	Floating

Table 2: OPAMP Settings

Properties	OPAMP0	OPAMP1
Mode	OpAmp mode	OpAmp mode
Bandwidth Selection	2 MHz	2 MHz
Charge Pump	Disable CP	Disable CP

Properties	OPAMP0	OPAMP1
Supporting Blocks On/Off	Follows OpAmp	Follows OpAmp
Vref connection	To IN+	To IN+
Vref	VDDA*(32 / 64)	VDDA*(32 / 64)

Table 3: Vref Settings

Properties	VREF OPAMP0	VREF OPAMP1
Enable selection	From register	From register
Register enable	Vref enable	Vref enable
Input voltage selection	VDDA	VDDA
Output selection	VDDA*(32 / 64)	VDDA*(32 / 64)

Table 4: Oscillator

Properties	OSC0
Control pin mode	Force on
OSC power mode	Auto Power on
Clock selector	OSC
CLK predivider by:	1
OUT0 second divider by:	24
OUT1 second divider by:	1

Table 5: Digital Rheostat Settings

Properties	RH0	RN1
Mode	None	Rheostat
Charge Pump Enable	From matrix	From matrix
Charge Pump Clock	Auto selection	Auto selection
Auto-Trim	Disable	Disable
Active level for UP/DOWN	Up when HIGH	Up when HIGH
Resistance (initial data)	256	256
UP/DOWN source	Ext. (From matrix)	Ext. (From matrix)
Clock	Ext. Clock (From matrix)	Ext. Clock (From matrix)

Table 6: Analog Switch Settings

Properties	SWITCH0	SWITCH1
Mode	Analog Switch	Analog Switch
Big PMOS control	By Matrix	--
Big NMOS control	--	By Matrix
Small NMOS enable	Disable	--

Properties	SWITCH0	SWITCH1
Small PMOS enable	--	Disable
Half Bridge Dead Time Select	Bypass	Bypass

Table 7: LUT Settings

IN2	IN1	IN0	2-bit LUT0	2-bit LUT1	3-bit LUT7 (MF1)	3-bit LUT8 (MF2)	3-bit LUT9 (MF3)	3-bit LUT10 (MF4)
0	0	0	1	Inverter	1	0	0	1
0	0	1	0		1	0	1	0
0	1	0	0		1	0	1	0
0	1	1	0		1	1	0	1
1	0	0	--		1	0	1	0
1	0	1	--		1	1	0	1
1	1	0	--		0	0	0	1
1	1	1	--		0	0	1	0

Table 8: DFF Settings

Properties	DFF3
Type	DFF / LATCH
Mode	DFF
Second Q select	Q of first DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Inverted (nQ)
Active level for RST/SET	Low level

Table 9: CNT/DLY Settings

Properties	8-bit CNT1/DLY1 (MF1)	8-bit CNT2/DLY2 (MF2)	8-bit CNT3/DLY3 (MF3)	8-bit CNT4/DLY4 (MF4)
Mode	Delay	Delay	Delay	Delay
Counter data	65	65	65	255
Edge select	Both	Both	Both	Both
DLY IN init. value	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial
Output polarity	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)
Mode signal sync.	Bypass	Bypass	Bypass	Bypass
Clock	OSC0	OSC0	OSC0	OSC0

I2C Settings: default.

4.4 PCB Layout

The PCB was designed using the easyeda.com service. See the full schematic diagram, PCB design, and PCB 3D model in Figures 2 and 4. The size of the board is 21 x 17 mm.

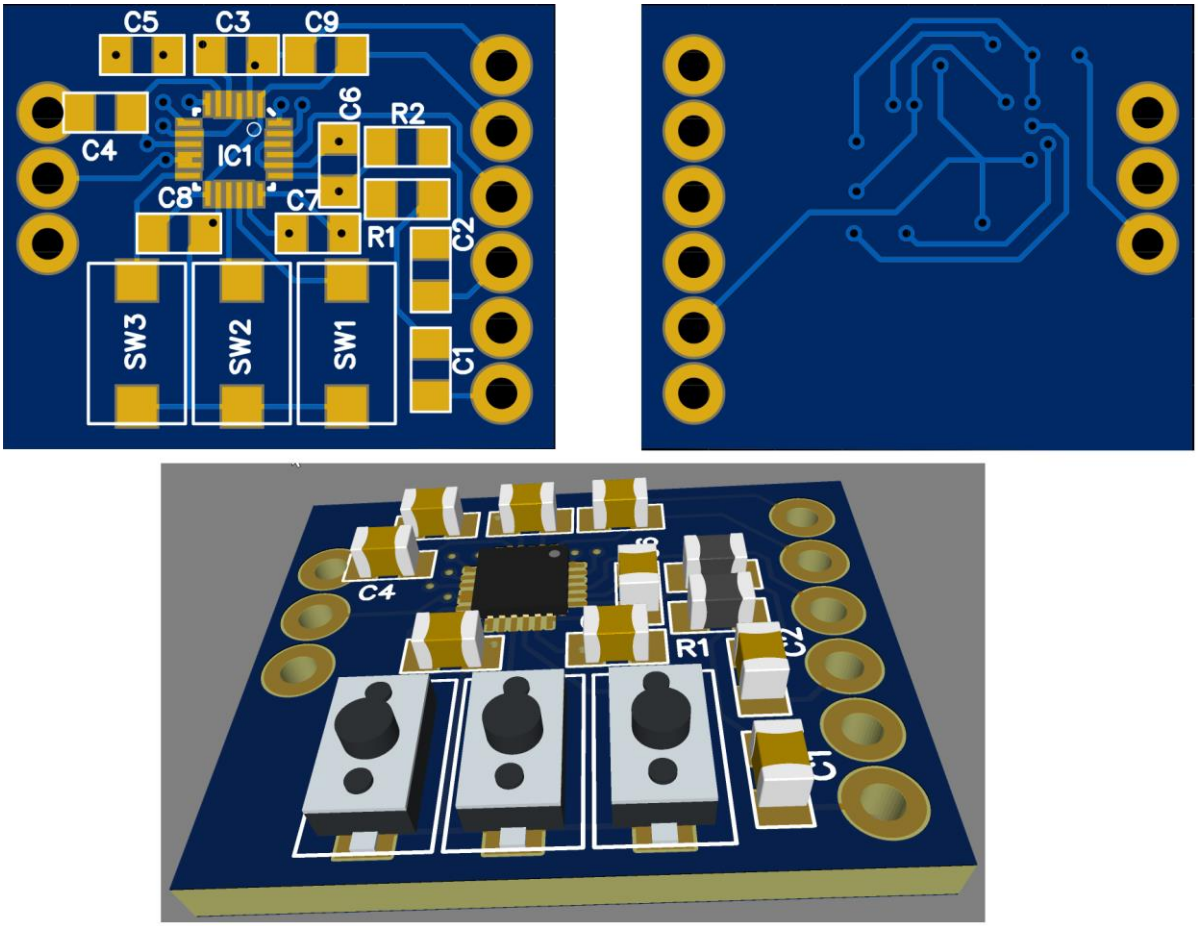

Figure 4: PCB Design and 3D Model

4.5 Suggestions for Future Designs

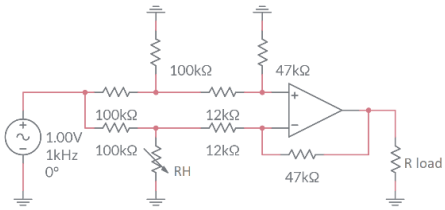

Figure 5: Attenuator with Logarithmic Characteristics

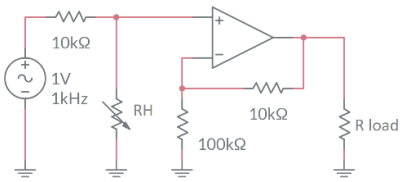

Figure 6: Attenuator With Inverse Logarithmic Characteristics

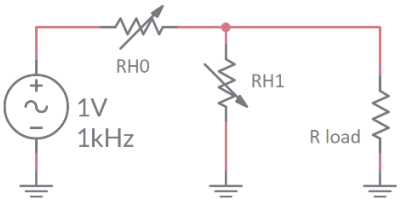

Figure 7: Using Two Rheostats in Potentiometer Mode

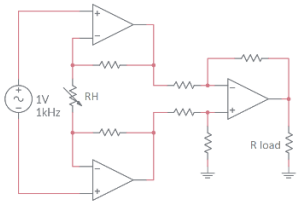

Figure 8: Instrumentation Amplifier with Controlled Gain

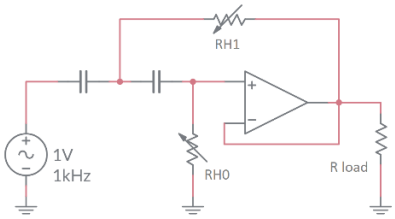

Figure 9: Adjustable 2nd Order High Pass Active Filter

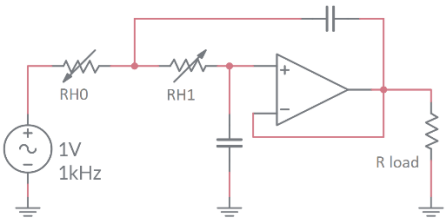

Figure 10: Adjustable 2nd Order Low Pass Active Filter

5 Conclusions

As can be seen, designing and building a digital stereo volume and balance controller with a mute function using the OPAMP PAK is very easy. The SLG47004 turned out to be the perfect IC for the design containing all necessary analog and digital macrocells. The design shown in this document is one of many versions of the device that can be built based on the SLG47004. There are some unused macrocells that can be used to design additional functions. And vise versa, if some features are not required, they can be easily deleted from the design.

Revision History

Revision	Date	Description
1.0	14-Feb-2022	Initial Version

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