Application Note

Frequency Multiplier

AN-CM-329

Abstract

This application note describes how to design a frequency multiplier circuit using only a single GreenPAK IC. It includes design files which can be found in the References section.

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1 Terms and Definitions

CD	Counter Data
CNT	Counter
DCMP	Digital Comparator
FSM	Finite State Machine

Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	NC	--	Keep Floating or Connect to GND	--
4	FLAG	Digital Output	Push Pull 1X	floating
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	NC	--	Keep Floating or Connect to GND	--
8	NC	--	Keep Floating or Connect to GND	--
9	NC	--	Keep Floating or Connect to GND	--
10	NC	--	Keep Floating or Connect to GND	--
11	GND	GND	Ground	--
12	IN	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
13	NC	--	Keep Floating or Connect to GND	--
14	NC	--	Keep Floating or Connect to GND	--
15	NC	--	Keep Floating or Connect to GND	--
16	OUT	Digital Output	Push Pull 1X	floating
17	NC	--	Keep Floating or Connect to GND	--
18	NC	--	Keep Floating or Connect to GND	--
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/configurable-mixed-signal.

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-329 Frequency Multiplier.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

3 Introduction

This application note describes how to implement a frequency multiplier using a GreenPAK™ programmable mixed-signal IC. The frequency multiplier can be used in a range of applications including control circuits and communication devices.

4 Frequency Multiplier

The overall GreenPAK design is shown in the figures below:

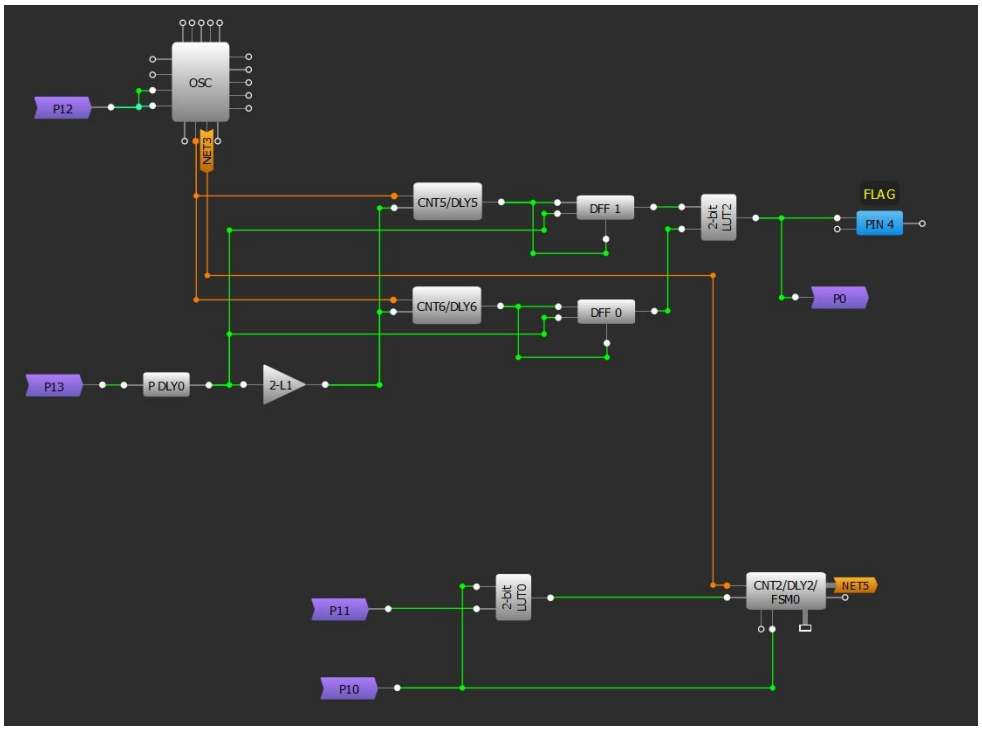

Figure 1: GreenPAK Design Flag Circuit

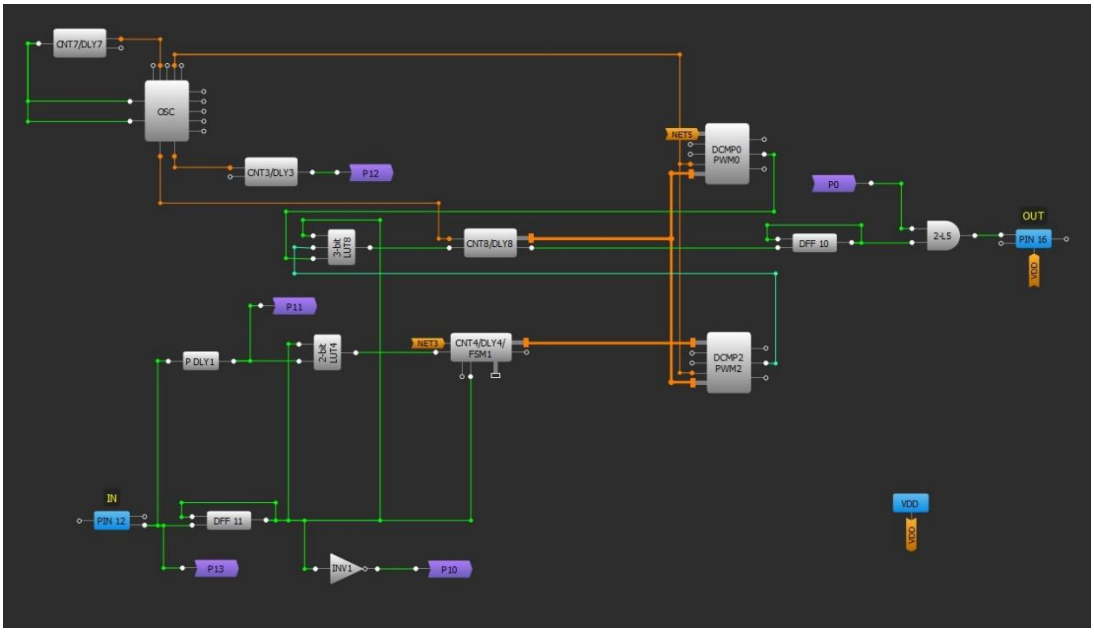

Figure 2: GreenPAK Design Out Circuit (continued)

The design can be divided into the following blocks:

Frequency Multiplier

Selector

Multiplier settings

FLAG

OUT

5 Frequency Multiplier

The design includes two frequency multiplier blocks consisting of FSM0/DCMP0 and FSM1/ DCMP2.

The frequency multiplier block that consists of FSM1/DCMP2 operates as follows: When the signal from the selector is LOW, then FSM1 counts the IN frequency, and when the signal from the selector is HIGH, then FSM1, CNT8, and DCMP2 generate an OUT frequency.

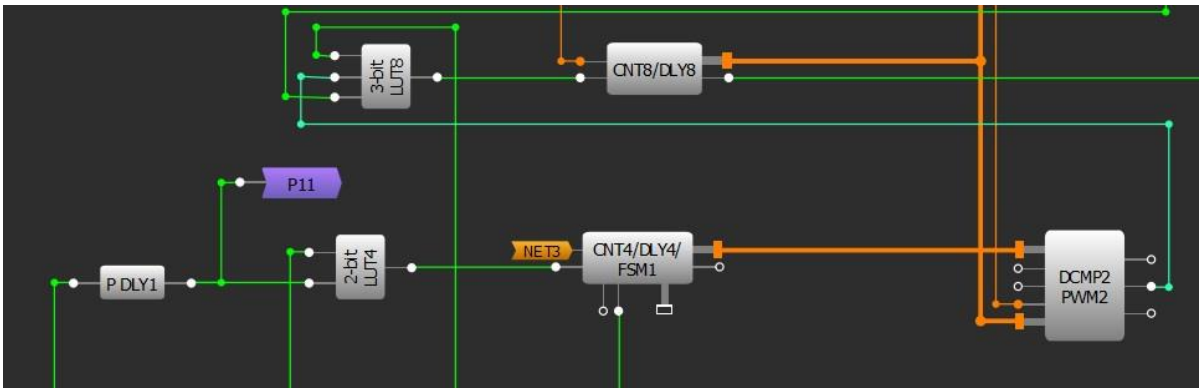

Figure 3: Frequency Multiplier

6 Selector

The selector chooses which of the two blocks counts input frequency and which generates the multiplied output frequency.

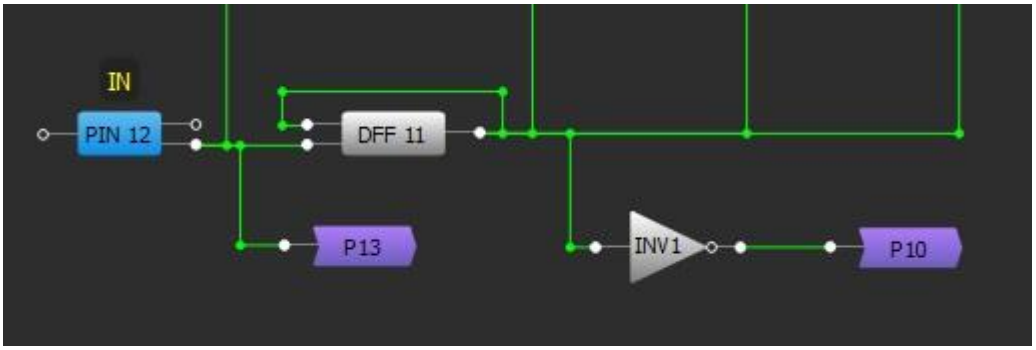

Figure 4: Selector

7 Multiplier Settings

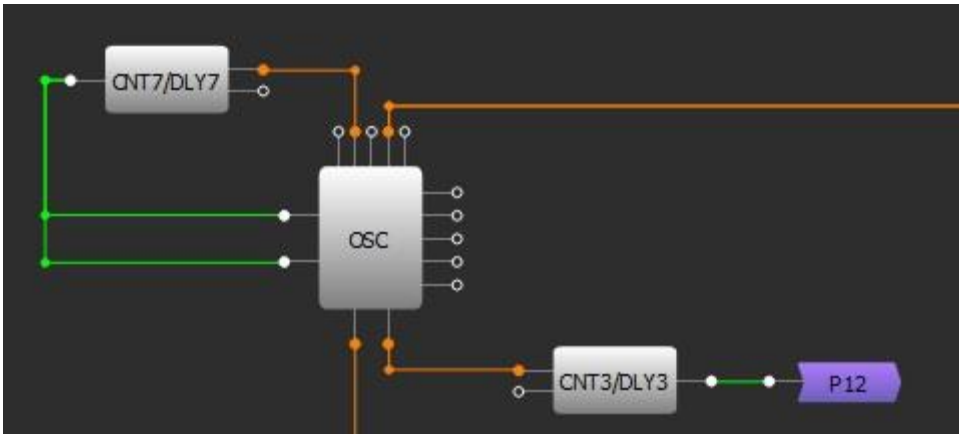

Figure 5: Multiplier Settings

CNT3 is used to select a factor by which the input frequency is multiplied. The counter data is determined by the formula:

$$CD = 2 * N - 1$$

where CD is counter data and N is the multiplying factor.

CNT7 is used to determine the input frequency. The counter period should be approximately:

$$\mathrm{T} \approx \frac{1}{100 \cdot F \cdot N}$$

where T is the counter period, F is the approximate input frequency, and N is the multiplying factor.

8 FLAG

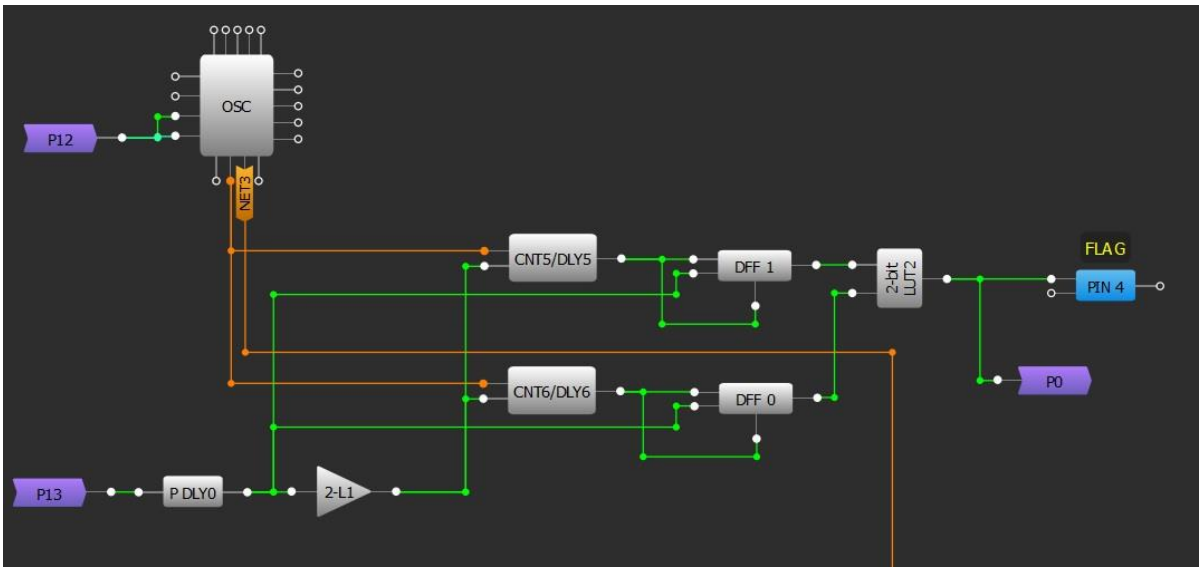

Figure 6: FLAG

For a given input frequency the circuit multiplexer range is between 0.2x and 5x. If the frequency is outside of this range, then FLAG will be LOW.

9 OUT

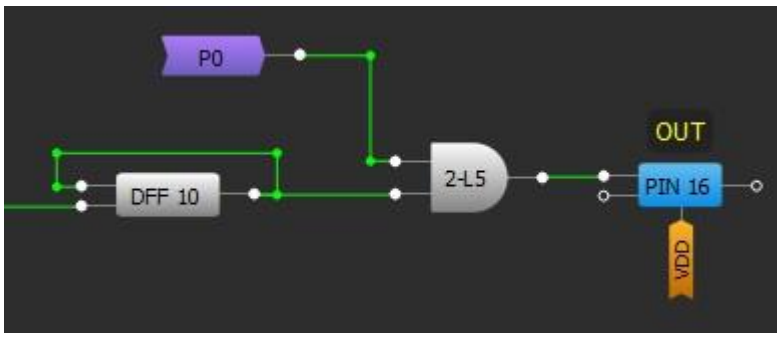

Figure 7: OUT

If FLAG is HIGH, DFF10 generates the output frequency with a 50% duty cycle. If FLAG is LOW, then OUT will be LOW.

10 Example

For example, consider multiplying an input frequency of ~1kHz by a factor of 15. The counter data CNT3 should be:

$$CD = 2 * 15 - 1 = 29$$

The counter period of CNT7 should be:

$$\mathrm{T} \approx \frac{1}{100 \cdot 1000Hz \cdot 15} \approx 666\ \mathrm{ns}$$

11 Experimental Waveforms

Channel 1 (yellow/top line): PIN#12 (IN)
Channel 2 (light blue/2nd line): PIN#4 (FLAG)
Channel 3 (magenta/3rd line): PIN#16 (OUT)

Figure 8: Waveform when input frequency is 1kHz

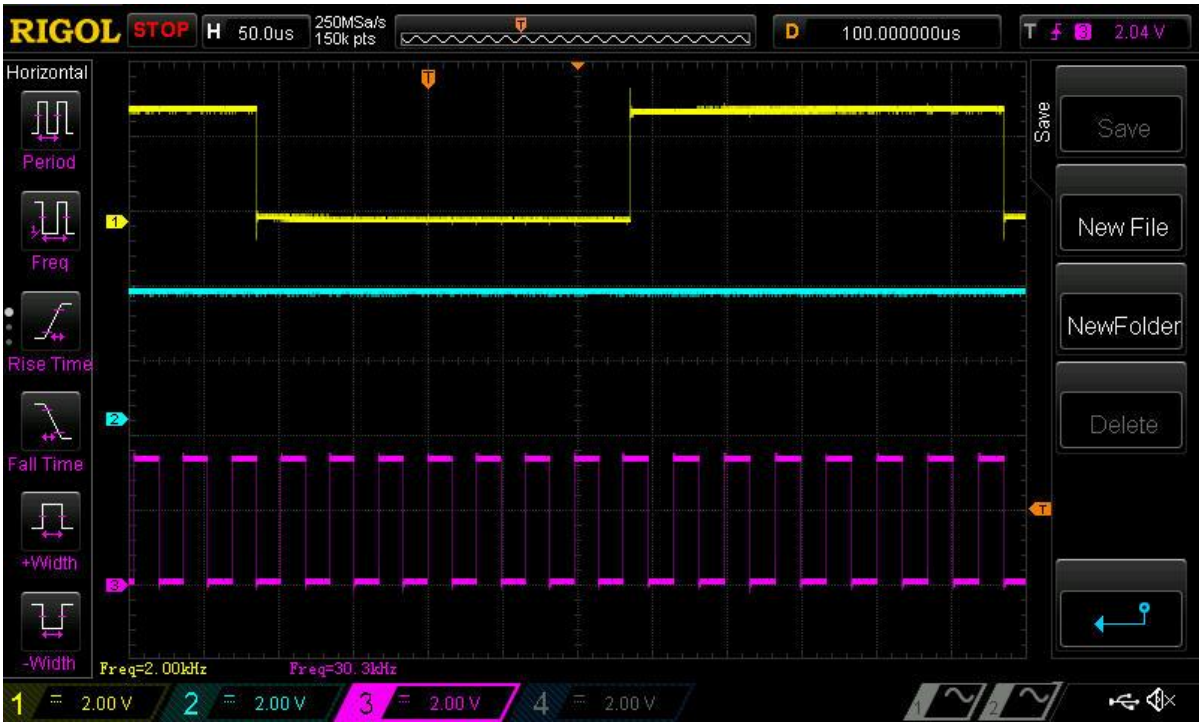

Figure 9: Waveform when input frequency is 2kHz

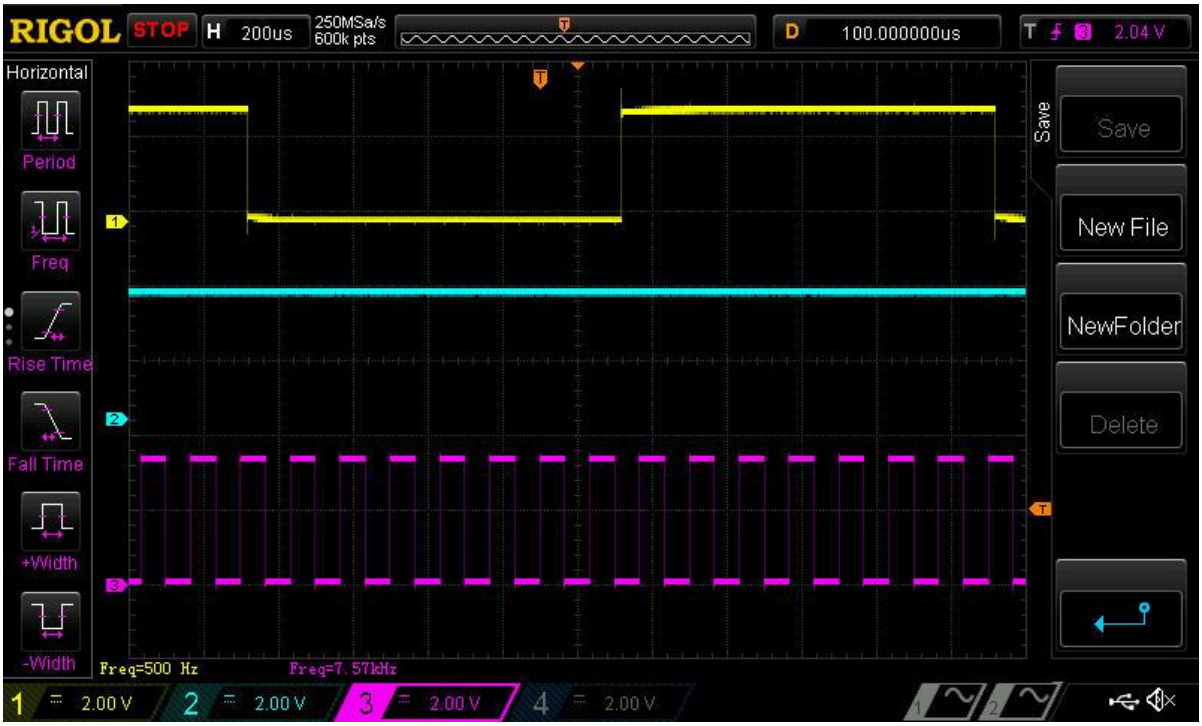

Figure 10: Waveform when input frequency is 0.5kHz

Figure 11: Waveform when input frequency is 6kHz

Figure 12: Waveform when input frequency is 150 Hz

Conclusion

This application note demonstrates how to make a frequency multiplier using a GreenPAK IC. Only a few internal blocks of the SLG46620 chip are used, leaving the bulk of the blocks available to build other circuitry. The given design is limited to an input frequency range of 0.2x to 5x the typical frequency for which the circuit was debugged (~1kHz). The typical output frequency cannot exceed 135 kHz.

Due to its size, configurability, and price, the GreenPAK is an excellent approach to implement a frequency multiplier.

Revision History

Revision	Date	Description
1.0	09-Mar-2022	Initial Version

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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