Application Note

Class D Power Amplifier Using HVPAK

AN-CM-321

Abstract

This application note describes several ways of implementing a self-oscillating class D audio power amplifier.

The application note comes complete with design files that can be found in the Reference section.

Contents

Figures

Tables

1 Terms and Definitions

ACMP	Analog Comparator
GPO	General Purpose Output
HV	High Voltage
IC	Integrated Circuit
I/O	Input / Output
LUT	Look-up Table
MOSFET	Metal–oxide–semiconductor Field-effect Transistor References
PWM	Pulse Width Modulation
THD + N	Total Harmonic Distortion Plus Noise

2 References

For related documents and software, please visit:
HVPAK™ | Renesas

Download our free GreenPAK Designer software [1] to open the .gp file [2] and view the proposed circuit design. Use the GreenPAK development tools [2] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download, and User Guide
[2] AN-CM-321 Class D Power Amplifier Using HVPAK.hvp, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47105 Datasheet
[6] Simple Self-Oscillating Class D Amplifier with Full Output Filter Control by Bruno Putzeys, May 2010
[7] A Universal Grammar of Class D Amplification by Bruno Putzeys, Hypex Electronics, The Netherlands, May 2007

Author: Nazar Sliunchenko

3 Introduction

This application note describes how to design a simple class D power amplifier using the High Voltage GreenPAK IC.

A class D amplifier operates by deriving a two-state signal from a continuous control signal and amplifying it using power switches. At the core of every class D amplifier is at least one comparator and one switching power stage. In all but the lowest-cost power amplifiers, a passive LC filter is added.

Here's a summary of the benefits and disadvantages of the Class-D amplifier versus the traditional Class-AB amplifier.

- Class AB

Benefit: Lowest distortion—total harmonic distortion plus noise (THD + N) is less than 0.1% for high fidelity.

Disadvantages: Inefficient—maximum possible efficiency is about 60%. High power consumption and significant heat generation. It's also larger in size.

- Class D

Benefits: High efficiency—greater than 90%. Less power consumption and lower heat generation. Smaller size. Very high-power potential (400 to 500 W) in a small package.

Disadvantages: High-frequency noise generation.

The most basic topology utilizes pulse-width modulation (PWM) with a triangle-wave (or sawtooth) oscillator. Figure 1 shows a simplified block diagram of a PWM-based, half-bridge Class D amplifier. It consists of a pulse-width modulator, two output MOSFETs, and an external lowpass filter (L_F and C_F) to recover the amplified audio signal. As shown in the figure, both MOSFETs operate as current-steering switches by alternately connecting the output node to V_{DD} and ground, thus the resulting output of a Class D amplifier is a high-frequency square wave. The output square wave is pulse-width modulated by the input audio signal. PWM is accomplished by comparing the input audio signal to an internally generated triangle-wave (or sawtooth) oscillator. The resulting duty cycle of the square wave is proportional to the level of the input signal. When no input signal is present, the duty cycle of the output waveform is equal to 50%. Figure 2 illustrates the resulting PWM output waveform due to the varying input-signal level.

This basic topology has a few downsides: Very low power supply rejection ratio, and High THD. The quality of the output signal is highly dependent on the linearity and stability of the triangle wave, which significantly complicates the circuit.

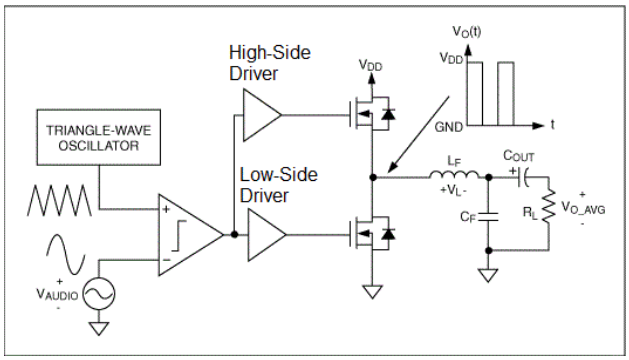


Figure 1: Half-Bridge Class D Amplifier, Basic Topology

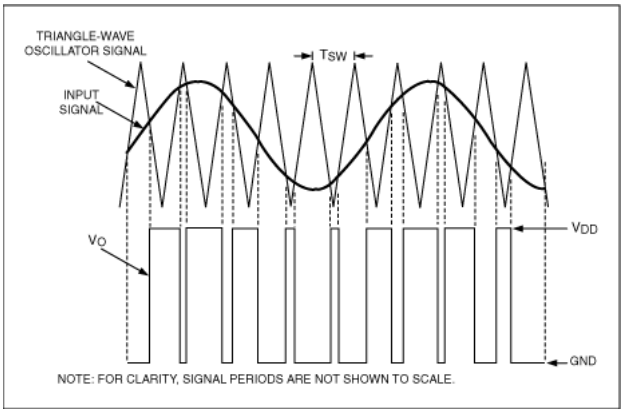


Figure 2: The Output-Signal Pulse Widths Vary Proportionally With the Input-Signal

One of the most commonly used topologies of class D audio amplifiers is known as self-oscillation. Self-oscillating class D audio amplifiers are characterized by having an open-loop bandwidth equal to the switching frequency as opposed to traditional PWM amplifiers, where the loop bandwidth typically will be limited to one-tenth of the switching frequency. This increased loop bandwidth provides valuable loop gain at low frequency, which is beneficial with respect to the reduction of Total Harmonic Distortion (THD).

There are several ways of designing a self-oscillating class D power amp, such as:

- Hysteresis switching, see Figure 3.

  The obvious shortcoming of this circuit is the variability of the switching frequency as a function of the power supply voltage. A minor modification is to use the switching waveform itself as the hysteresis feedback. Amplifiers constructed along these lines typically produce fairly respectable performance, accounting for the popularity of this arrangement. The most important problem here is that the minimum pulse width produced is only half that of the idle pulse width. The operating frequency swings quite strongly with the modulation index, following a parabola with its maximum at zero modulation and hitting zero at maximum modulation. The result is modulation close to clipping, as the switching frequency traverses the audio band. The oscilloscope plot (Fig. 4) of the output (second-order reconstruction filter presumed) is recognizable in that regard.

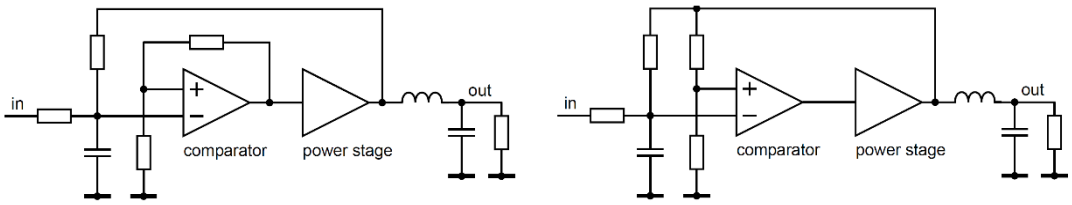


Figure 3: Hysteresis Switching Topology

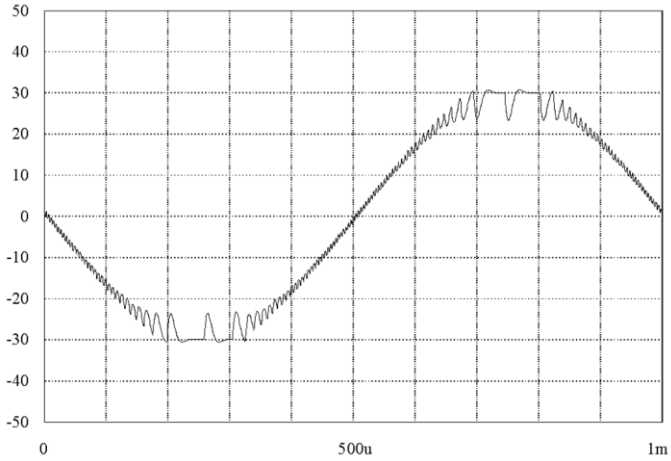


Figure 4: Hysteresis Switching Amplifier Output Signal

- Phase-shift controlled oscillation.

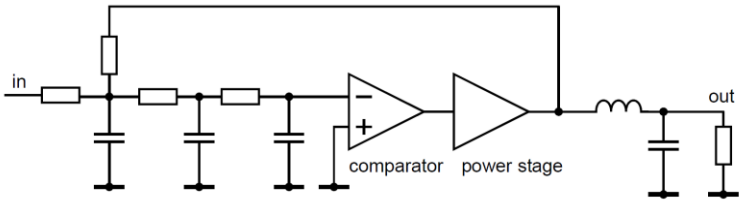


Figure 5: Phase-shift Controlled Oscillation Topology

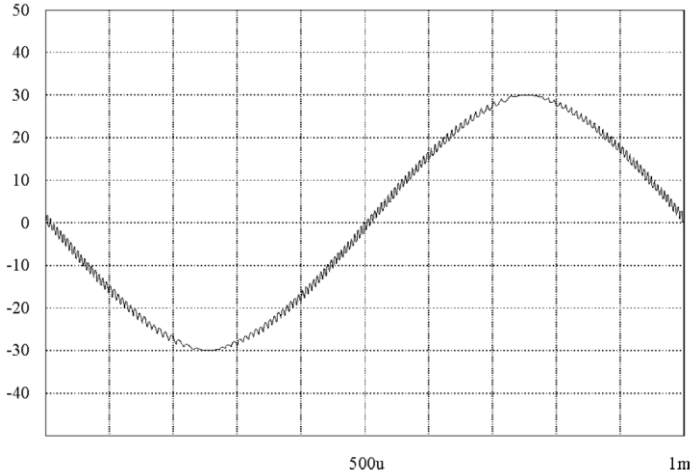


Figure 6: Phase-Shift Controlled Oscillation Amplifier Output Signal

A method of obtaining self-oscillation without the use of hysteresis employs the phase shift of the feedback network to produce stable self-oscillation. The amplifier will oscillate at the frequency where the feedback network has a 180-degree phase shift. A rather pleasing characteristic of this method is that the switching frequency can be made much more stable than with a hysteresis modulator. In theory, the minimum pulse width at maximum modulation becomes zero (in practice about twice the propagation delay of the active electronics).

Switching frequency still drops to zero in the process, but only much later, and much less energy will be in the carrier by that time. After reconstruction by a second-order filter, the amplitude of the residual remains nearly constant. Even under careful listening conditions, the clipping behavior sounds indistinguishable from that of a good linear amplifier.

A notable disadvantage of phase control is that the modulation is inherently nonlinear, adding distortion at large modulation indexes.

Nevertheless, this topology provides a simple low-cost solution suitable for most applications. For the HV PAK design refer to Section 4.1 and Section 4.2.

- Phase-shift control using the reconstruction filter.

  The phase shift of the reconstruction filter is usually seen as a burden, rarely as an advantage. Second-order filters turn out to be very interesting for building phaseshift controlled amplifiers. One is reminded that the switching frequency is set well beyond the corner frequency of the filter. At any sufficiently high frequency, a second-order low pass filter produces a phase shift close to 180 degrees. Varying load conditions only affect this to the order of a few degrees.

  Closing a negative feedback loop around such a filter is not enough though. The oscillation occurs at a phase shift of exactly 180 degrees (the other 180 degrees are furnished by the polarity inversion), which only happens at infinity. An additional network is in order that holds the phase shift well away from 180 degrees below the desired switching frequency, and another one that pushes it well beyond it above this frequency. Any practical circuit will already have the latter for free. The combined propagation delays of the comparator and the power stage constitute a phase shift directly proportional to frequency. The former can be as simple as a phase lead network in the feedback path.

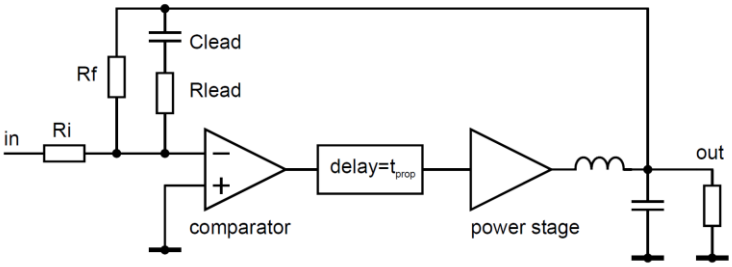
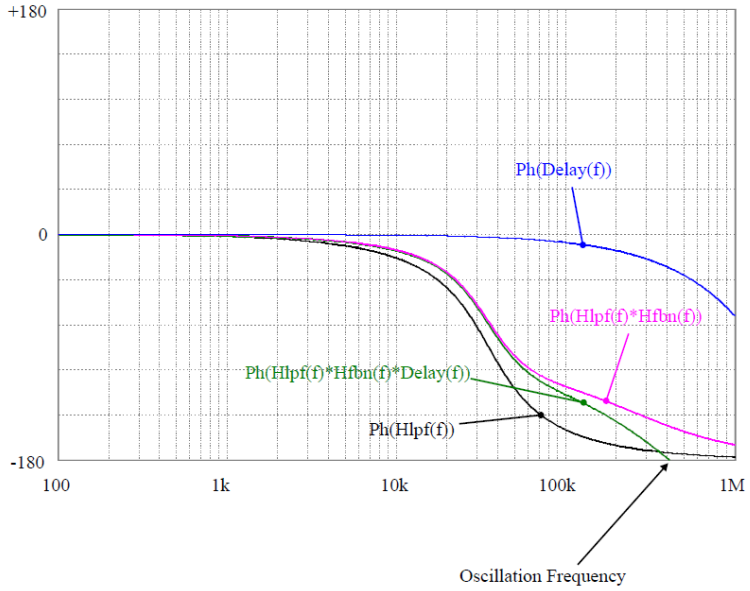


Figure 7: Phase-Shift Control Using the Reconstruction Filter Topology

Since at any useful oscillation frequency the phase shift of the output filter is 180 degrees, oscillation will occur at the frequency where the propagation delay and the phase lead cancel out. Care should be taken to ensure that under any realistic load condition there is not a second point with 180 degrees phase shift, because this point will be most certainly be the physical resonance frequency filter. Failing this usually leads to the undoing of the amplifier the first time it is overdriven with no load attached. See Figure 8.



Where H_{lpf} is the transfer function of the LC filter and H_{fbn} that of the feedback network Delay(s) is a linear phase shift function representing the propagation delay.

Figure 8: Phase-Shift

The phase-shift control using the reconstruction filter topology has a big advantage over previously described topologies. The negative feedback loop is encompassing the reconstruction filter, this allows to completely compensate for any non-linearity. The amplifier designed using this topology is capable of producing extremely low THD+N and can compete with class AB while having all advantages of class D.

Note that this topology is not considered in this application note. It is a subject for future projects.

4 Design Operation

4.1 Simple Phase-shift Controlled Oscillation Amplifier

To build a simple phase-shift controlled oscillation amplifier using HV PAK requires a minimum of two macrocells: ACMP and HV OUT CTRL. Figure 10 shows a GreenPAK Designer project of such a device. This amplifier provides a simple solution and requires fewer external components which means less PCB surface. As can be seen, this project uses only one HV bridge (mono). The other one can be used as a second channel (stereo) or to drive a motor or solenoid, for example, in the intercom device to lock/unlock the door. In addition, this design has the Enable function on PIN 2 which is active LOW. This schematic has a relatively high oscillating frequency, close to 680 kHz, but in this case, it is an advantage. The higher the frequency, the smaller the output filter L1, L2, and C4. Figure 9 shows the test PCB and its dimensions. If required, the frequency can be decreased by increasing capacitance C2.

The amplifier has the following characteristics:

- Power supply voltage – 3.5 V to 5 V
- Current consumption (no input signal) – 3.2 mA

- Stand-by current (Enable – Low) – 0.82 mA
- Output power (supply – 5V, load – 4 Ohm) – 3 W (max)
- Gain – 20 dB
- Input resistance – 5.6 kOhm

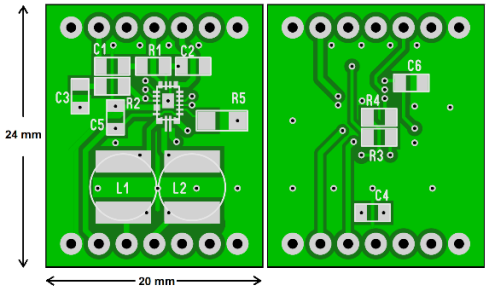


Figure 9: Test PCB. Top – Left, Bottom – Right

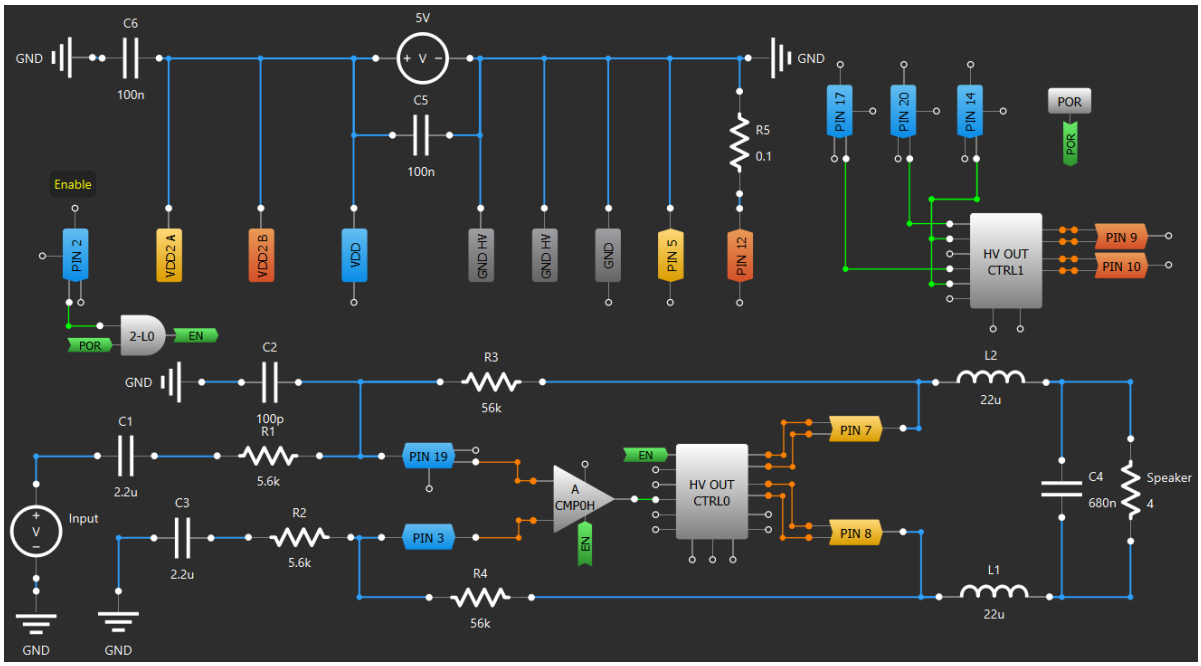


Figure 10: Simple Phase-shift Controlled Oscillation Amplifier Project

Also, as previously mentioned, the design has the option of driving an electric motor, solenoid, relay, or similar device by HV OUT CTRL1 bridge. In this case, it is configured as two separate half-bridges

and can be controlled individually. PIN 20 controls the half-bridge outputted to PIN 9 and PIN 17 controls the half-bridge outputted to PIN 10. PIN 14 serves to enable the bridge (active HIGH).

4.1.1 Macrocell Configuration

Table 1: PIN Settings

Properties	PIN 2	PIN 14, 17, and 20	PIN 7, 8, 9, and 10	PIN 3 and 19
I/O selection	Digital input	Digital input	Digital output	Analog input/output
Input mode OE=0	Digital in with Schmitt trigger	Digital in without Schmitt trigger	None	Analog input/output
Output mode OE=1	None	None	HIGH and LOW side	Analog input/output
Resistor	Pull Up	Pull Down	--	Floating
Resistor value	1M	1M	--	Floating

Table 2: LUT Settings

IN1	IN0	2-bit LUT0 OUT
0	0	0
0	1	0
1	0	0
1	1	1

Table 3: ACMP Settings

Properties	ACMP0H
Hysteresis	Disable
IN+ gain	Disable
Connections	
IN+ source	PIN 19 (GPIO5)
IN- source	Ext. Vref (PIN 3 (GPI))

Table 4: HV Output Settings

Properties	HV OUT CTRL0	HV OUT CTRL1
Slew rate	Fast for pre-driver mode	Fast for pre-driver mode
HV OUT mode	Full bridge	Half-bridge
Mode control	PH-EN	IN-IN
Thermal shutdown	Enable	None
OCP deglitch time enable	Without deglitch time	Without deglitch time
Control delay of OCP0 retry	Delay 492 us	Delay 492 us
Control delay of OCP1 retry	Delay 492 us	Delay 492 us
VDD2A UVLO	Desable	Desable

4.2 Phase-shift Controlled Oscillation Amplifier without Output Filter

As can be seen from the previous design, despite the low count of the external components and small HV PAK package size, the device occupies a significant part of the PCB area. While it's possible to reduce resistor's and capacitor's size down to 0201 (instead of 0805), except R5, it is impossible to use smaller inductance L1 and L2 due to high current. The next design allows working around this issue.

In the traditional design of the full bridge class D amp, both high and low-frequency signals are inverted on the bridge outputs. So, the output filter prevents load shunting the high-frequency signal.

The design, shown in Figure 11 provides a solution where the high-frequency signal on both outputs (PIN 7 and PIN 8) is in-phase, so that current will not run through the load. At the same time, the audio signal on those pins will be inverted relative to each other.

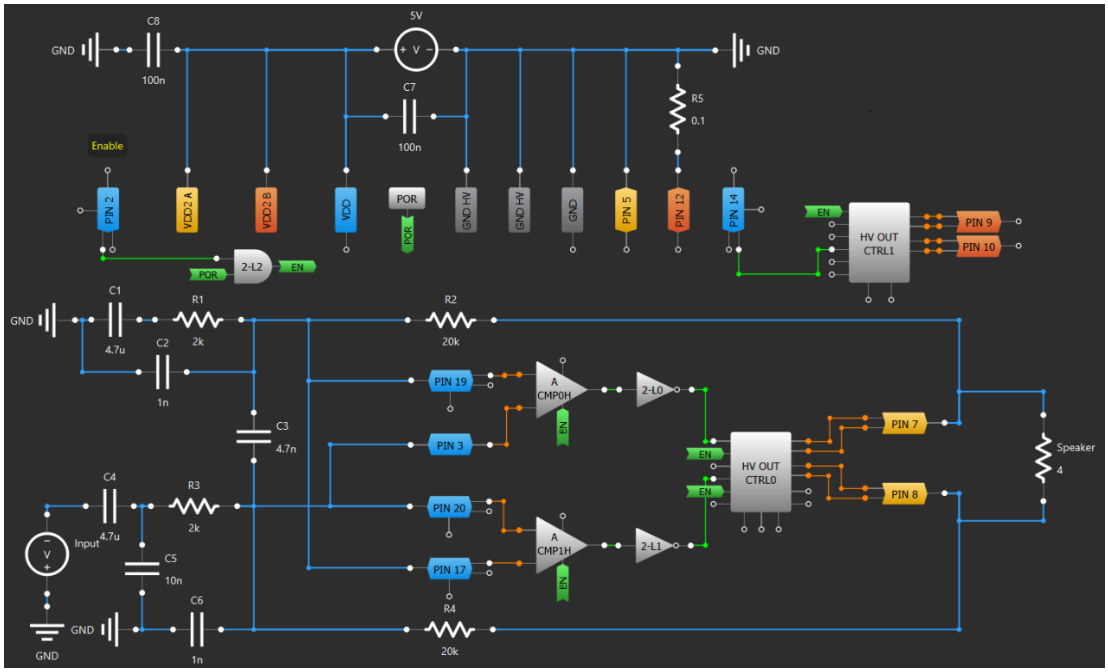


Figure 11: Phase-shift Controlled Oscillation Amplifier without Output Filter Project

This design uses more external components compared to the previous one, but the absence of two inductors results in a smaller PCB footprint, see Figure 12.

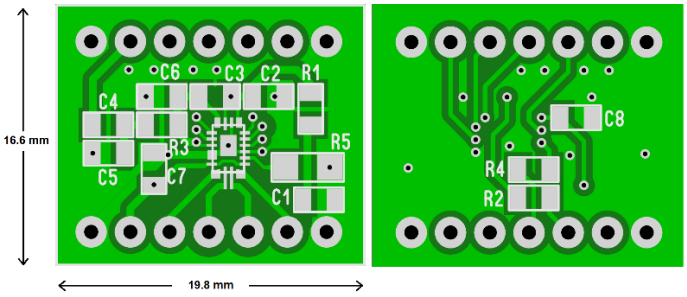


Figure 12: Test PCB without Output Filter. Top – Left, Bottom – Right

The device is working in the same way as the amp described in the previous chapter, but the HV outputs are configured as two separate half-bridges. This allows controlling both outputs independently. Using two ACMPs for each half-bridge, two identical oscillators are built which are synchronized by the capacitor C3. This results in identical (in-phase) square wave voltage on both outputs. It means the output pins can be shorted and no high-frequency current will leak.

At the same time, the audio signal is introduced to opposite inputs of two ACMPs. This results in the output signal being modulated counter-phase. So, only the low-frequency current will flow through the load, thus eliminating the need for the output filter.

The amplifier has the following characteristics:

- Power supply voltage – 3.5 V to 5 V
- Current consumption (no input signal) – 2.1 mA
- Stand-by current (Enable – Low) – 0.82 mA
- Output power (supply – 5V, load – 4 Ohm) – 3 W (max)
- Gain – 20 dB
- Input resistance – 2 kOhm

4.2.1 Macrocell Configuration

Table 5: PIN Settings

Properties	PIN 2	PIN 14	PIN 7, 8, 9, and 10	PIN 3, 17, 19 and 20
I/O selection	Digital input	Digital input	Digital output	Analog input/output
Input mode OE=0	Digital in with Schmitt trigger	Digital in without Schmitt trigger	None	Analog input/output
Output mode OE=1	None	None	HIGH and LOW side	Analog input/output
Resistor	Pull Up	Pull Down	--	Floating
Resistor value	1M	1M	--	Floating

Table 6: LUT Settings

2-bit LUT0	2-bit LUT1
Inverter	Inverter

Table 7: ACMP Settings

Properties	ACMP0H	ACMP1H
Hysteresis	Disable	Disable
IN+ gain	Disable	Disable
Connections		
IN+ source	PIN 19 (GPIO5)	PIN 20 (GPIO6)
IN- source	Ext. Vref (PIN 3 (GPI))	Ext. Vref (PIN 17 (GPIO4))

Table 8: HV Output Settings

Properties	HV OUT CTRL0	HV OUT CTRL1
Slew rate	Fast for pre-driver mode	Slow for motor drive
HV OUT mode	Half-bridge	Full bridge
Mode control	IN-IN	PH-EN
Thermal shutdown	Enable	None
OCP deglitch time enable	Without deglitch time	Without deglitch time
Control delay of OCP0 retry	Delay 492 us	Delay 492 us
Control delay of OCP1 retry	Delay 492 us	Delay 492 us
VDD2A UVLO	Desable	Desable

4 Conclusions

As can be seen, building a simple low-cost class D amplifier is very easy using the High Voltage GreenPAK IC. Both designs shown in this document are the simplest versions of the devices that can be built based on the SLG47105. They are not intended to be a part of Hi-Fi equipment, but nevertheless can be used in portable audio devices, intercoms, doorbells, etc. The amplifier described in Section 4.1 can be modified to a Stereo amplifier, or the remaining full-bridge (or two half-bridges) can be used to drive any high current load such as DC motor, solenoid, relay, high power LED, etc. The last statement is also true for the amplifier described in Section 4.2.

Revision History

Revision	Date	Description
1.0	25-Aug-2021	Initial Version

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.