Application Note

Adjustable Analog Filter

AN-CM-310

Abstract

This application note illustrates how to use the SLG47004 to implement an adjustable analog filter and describes different ways to adjust the filter`s cutoff frequency.
The application note comes complete with design files which can be found in the References section.

Contents

1 Terms and Definitions

ADC	Analog-to-digital converter
CNT	Counter
DFF	D flip-flop
LUT	Look up table
OpAmp	Operational amplifier

2 References

For related documents and software, please visit:

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Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-310 Adjustable Analog Filter.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] Analog Filter Wizard, Filter Design Tool Webpage, Analog Devices

Author: Marian Hryntsiv

3 Introduction

There are a variety of applications where signals from different sources (for example, sensors) are sensed with one ADC. Such systems require an analog multiplexer with analog filters for each channel, because each signal source may have its own set of filter requirements (for example, different cutoff frequencies). An alternative space-efficient and cost-efficient solution is to use one tunable analog filter for all channels (Figure 1). The SLG47004 IC solves this task perfectly.

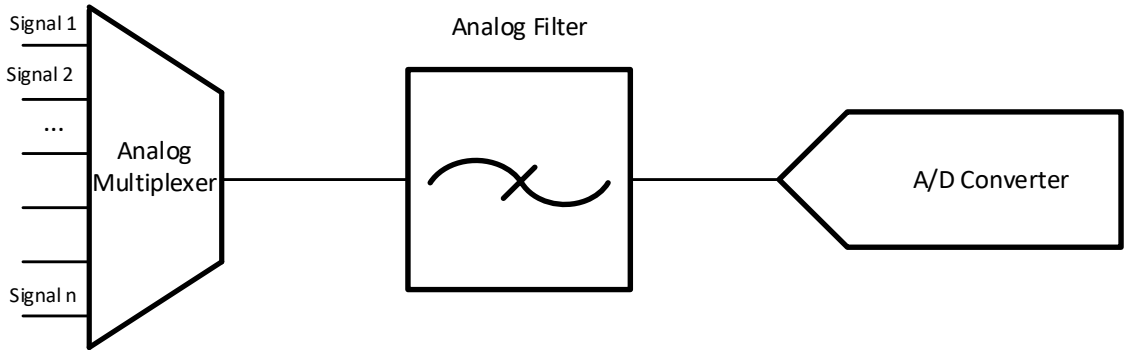

Figure 1: Analog Interface with One Tunable Filter

4 System Overview

This application note demonstrates the implementation of the adjustable analog filter by highlighting an example second-order, programmable, active low-pass Sallen-Key filter (Figure 2).

This filter is implemented with two resistors, two capacitors, and an operational amplifier. Two resistors in this circuit are replaced with the SLG47004 Digital Rheostats, and one of the SLG47004 operational amplifiers is used as an active element.

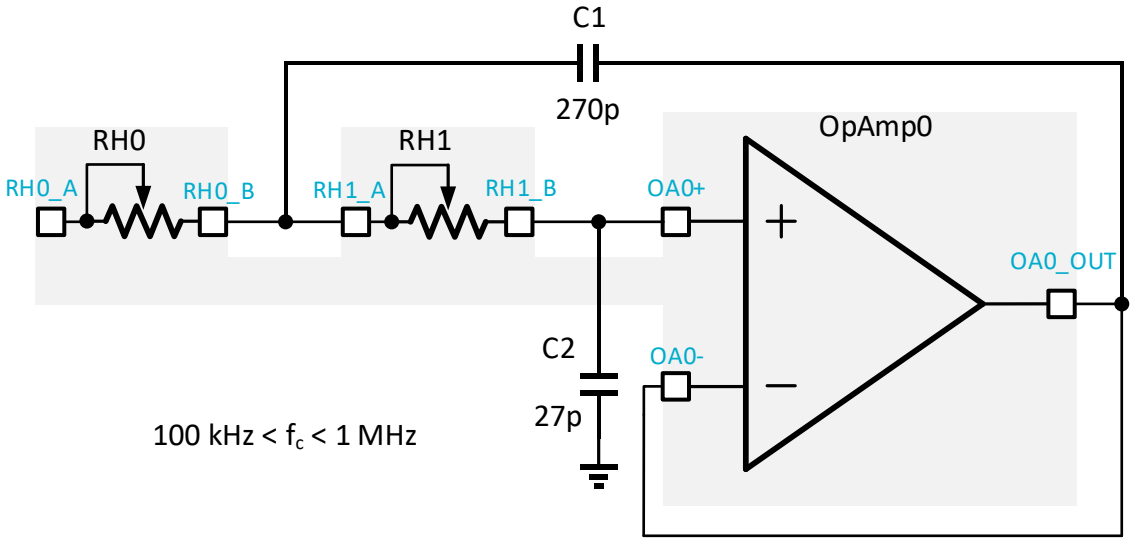

Figure 2: Sallen-Key Filter Based on the SLG47004

By adjusting two Digital Rheostats the cutoff frequency and the approximation method of this active filter can be changed. The Butterworth approximation method was used in this application note. The

frequency behavior of the Butterworth filter is maximally flat in the magnitude response in the passband. The rate of attenuation in the transition band is better than the Bessel filter, though not as good as the Chebyshev filter. There is no ringing in the stopband. The step response of the Butterworth filter has some overshoot and ringing in the time domain, though this is comparatively less than the Chebyshev filter.

The equation for the low-pass filter configuration on Figure 2 is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K/(RH_1RH_2C_1C_2)}{s^2 + s(1/RH_1C_1 + 1/RH_2C_1 + 1/RH_2C_2 - K/RH_2C_2) + 1/RH_1RH_2C_1C_2}$$

where K = 1;

This formula can be used to calculate the appropriate resistance and capacitance. Alternatively, it is possible to determine the capacitors and resistors values using filter design tools [5].

The capacitor values in the filter circuit are kept constant while the resistive elements are adjusted. For this project, capacitor valuse chosen are: C1 = 270 pF and C2 = 27 pF.

The SLG47004 contains two 10-bit Digital Rheostats. The full resistance for both Digital Rheostats is 100 kΩ. The range of digital code that corresponds to the rheostat resistance is from 0 to 1023 (1024 taps). Code 0 corresponds to the minimum resistance between the RHx_A and RHx_B terminals. As the code value increases, the resistance between the RHx_A and RHx_B terminals monotonically increases. Consequently, when the code value decreases, the resistance between the RH0_A and RH0_B terminals decreases as well. The voltage on any rheostat pin can be in the range from AGND to VDDA, and can be dynamically changed during operation.

The values calculated for this filter design are summarized in Table 1. This table also includes the closest resistance values for RH0 and RH1 along with the digital program code.

Table 1: The Butterworth Filter Design Adjusting the Resistors through a Digital Rheostat

Cutoff Frequency, kHz	Calculated RH0 Value, Ω	Closest Digital Rheostat RH0 Value, Ω	Digital Rheostat RH0 Code	Calculated RH1 Value, kΩ	Closest Digital Rheostat RH1 Value, kΩ	Digital Rheostat RH1 Code
100	4400	4395	44	78.900	78.906	807
1000	440	490	4	7.890	7.910	80

5 Functional Block Architecture

Figure 3 shows the internal design of the project in GreenPAK Designer software.

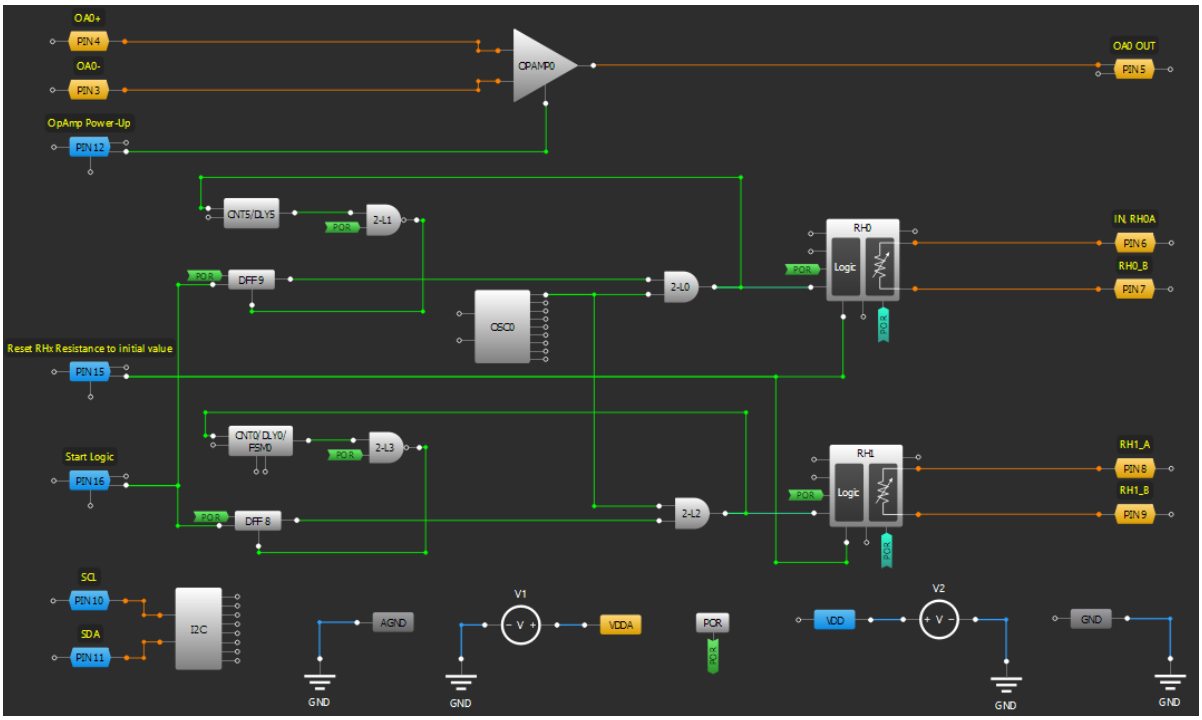

Figure 3: GreenPAK Designer Project

5.1 Setting Rheostat Data

Both rheostats allow setting "Resistance (Initial data)" in their properties and thus setting the desired filter's cutoff frequency (Figure 4).

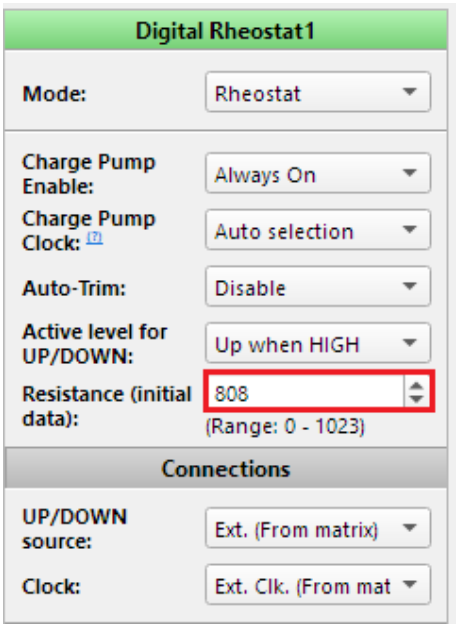

Figure 4: Digital Rheostat 1 Properties

5.2 Changing Rheostat Data

There are two ways to change Digital Rheostats value: using I²C, and using internal logic.

5.2.1 Changing Rheostat Value via I²C

The SLG47004 has an I²C macrocell, which allows reading and writing data to Digital Rheostats (Figure 5). The rheostats resistance data is stored in the registers [C0, C1] for RH0 and [D0, D1] for RH1. The I²C master can write data to these registers and thus can adjust the cutoff frequency of the filter according to the digital code in Table 1. Note that to read the rheostat data, the I²C master should read the registers [C2, C3], [D2, D3]

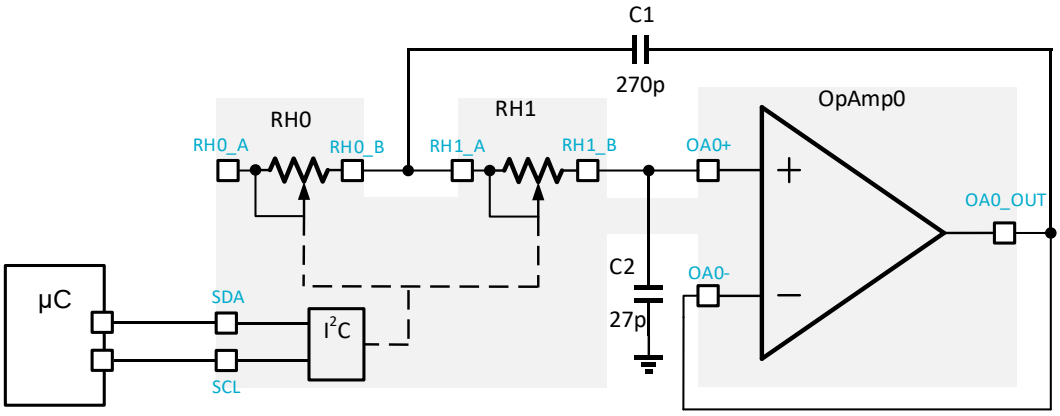

Figure 5: I²C Connection to Change Rheostats Resistance

5.2.2 Changing Rheostat Value via Internal Logic

Adjusting the cutoff frequency by I²C is a simple and convenient method, but it requires an I²C master. An alternative method can be implemented with two pins and internal logic (Figure 6).

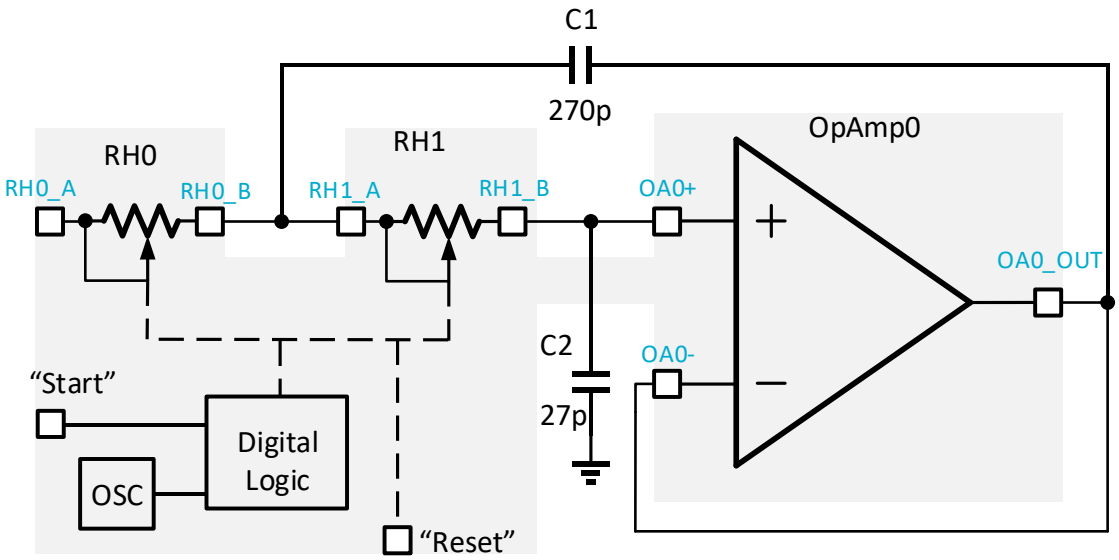

Figure 6: Internal Logic Block Diagram to Change Rheostats Resistance

A High level signal on the Start (Pin 16) and Reset (Pin 15) pins allows switching between two different frequencies. When the rheostat's initial value is set to 100 kHz cutoff frequency, the High level signal on Pin16 starts changing this frequency to 1 MHz (Figure 7). The High level signal on Pin15 resets the frequency again to 100 kHz (Figure 8).

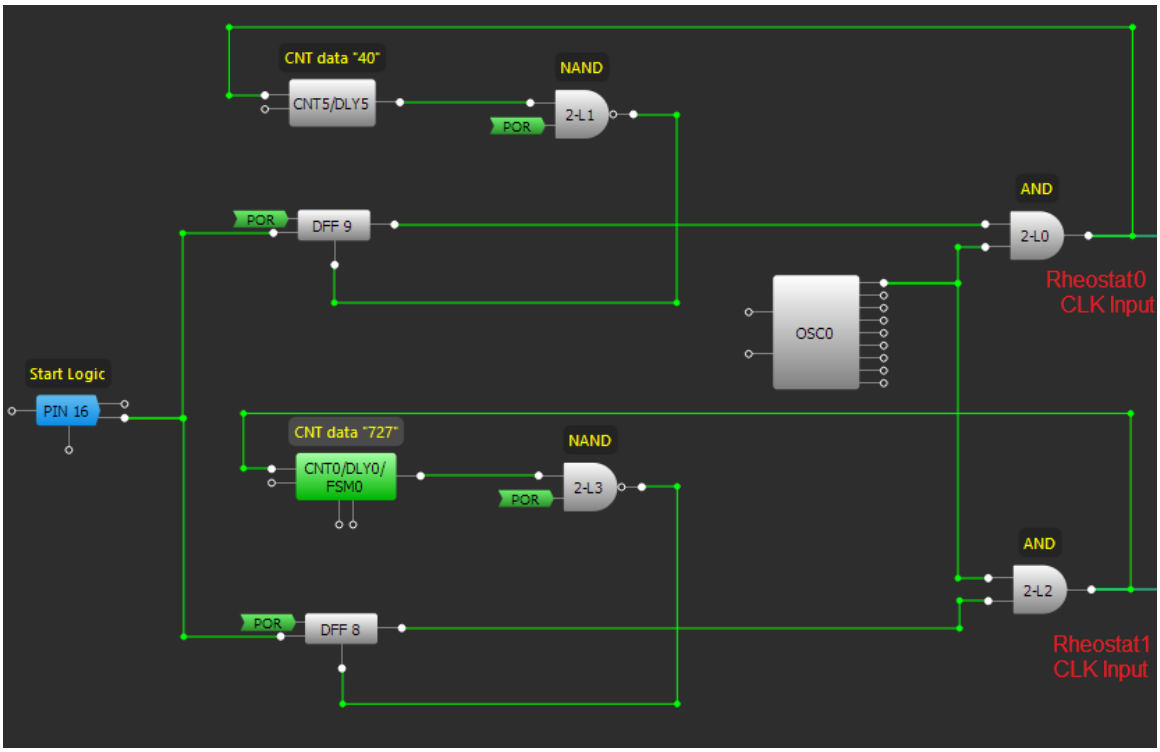

Figure 7: Internal Logic for Changing Rheostat Resistance

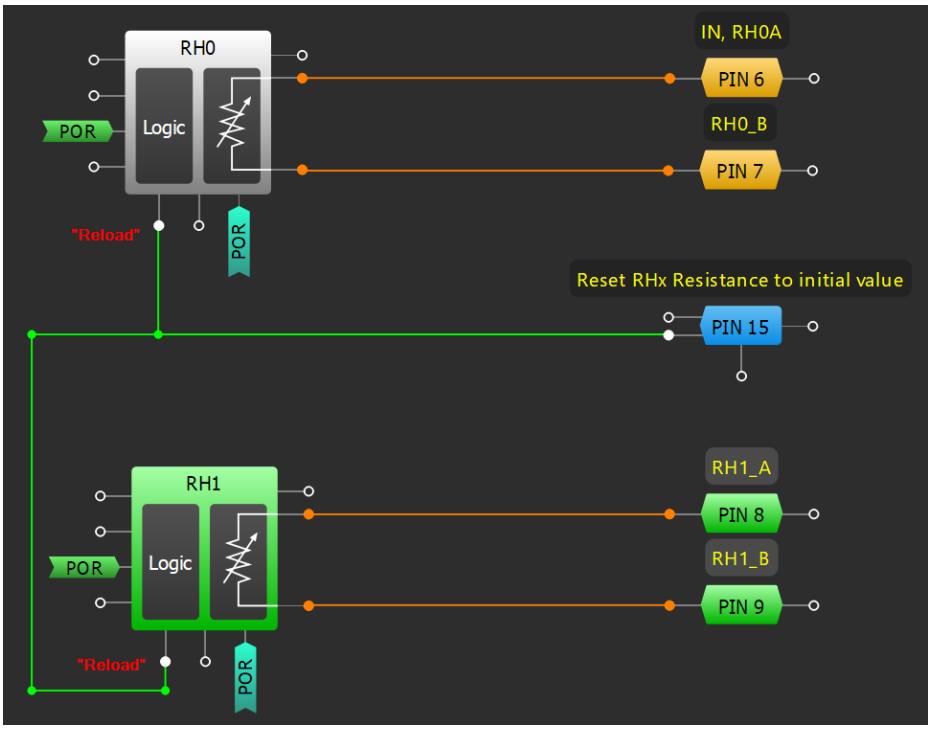

Figure 8: Rheostat Reloading Unit

To detail this behavior further, for 1 MHz cutoff frequency RH0 resistance is 488 Ω (code 4) and RH1 is 7.910 kΩ (code 80). To change the frequency to 100 kHz the RH0 resistance = 4.395 kΩ (code 44) and RH1 resistance = 78.906 kΩ (code 807). So, for RH0 the digital code value must be increased by 40 and for RH1 by 727. To increase the resistance in the rheostat's settings "Active level for UP/DOWN" must be set to "Up when High".

8-bit and 16-bit Counters can be configured to provide the necessary number of clock pulses from the oscillator to the rheostats. 8-bit Counter data must be set to "40" and 16-bit Counter to "727".

CNTs stop is provided by the internal logic (Figure 7). When "Start Logic" signal goes High, DFFs will trigger on its rising edge. A High level on DFFs outputs will cause a clock signal on LUT0 and LUT2 outputs. After that, Counters values start going down and when they reach "0" a High level will appear at LUT1 and LUT3 inputs respectively. As these LUTs are NAND gates, a High level of signals on their inputs will reset the corresponding flip-flop and will stop counting.

Software simulation results for this internal logic are shown in Figure 9. For hardware testing refer to Figure 10.

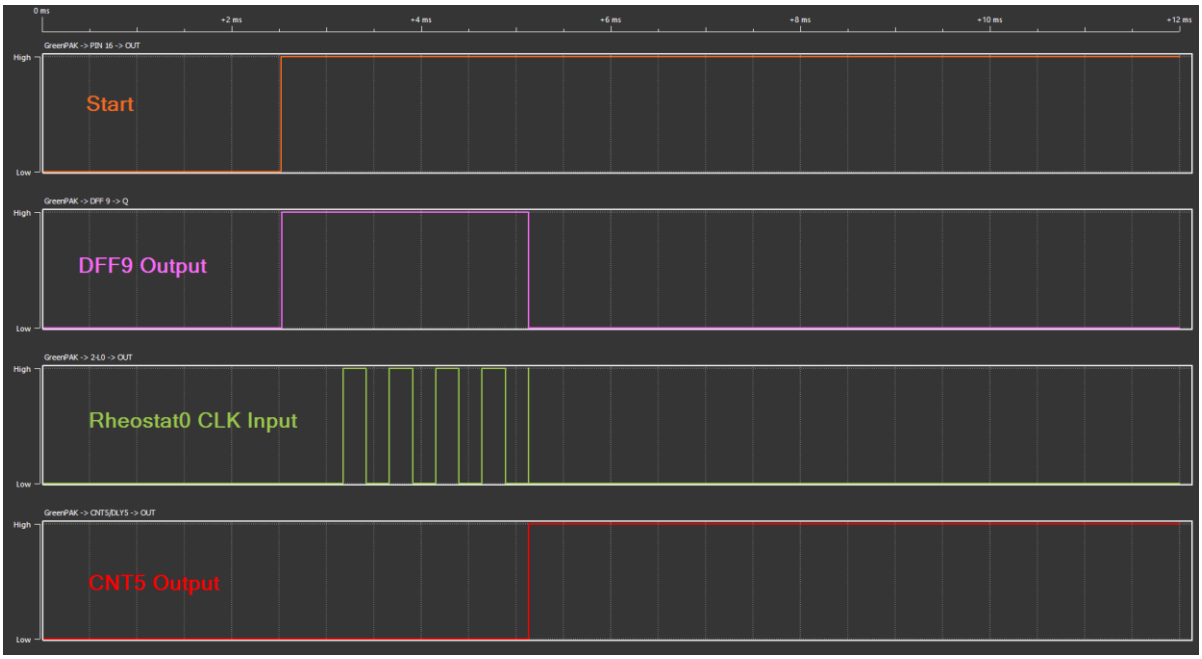

Figure 9: Software Simulation of Internal Logic at CNT5 Data = 5

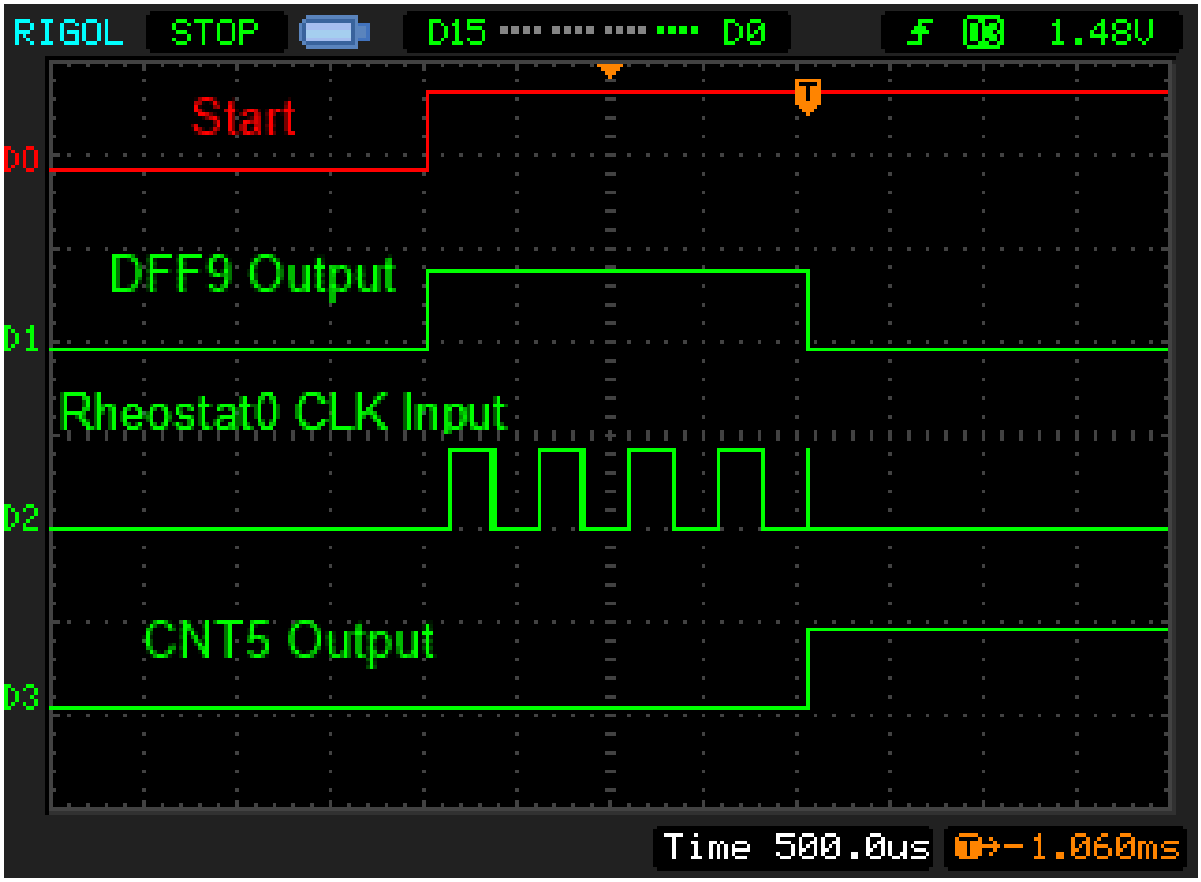

Figure 10: Hardware Testing Waveforms for Internal Logic at CNT5 Data = 5

For resetting the cutoff frequency Pin15 works as a Digital Input and is connected to "Reload" input of the rheostats. When Reload signal goes High, the rheostat value stored in the MTP NVM will be loaded into the rheostat (Register and Counter) overwriting any current setting. For the normal rheostat operation "FIFO nReset" input should have a logic High level (Figure 7).

5.3 Macrocells Settings

Table 2: LUTs Settings

IN1	IN0	2-bit LUT0 OUT	2-bit LUT1 OUT	2-bit LUT2 OUT	2-bit LUT3 OUT
0	0	0	1	0	1
0	1	0	1	0	1
1	0	0	1	0	1
1	1	1	0	1	0

Table 3: DFFs Settings

Properties	DFFs 8, 9
Type	DFF/LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low

Properties	DFFs 8, 9
Q output polarity	Non-Inverted (Q)
Active level for RST/SET	Low Level

Table 4: PINs Settings

Properties	PINs 3, 4, 5, 6, 7, 8, 9	PINs 10, 11	PINs 12, 15, 16
I/O selection	Analog input/output	Digital input	Digital input
Input mode	Analog input/output	Digital in without Schmitt trigger	Digital in without Schmitt trigger
Output mode	Analog input/output	None	None
Resistor	Floating	Floating	Pull Down
Resistor value	Floating	Floating	100 kΩ

Table 5: OpAmp Settings

Properties	OpAmp0
Mode	OpAmp Mode
Bandwidth Selection	8 MHz
Charge Pump	Enable CP
Supporting Blocks On/Off	Follows OpAmp
Vref Connection	Disconnected

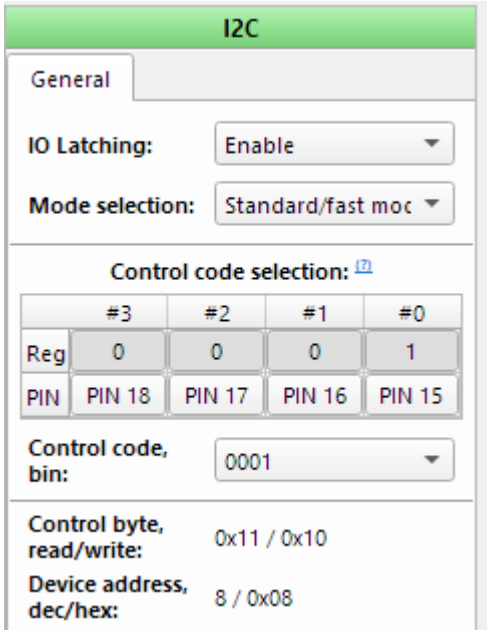

Figure 11: I²C Settings

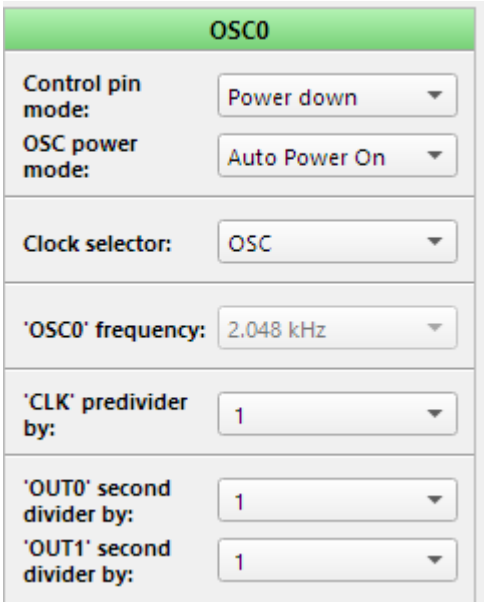

Figure 12: OSC Settings

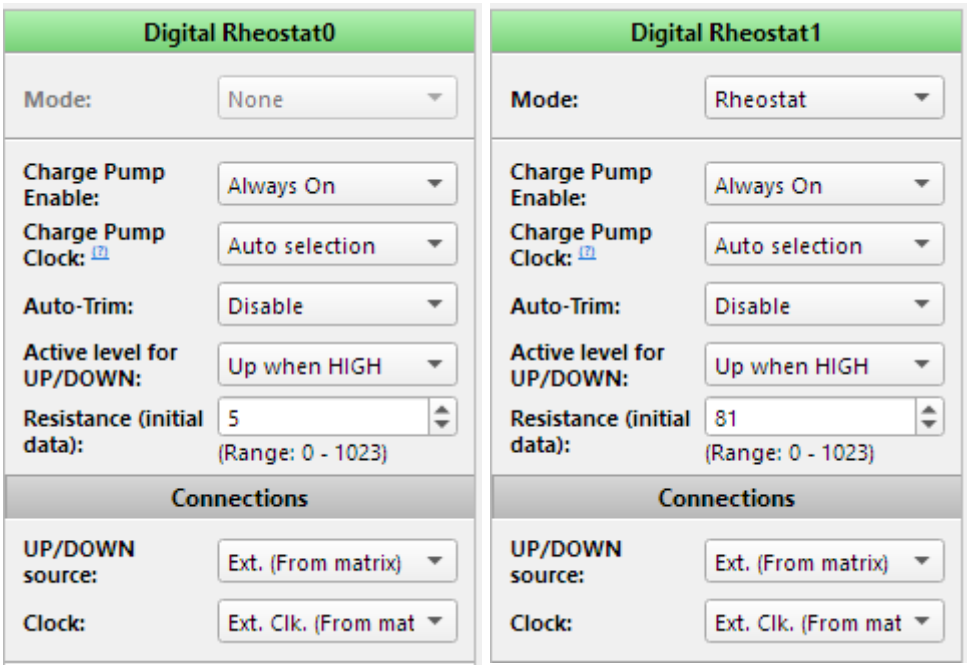

Figure 13: Digital Rheostat Settings for 1 MHz Cutoff Frequency

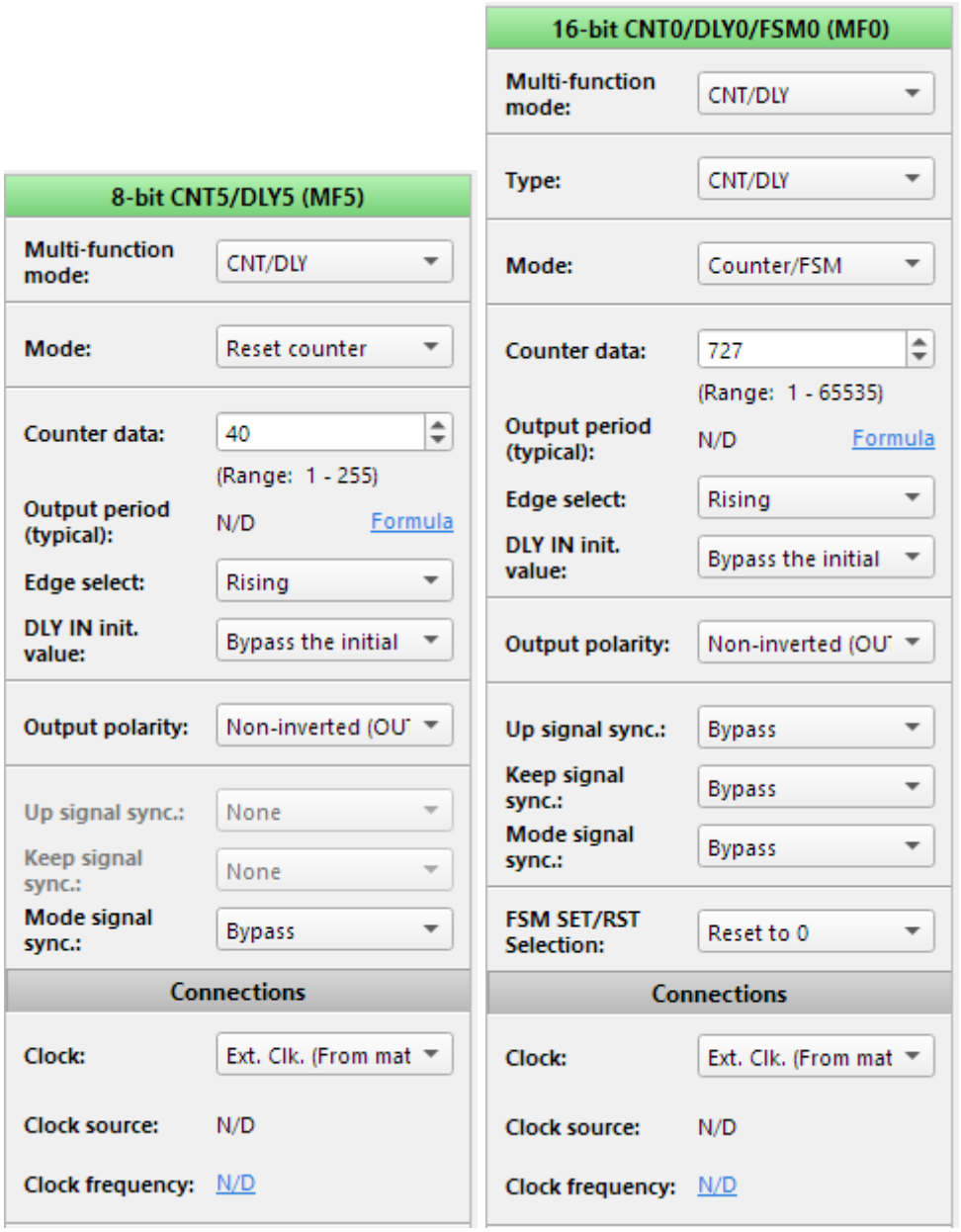

Figure 14: Counter Settings

5.4 Software Simulation

The frequency response of the second-order, active low-pass Sallen-Key filter (for 100 kHz and 1 MHz corner cutoff frequencies) is shown in Figure 15.

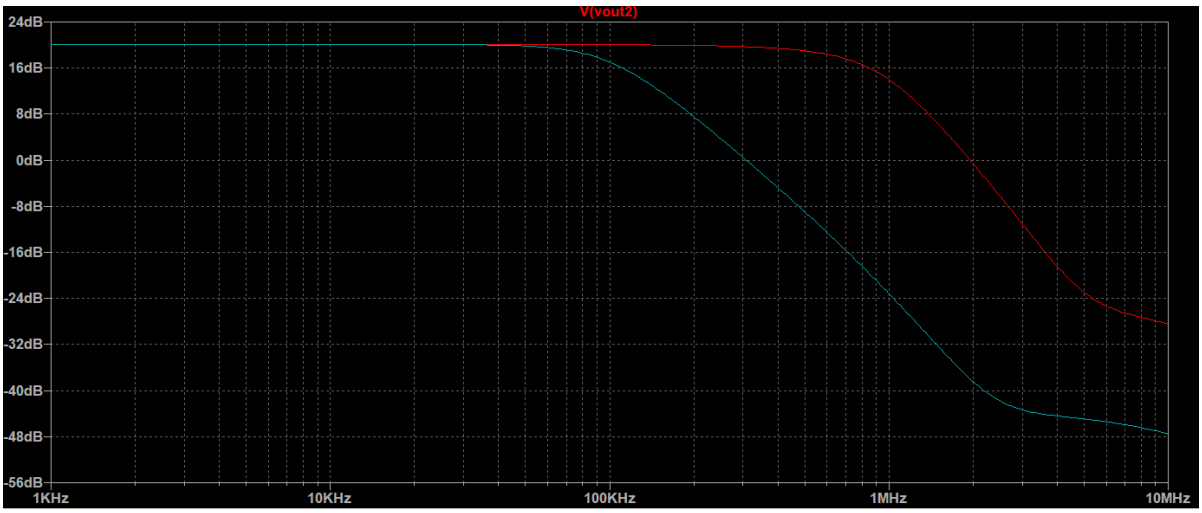

Figure 15: Simulated Frequency Response of Filter for Two Cutoff Frequencies

5.5 Hardware Testing

Results of prototype testing for both cutoff frequencies are shown in Figure 16.

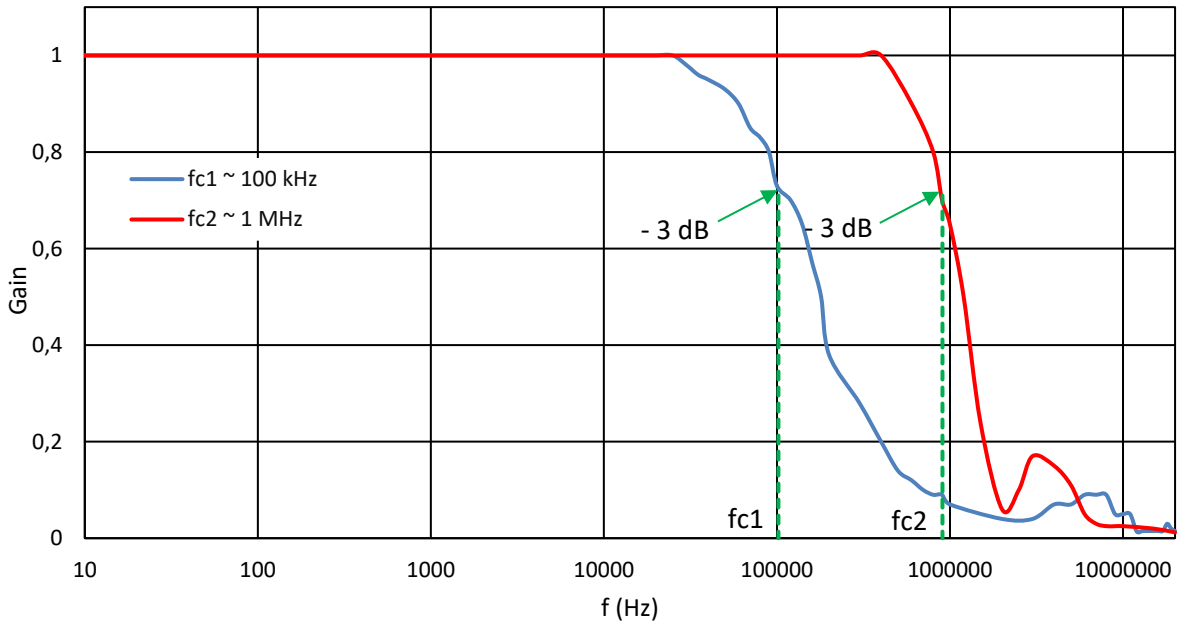

Figure 16: Frequency Response of Prototype Filter for Two Cutoff Frequencies

Conclusions

The SLG47004 has the necessary internal resources to implement advanced analog features. This application note illustrates how to implement an adjustable analog filter as a functional replacement of multiple standard products. Using one tunable analog filter for different cutoff frequencies provides a more flexible, cost-efficient solution that yields a smaller PCB footprint and lower power consumption. Due to the configurable nature of the SLG47004, this application note's approach can be easily expanded for augmented functionality, such as adjusting other filter requirements like the filter approximation method.

Revision History

Revision	Date	Description
1.0	18-Nov-2020	Initial Version

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