

# Application Note

## Tracking ADC

### AN-CM-309

#### Abstract

*This application note describes the implementation of a simple tracking ADC based on digital rheostats of the SLG47004. No external components and no special tuning procedure are required for the proposed ADC structure. Also, the circuit has much better PSRR and temperature drift than a capacitor based counter type ADC.*

*The proposed ADC can be used for monitoring slow-changing signals like temperature, battery voltage, and others.*

*This application note comes complete with design files which can be found in the References section.*

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## 1 Terms and Definitions

ACMP	Analog comparator
ADC	Analog to digital converter
DAC	Digital to analog converter
IC	Integrated circuit
OpAmp	Operational amplifier

## 2 References

For related documents and software, please visit:

[GreenPAK™ Programmable Mixed-Signal Products | Renesas](#)

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

- [1] [GreenPAK Designer Software](#), Software Download and User Guide
- [2] [AN-CM-309 Tracking ADC.gp](#), [GreenPAK Design File](#)
- [3] [GreenPAK Development Tools](#), [GreenPAK Development Tools Webpage](#)
- [4] [GreenPAK Application Notes](#), [GreenPAK Application Notes Webpage](#)
- [5] SLG47004, Datasheet

Author: Vladyslav Kozlov

## Tracking ADC

### 3 Introduction

The growing development of digital ICs like microcontrollers, microprocessors, FPGA, and others, allows using complex digital processing techniques instead of analog signal conditioning. This tendency made ADC a widely used component of mixed-signal circuits.

There are a lot of types of ADC: successive-approximation ADC, sigma-delta ADC, direct-conversion ADC, capacitor charge/discharge based ADC, ADC with voltage-to-frequency converters, and others. All these ADC types have different accuracy, frequency, and cost characteristics. The proposed structure of ADC is the tracking ADC.

### 4 Tracking ADC Principle

The main components of the tracking ADC are:

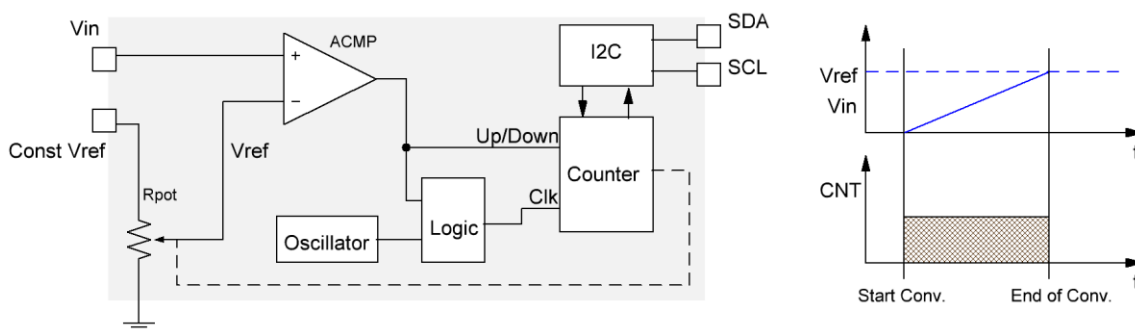
- DAC. Current project uses buffered voltage reference output and digital potentiometer as DAC.
- ACMP.
- Counter with Up/Down control input. In the SLG47004 this counter is embedded into the digital rheostats macrocells.

The operation principle of the tracking ADC is shown in [Figure 1](#). When conversion starts, the counter begins to change the resistance of digital potentiometer depending on the level at Up/Down input. At each (Oscillator) step the voltage at the inverting input of ACMP increases (or decreases). The conversion ends when ACMP changes its output. After the end of the conversion it's possible to calculate sampled input voltage:

$$V_{in} = \frac{V_{ref}}{N_{taps}} \cdot N,$$

where  $V_{in}$  – input voltage at inverting input of ACMP;  $V_{ref}$  – reference voltage;  $N_{taps}$  – maximum number of potentiometer taps;  $N$  – the value of counter after the end of conversion.

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**Figure 1: Basic Structure and Operation Principle of the Tracking ADC**

[Figure 2](#) shows the internal design of the tracking ADC based on the SLG47004.

Pulse at “Start Conversion” input begins conversion process. There are two options for initial rheostats value:

- If “Auto-Reload” input is floating, every new conversion starts from the rheostats default value of 512. This default value corresponds to  $V_{ref}/2$  voltage at dividers output.
- If “Auto-Reload” input is connected to ground, every new conversion starts from the previous rheostat value. This option can speed up the conversion time for slow-changing processes.

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The stop condition occurs when ACMP changes its input from Low to High the 3<sup>rd</sup> time.

The User can hold a logic level High at “Start Conversion” input to track input voltage level. In this case the rheostat will keep on switching and changing Vref voltage near Vin voltage level. Note that “In Progress/Done” output will change its level to logic Low after ACMP changes its input from Low to High the 3<sup>rd</sup> time, even if logic level High is being kept at the “Start Conversion” input.

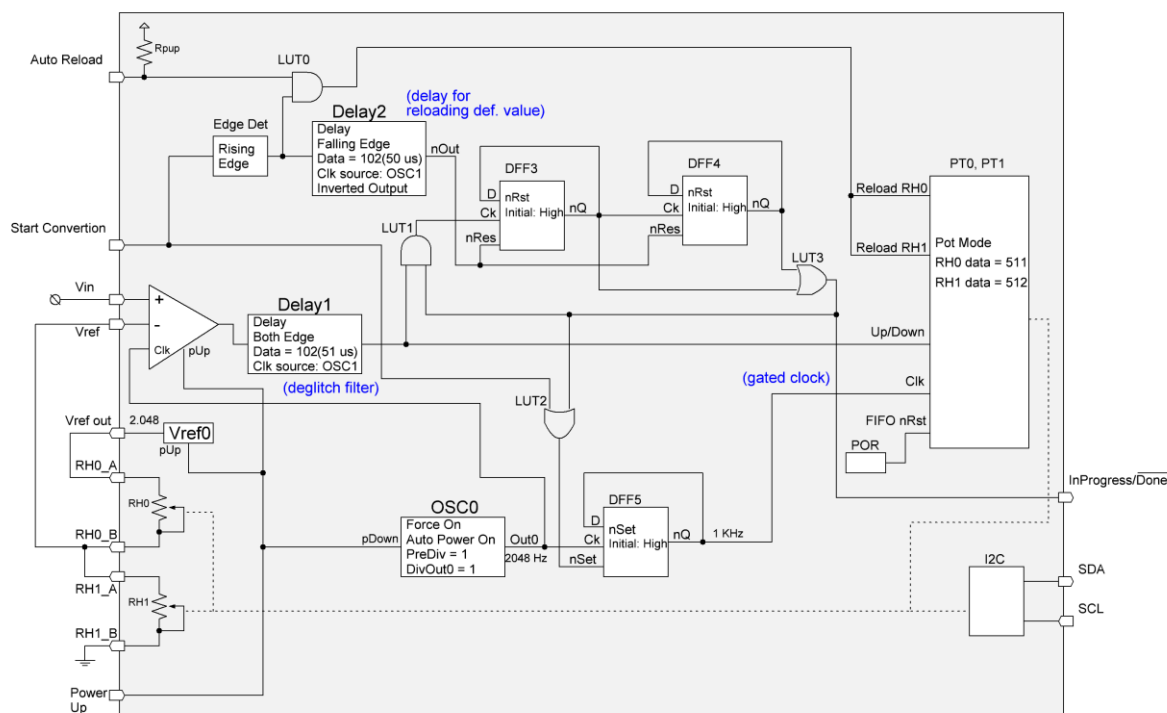


Figure 2: Internal Design of the Tracking ADC Based on SLG47004

5 Internal Blocks Configuration

Figure 3 shows the design of the project in GreenPAK Designer Software.

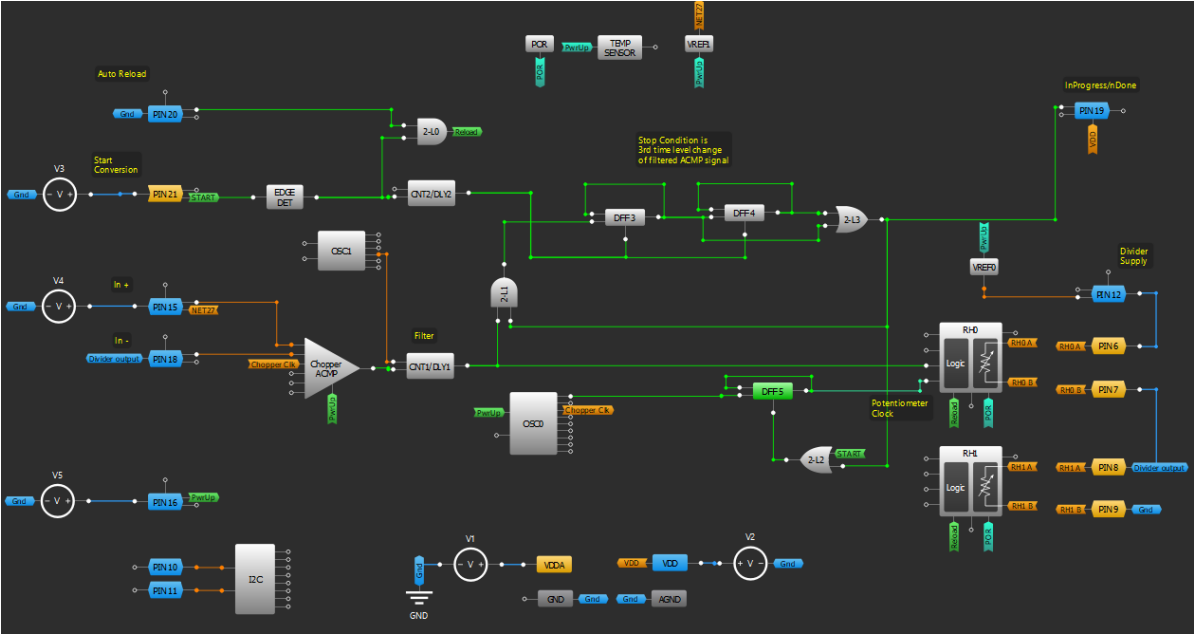


Figure 3: Project Design in GreenPAK Designer Software

5.1 Chopper ACMP Configuration

Chopper ACMP	
OUT polarity:	Non-inverted (OU <sup>+</sup> )
IN- Vref source:	HD buffer
Auto-Trim Channel:	Channel0
Auto-Trim:	Disable
Channel 0	
IN+ CH0 source:	Ext. Vref (PIN 15 (G
IN- CH0 source:	Ext. Vref (PIN 18 (G
CH0 clock:	OSC0
Channel 1	
IN+ CH1 source:	InAmp OUT
IN- CH1 source:	Ext. Vref (PIN 18 (G
CH1 clock:	Ext. Clk. (From mat

Figure 4: Chopper ACMP Configuration

## 5.2 Oscillators Configurations

OSC0	OSC1
Control pin mode: Force on	Control pin mode: Power down
OSC power mode: Auto Power On	OSC power mode: Auto Power On
Clock selector: OSC	Clock selector: OSC
'OSC0' frequency: 2.048 kHz	'OSC1' frequency: 2.048 MHz
'CLK' predivider by: 1	'CLK' predivider by: 1
'OUT0' second divider by: 1	'OUT0' second divider by: 1
'OUT1' second divider by: 1	'OUT1' second divider by: 1

Figure 5: Oscillators Configurations

## 5.3 Digital Rheostats Configurations

Digital Rheostat0	Digital Rheostat1
Mode: None	Mode: Potentiometer
Charge Pump Enable: Always On	Charge Pump Enable: Always On
Charge Pump Clock: LPBG chopper OSC	Charge Pump Clock: LPBG chopper OSC
Auto-Trim: Disable	Auto-Trim: Disable
Active level for UP/DOWN: Up when LOW	Active level for UP/DOWN: Up when HIGH
Resistance (initial data): 511 (Range: 0 - 1023)	Resistance (initial data): 512 (Range: 0 - 1023)
<b>Connections</b>	
UP/DOWN source: Ext. (From matrix)	UP/DOWN source: Ext. (From matrix)
Clock: Ext. Clk. (From mat)	Clock: Ext. Clk. (From mat)

Figure 6: Digital Rheostats Configurations

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## 5.4 LUTs Configurations

Figure 7 displays the configuration interface for four 2-bit LUTs (LUT0, LUT1, LUT2, LUT3). Each LUT configuration includes a truth table with 4 inputs (IN3, IN2, IN1, IN0) and 1 output (OUT). The configuration options for each LUT are as follows:

- LUT0 (DFF/LATCH0):** Type: LUT. Standard gates: AND. Regular shape: ☐. Invert: ☐.
- LUT1 (DFF/LATCH1):** Type: LUT. Standard gates: AND. Regular shape: ☐. Invert: ☐.
- LUT2 (DFF/LATCH2):** Type: LUT. Standard gates: OR. Regular shape: ☐. Invert: ☐.
- LUT3 (DFF/LATCH3):** Type: LUT. Standard gates: OR. Regular shape: ☐. Invert: ☐.

Figure 7: LUTs Configurations

## 5.5 DFFs Configurations

Figure 8 displays the configuration interface for three 3-bit DFFs (DFF0, DFF1, DFF2). Each DFF configuration includes settings for Mode, Second Q select, nSET/nRESET option, Initial polarity, Q output polarity, and Active level for RST/SET. The configuration options for each DFF are as follows:

- DFF0 (DFF/LATCH3):** Mode: DFF. Second Q select: Q of first DFF. nSET/nRESET option: nRESET. Initial polarity: High. Q output polarity: Inverted (nQ). Active level for RST/SET: Low level.
- DFF1 (DFF/LATCH4):** Mode: DFF. Second Q select: None. nSET/nRESET option: nRESET. Initial polarity: Low. Q output polarity: Inverted (nQ). Active level for RST/SET: Low level.
- DFF2 (DFF/LATCH5):** Mode: DFF. Second Q select: None. nSET/nRESET option: nSET. Initial polarity: High. Q output polarity: Inverted (nQ). Active level for RST/SET: Low level.

The 'Information' section for each DFF provides a truth table and operational notes:

**Normal operation**

D	CLK	Q(t)	nQ(t)
0	↑	0	1
0	↓	t - 1	t - 1
1	↑	1	0
1	↓	t - 1	t - 1

t - 1 - previous state;  
nRESET = 0 => Q = 0; nQ = 1;  
nRESET = 1 => normal operation;  
nSET = 0 => Q = 1; nQ = 0;  
nSET = 1 => normal operation;

Figure 8: DFFs Configurations



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## 5.6 Filter/Edge Detector Configuration

FILTER/EDGE DET	
Type:	EDGE DET
Mode:	Rising edge detec
Output polarity:	Non-inverted (OU)

Figure 9: Filter/Edge Detector Configuration

## 5.7 Vref0 Configuration

To configure the Vref0 macrocell, the ACMP0L should also be configured.

A CMP0L	VREF0
Hysteresis: 0 mV	Power down source: From matrix
IN+ gain: Disable	Power down register: Disable
Input LPF: Disable	Force bandgap on: Enable
Vref LPF: <a href="#">[?]</a> Disable	Source selector: A CMP0L reference
Low power start up: Disable	
Sampling mode: Disable	
Vrefs source selection: 2.048 V	
Connections	
IN+ source: OpAmp0 Out	Output: PIN 12 (GPIO0)
IN- Low to High source: 2048 mV	
IN- High to Low source: 2048 mV	
Information	
Typical ACMP thresholds	
V_IH (mV)	V_IL (mV)
2048	2048

Figure 10: ACMP0L and Vref0 Configurations

## 5.8 IO Pins Configurations

PIN 12 (GPIO0)	PIN 16 (GPIO2)	PIN 19 (GPIO5)	PIN 20 (GPIO6)
I/O selection: Analog input/out	I/O selection: Digital input	I/O selection: Digital output	I/O selection: Digital input
Input mode: Analog input/out OE = 0	Input mode: Digital in without OE = 0	Input mode: None OE = 0	Input mode: Digital in without OE = 0
Output mode: Analog input/out OE = 1	Output mode: None OE = 1	Output mode: 1x push pull OE = 1	Output mode: None OE = 1
Resistor: Floating	Resistor: Floating	Resistor: Floating	Resistor: Pull Up
Resistor value: Floating	Resistor value: Floating	Resistor value: Floating	Resistor value: 100K

Figure 11: IO Pins Configurations

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5.9 I<sup>2</sup>C Macrocell Configuration

I<sup>2</sup>C Macrocell uses default settings.

## 6 Design Verification Using Software Simulation and Hardware Prototype

Figure 12 shows the results of software simulation of the tracking ADC with disabled auto-reload feature. It can be seen that after a start pulse, the clock signals come to the digital potentiometer. At each clock the potentiometer changes the wiper position (the 3<sup>rd</sup> common terminal) and the reference voltage approaches the input voltage. When the reference voltage at wiper terminal becomes equal to the input voltage, the ACMP changes its level. After the 3<sup>rd</sup> rising edge of the ACMP signal the process ends. The same process is demonstrated in Figure 13.

If auto-reload feature is disabled, the process begins from the current potentiometer state. But if auto-reload feature is enabled, the digital potentiometer starts counting from the default value defined by the User. The operation of the tracking ADC with enabled auto-reload feature is shown in Figure 14.

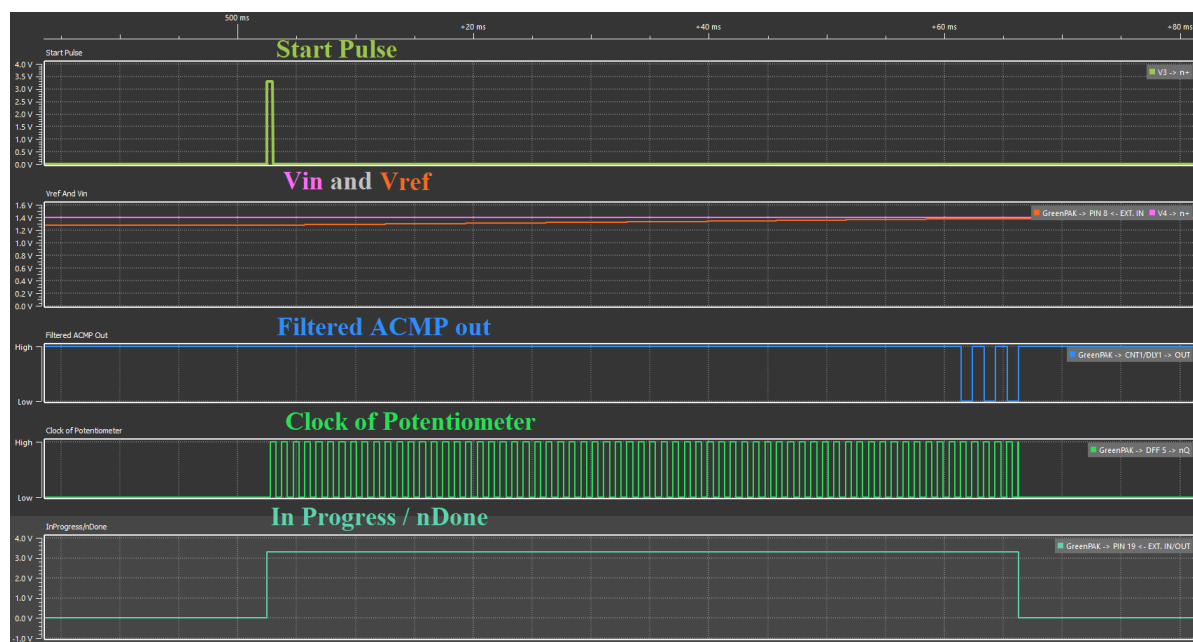


Figure 12: Software Simulation of ADC Operation with Disabled Auto-Reload Feature

## Tracking ADC

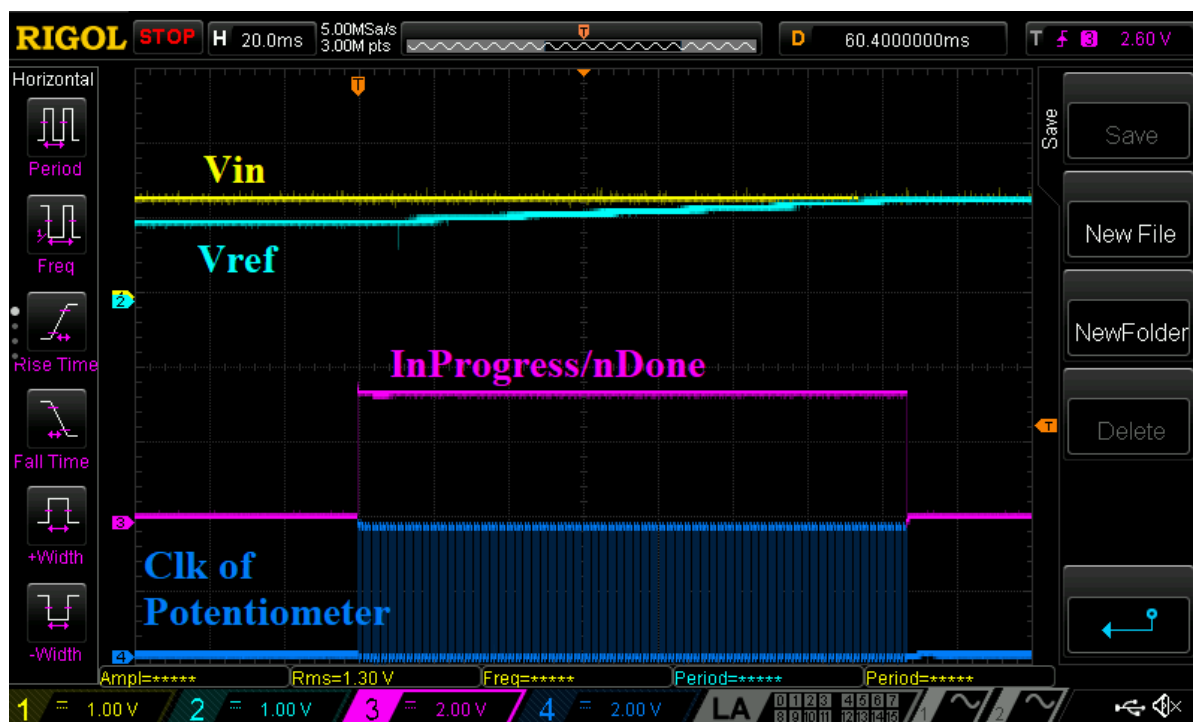


Figure 13: Waveforms of ADC Operation with Disabled Auto-Reload Feature

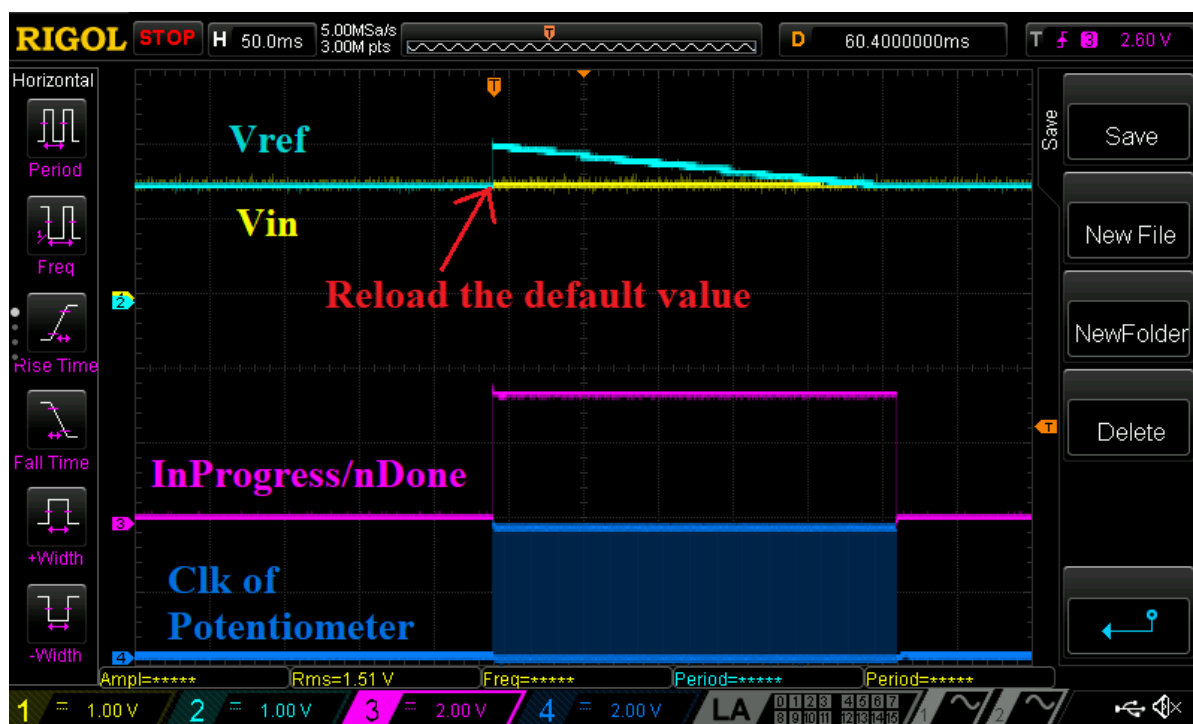


Figure 14: Waveforms of ADC Operation with Enabled Auto-Reload Feature

## 7 Accuracy and Timing Characteristics

The most essential error sources of ADC are non-linearity (DNL and INL), gain error, and offset error. The output voltage considering errors caused by the rheostats DNL and INL can be estimated using formula (1). The digital rheostats of the SLG47004 have DNL and INL =  $\pm 1$  LSB (max).

$$V_{out} = \frac{V_{ref}}{R_{RH} \pm \frac{1LSB_{INL}}{1024} R \pm \frac{2LSB_{DNL}}{1024} R} \cdot \frac{R_{RH}}{1024} \cdot \left( N \pm 1LSB_{DNL} \pm \frac{1LSB_{INL}}{1024 - N} \right), \quad (1)$$

where  $V_{out}$  – output voltage;  $V_{ref}$  – reference voltage of divider;  $R_{RH}$  – maximum rheostat resistance;  $N$  – number of bits that corresponds to sampled voltage.

According to formula (1), the maximum error caused by the rheostats DNL and INL is  $\sim 2$ LSB. The next DC error source is the input offset voltage of the comparator. In the case of 2.048 V voltage reference of divider:

$$V_{offsetLSB} = V_{offsetACMP} \frac{1024}{2.048},$$

where  $V_{offsetLSB}$  and  $V_{offsetACMP}$  – comparator offset in LSB and in volts.

In the case of Chopper ACMP  $V_{offsetLSB} = 0.15$  LSB (0.3 mV maximal offset).

The absolute value of  $V_{ref}$  is another additional error source. The  $V_{ref}$  with accuracy of  $\pm 1$  % causes a gain error of 10 LSB. Eventually, full-scale error is **12.15 LSB max**.

Note that both gain and offset errors can be easily compensated by software, unlike DNL and INL errors.

Temperature drift of the system depends mainly on the temperature drift of internal  $V_{ref}$ . It is equal to 40  $\mu$ V/ $^{\circ}$ C. It should be noted that the temperature change doesn't affect the potentiometer ratio.

Maximum time of the conversion depends on the maximum allowed switching frequency of rheostats. The switching frequency of the rheostats is 1 kHz max in regular mode. Maximum time of the conversion:  $T_{Conv} = \frac{1}{f_{max}} (512 + 5) = 0.517$ s or  $\sim 2$ Hz

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## 8 Conclusions

This application note describes the design of a simple tracking ADC based on the unique analog blocks within the SLG47004. Another popular type of ADC for the devices that don't have dedicated embedded ADC is the capacitor based or the Wilkinson ADC. The main principle of that ADC is the measurement of the time of an external capacitor charging (discharging). The comparison of these two ADC types can be found in [Table 1](#).

**Table 1: The Comparison of Tracking ADC and Capacitor Based (Wilkinson) ADC**

Parameter	Tracking ADC	Capacitor Based ADC
External components	-	One capacitor
The full-scale error without calibration, % of full range	1.2 % (max)	>10 % for mainstream capacitors >1 % for best in class ceramic capacitors
Temperature drift, ppm	20 ppm/°C	From 30 ppm/°C to 2500 ppm/°C for ceramic capacitors
Sample time, ms	517 (max)	>7 (limited by the ACMP propagation error)

The data from [Table 1](#) shows that the tracking ADC has much better accuracy performance while the Wilkinson is much faster.

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**Tracking ADC****Revision History**

Revision	Date	Description
1.0	03-Nov-2020	Initial Version

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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