Application Note

I²C Bus Multiplexer

AN-CM-285

Abstract

This app note will explain how to build a bidirectional four-channel I²C bus multiplexer circuit and will also discuss how to use the circuit as a level shifter depending on SLG46826 IC

Contents

Figures

Tables

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1 Terms and Definitions

I²C	Inter-Integrated Circuit
SDA	Serial Data Line
SCL	Serial Clock Line
LUT	Look-up table
NOR	A digital logic gate that gives a true (1 or high) output if the two inputs are 0s

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas.

Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] Go Configure™ Software Hub | Renesas, Software Download and User Guide

[2] AN-CM-285 I2C Bus Multiplexer.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG46826V, Datasheet

[6] www.i2c.info

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3 Introduction

In this app note we will clarify how to build a bidirectional 2-bit mux circuit that can be used with I²C lines. The circuit also has the extra functionality of operating as a level shifter, if needed. The design is based upon the GreenPAK SLG46826V, although any GreenPAK with I²C can work for this purpose. Due to the bidirectionality of the SDA and SCL lines, this design can be utilized for single-master or multi-master I²C communication.

The SLG46826V GreenPAK is a dual-rail IC that includes all the elements needed to construct a bidirectional multiplexer circuit suiting the I²C protocol. Use of the GreenPAK IC enables a small form factor. In addition to the already-small size to implement the I²C multiplexer circuit, the GreenPAK is also able to integrate the Oscillator and Pull-up resistors needed for the circuit.

The design has been optimized for a real world application and can be easily modified to fit the requirements of the reader's system.

It has been examined by placing it within an I²C network comprised of an Arduino board and four I²C-LCD screens, wherein each screen contains the same I²C address. Each screen was individually written-to with the help of the designed GreenPAK IC.

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4 I²C Protocol

Connecting two or more devices to transmit and receive information requires a special path of communication, controlled by a communication protocol shared by both the sender and the receiver. An Inter-Integrated Circuit bus, also known as I²C, is a very common bidirectional communication bus, using two lines to send serial information between devices.

I²C is used to create a network of communication between a controller and a set of peripherals. It has become supported by numerous electronic sensors and actuators because it's efficient and easy to route. The I²C bus supports 7-bit and 10-bit address space device and consists of two signal lines: SCL and SDA lines, which are used to communicate with the devices. The SCL stands for 'serial clock' which carries a clock signal driven by the master. The SDA stands for 'serial data', whereupon the master and slave can both send and receive data. When there is no transfer between I²C peripherals, both SCL and SDA lines are pulled up to V_{DD}.

We can connect up to 128 devices using I²C protocol, all sharing the same SCL and SDA lines. A small-scale example is shown in Figure 1.

Systems often require several different supply voltages for different ICs, and peripherals today are often linked to the microcontroller with the help of an I²C bus and an I²C level shifter or I²C-bus multiplexer to resolve compatibility.

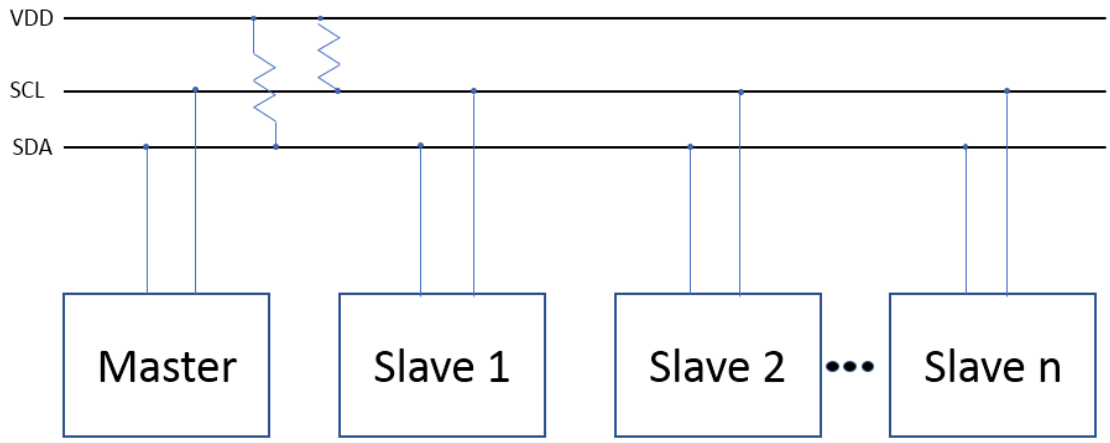

Figure 1: I²C Network Diagram

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5 I²C Bus Multiplexer

In I²C networks every device must have a unique unrepeated address to achieve communication between the master and slave correctly, but when many sensors and peripherals are combined on the same bus it may happen that the same I²C address is allocated to more than one device. To solve this problem, we implement a unique multiplexing circuit that connects slaves having the same address to the communication buses, and we may interchange channels through the polling inputs.

The I²C bus multiplexer circuit is a bidirectional selector for both buses SCL and SDA, designed using the SLG46826 dual-rail IC to build a four-channel output mux circuit as illustrated in Figure 2. The bi-directionality of the SCL line, though not required for a single-master system, ensures that the topology can be used in a multi-master configuration, wherein a primary master (attached to the left side of Figure 2) can arbitrate whether a secondary master (connected to address on the right-hand side of Figure 2) can send commands to the main I²C network.

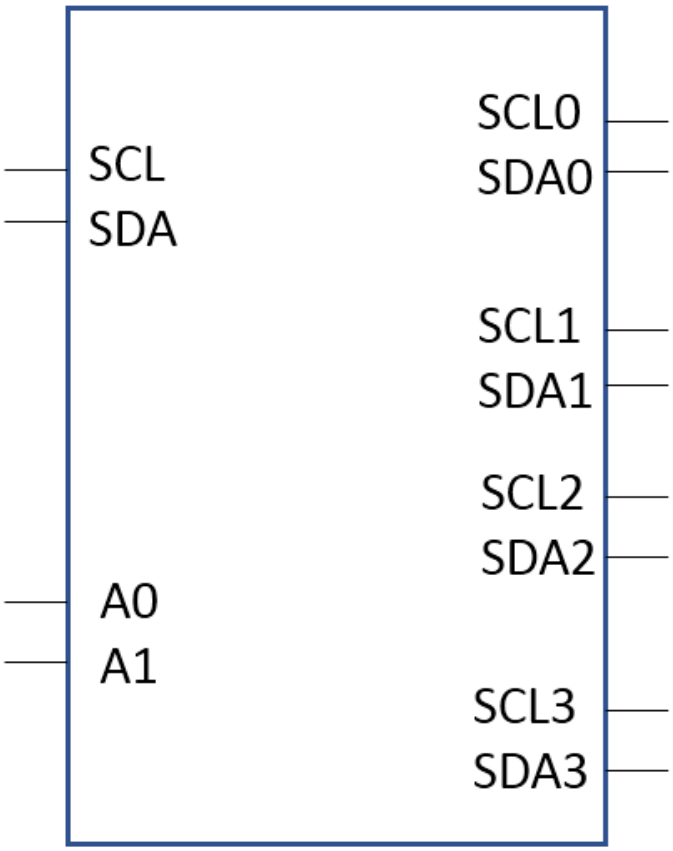

Figure 2: I²C Bus Multiplexer IC Diagram

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6 GreenPAK Design

The design consists of two main parts; the SDA line multiplexer and the SCL line multiplexer. The key behaviour of this circuit is the configuration and flexibility of the SLG46826's bi-directional pins and the OE (Output Enable) logic that configures whether a particular pin should be an input or output.

6.1 SDA Line Multiplexer

In this part, Pin 3 will be linked to one of the Pins 7, 13, 15, 16 based on the state of the inputs A0 and A1. These inputs have been configured to act as Digital input/output. The output type is Open Drain NMOS and the input is pulled up to 10 kΩ resistors. As illustrated in Figure 3 the NOR gates control OE 'Output Enable' of every pin; when OE is 'low', the pin becomes an input connected to a 10K Pull-up resistor, and when OE is at 'high', the pin becomes an output and is GND.

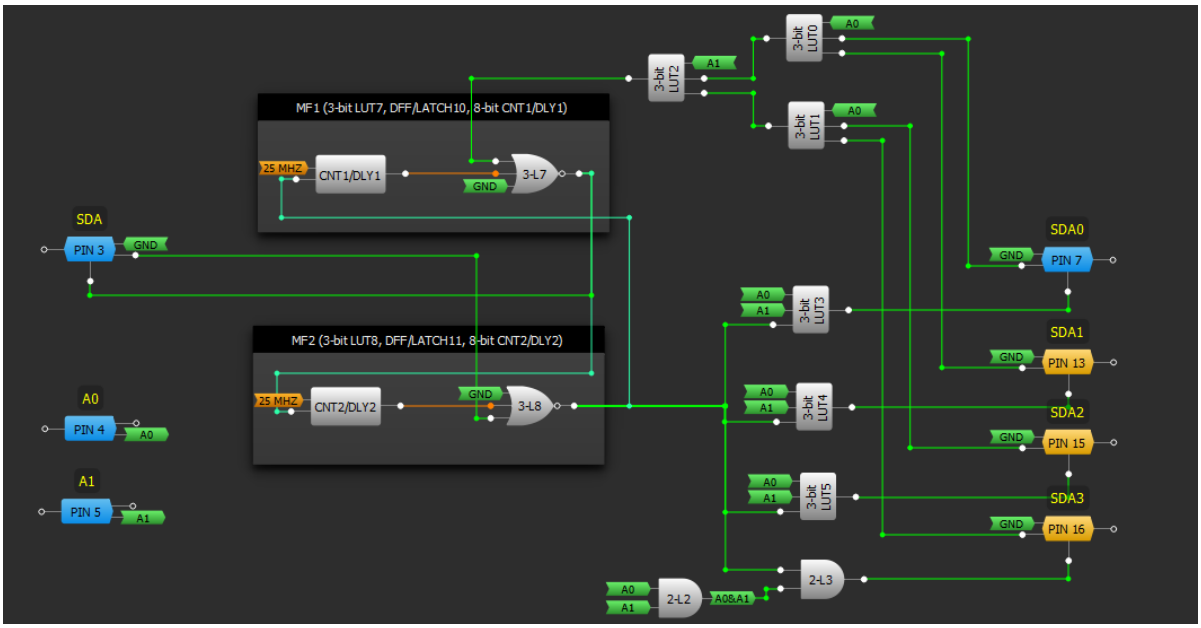

Figure 3: SDA Line Mux Design

The output of 3-bit LUT7 is linked to OE of Pin 3 while the output of 3L8 NOR gate will be multiplexed and connected to the OE of the Pins 7, 13, 15, 16. The time delay blocks were configured to operate as Falling Edge Delay and hence generate a time delay to NOR gates. 2-bit demultiplexer was built using the blocks 3L3, 3L4, 3L5, 2L2, and 2L3.

Thus, when [A1A0] = [00] the 3L8 output passes to Pin 7 and the active channel is 0 through 3L3, while the rest of the channels are inputs pulled up to 1. When [A1A0] = [01] the 3L8 output passes to Pin 13 through 3L4, when [A1A0] = [10] the output passes to Pin 15 through 3L5, and when [A1A0] = [11] the 3L8 output passes to Pin 16 through the two AND gates 2L3 and 2L2.

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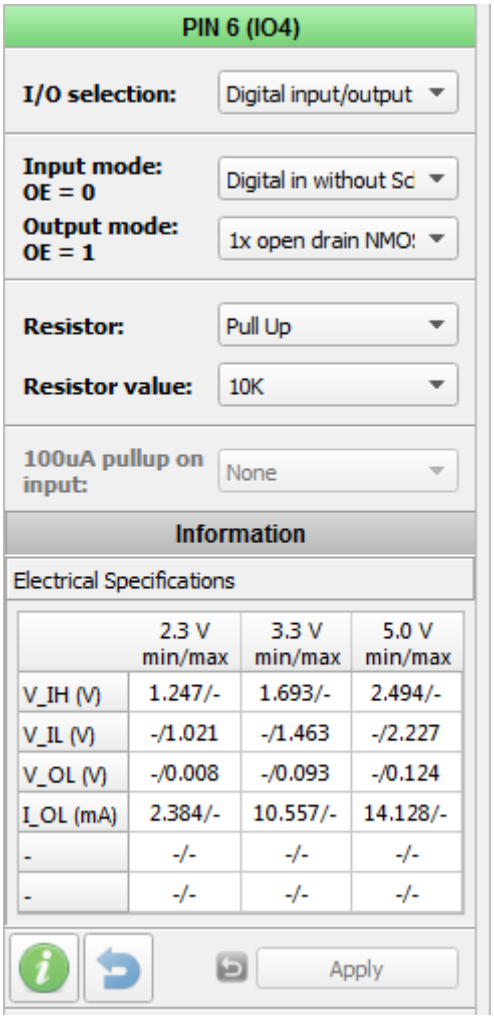

Figure 4: Pin 6 Properties

The blocks 3L0,3L1, and 3L2 were used to construct a 2-bit multiplexer circuit; it then selects one input signal coming from Pins 7, 13,15, 16 and passes it to the NOR gate in order to be later passed to Pin 3 (SDA). Pins 4 and 5 were configured to serve as inputs linked to a Pull-down resistor, then channel 0 is active as [A0A1] = [00] in the initial state.

MF1 and MF2 are multifunction blocks that can be configured to carry out more than one function. They have been employed in this design to generate a time delay, in addition, to formulate NOR gate. The 'DLY IN' input for every counter is connected to a NOR gate output.

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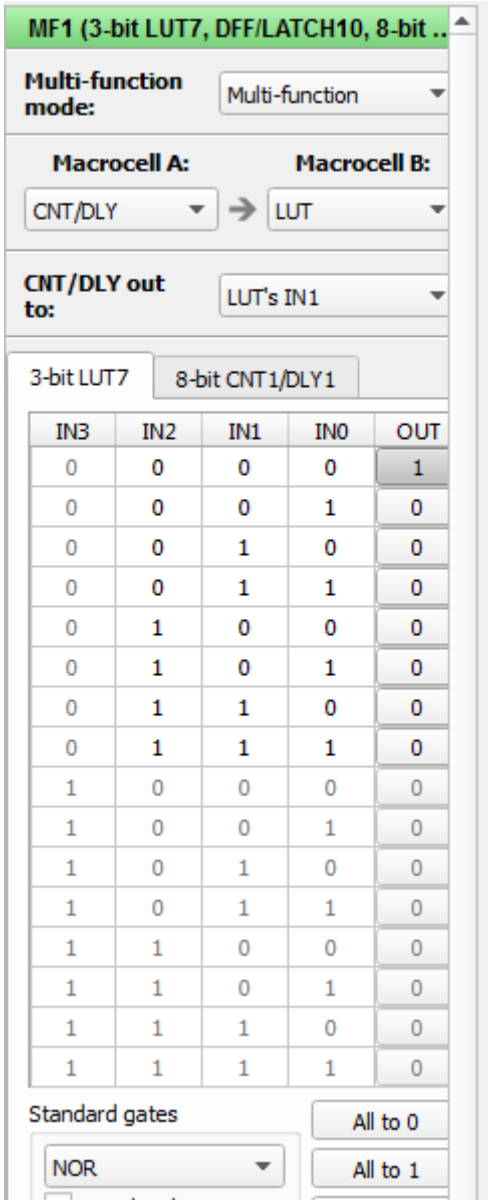

Figure 5: MF1 (Multifunction Block) Configuration

Design Sequence of Events:

When the bus is in Idle state (not transmitting or receiving) the communication pins are then linked to a Pull-up resistor (high) and all pins in an input state according to the signal passing to OE. If one of the inputs receives a LO signal, the signal is propagated through a NOR gate, causing a HI signal at the appropriate OE, based upon A0A1. This configures the pin into output and is consequently held to GND. If the input returns to HI a short time delay is generated to hold OE state to take into consideration the time the pin needs to change from LO to HI (from input to output).

To proceed with the sequence of events, consider this example:

In the initial state, there is no communication on the bus and [A1A0] = [00]. i.e. all pins are inputs, and since the Pull-up resistor is activated for the inputs, the signal HI passes into the IC from all inputs. When Pin 3 receives a LO from the master, the signal passes to 3L8, then to 3-bit LUT3 and 3L3 output is low as well for the signal low reaches OE of Pin 7 which makes Pin 7 change its state from input to output. The LO signal propagates to the external device through the bus SDA0.

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When the master releases the communication bus the input becomes HI due to the existing Pull-up resistor. The HI then passes to 3L8 which reverses the signal and passes the signal low to the OE of Pin 7, causing the pin to change its state from output to input. Since the Pull-up resistor is active, the HI is passed to the external device and a time delay is applied on the falling edge in order to give sufficient time to the pin to alter its IO state prior to receiving new values.

6.2 SCL Line Multiplexer

Like the design of the multiplexer circuit of SDA bus, another multiplexer circuit for SCL bus has been designed with the same configuration, where Pins 6, 17, 18, 19 and 20 were configured to operate as a Digital Input/Output and the internal Pull-up resistor was activated on the pins. Hence, the signal coming from the master through Pin 6 will be connected to one of the Pins 17, 18, 19 and 20 according to A1 and A0. The blocks 3L11, 3L12, 3L13, and 2L0 were used to build a 2-bit demultiplexer while the blocks 4L0, 3L6, and 2L1 were employed to construct a 2-bit mux and consequently the bi-directional communication.

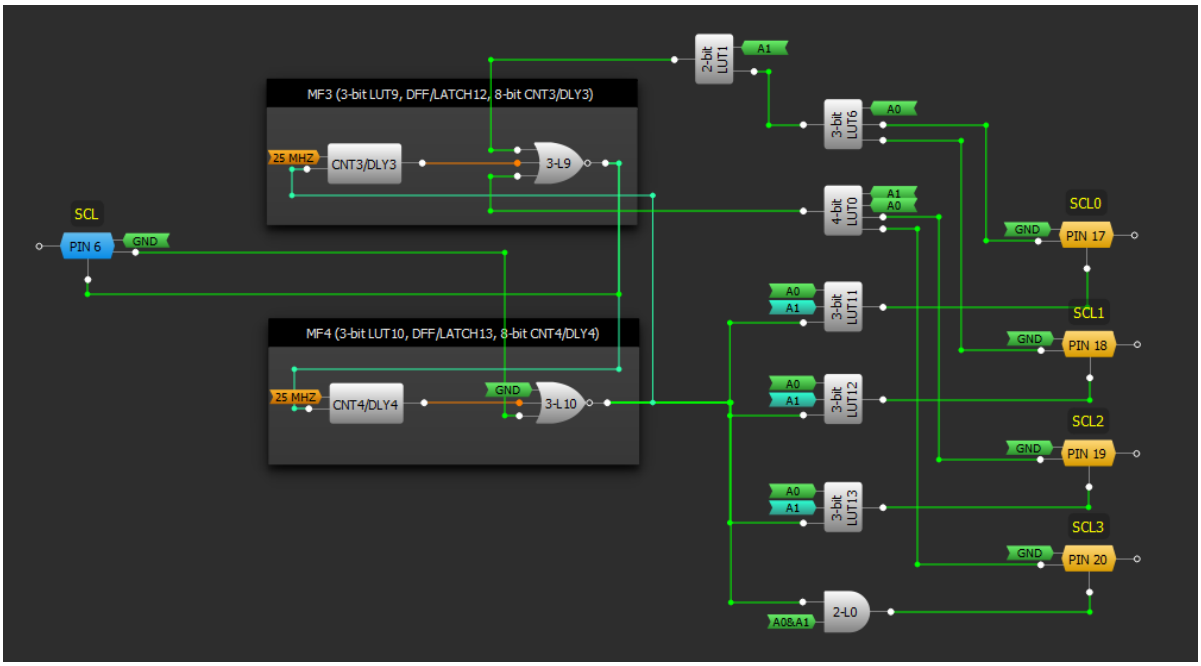

Figure 6: SCL Line Mux Design

Table 1: Selecting Inputs States

A0	A1	Enabled channel
0	0	Channel 0
1	0	Channel 1
0	1	Channel 2
1	1	Channel 3

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7 Level Shifting Feature

The SLG46826 has dual power supplies V_{DD} and V_{DD2}, which allows the design to add level shifting as another feature of the mux circuit. Pins 3, 6, and 7 are powered from V_{DD}, while Pins 13, 15, 16, 17, 18, 19, and 20 are powered from V_{DD2}. Therefore, it's possible to use this mux circuit as a level shifting circuit for channels 1, 2, 3 without channel 0. The desired voltage (V_{DD} and V_{DD2}) can be selected from project Info.

Table 2: GreenPAK Pins Map of Implemented Multiplexer

Power	GreenPAK Pin	Function		GreenPAK Pin	Function		Power
V_{DD}	3	SDA		7	SDA0	Channel 0	V_{DD}
V_{DD}	6	SCL		17	SCL0		V_{DD2}
				13	SDA1	Channel 1	V_{DD2}
				18	SCL1		V_{DD2}
				15	SDA2	Channel 2	V_{DD2}
				19	SCL2		V_{DD2}
				16	SDA3	Channel 3	V_{DD2}
				20	SCL3		V_{DD2}

8 Results

To make sure that the design is working as expected, the design was placed in a real-world scenario: to control four screens (I²C-LCD) all having the same static I²C address. All communications came from a single master, in this case, an Arduino board.

A program has been written for an Arduino board to operate as a master and print a different phrase on each screen through I²C protocol. The screens were interchanged on the buses by the I²C mux circuit and Arduino digital outputs to control A0 and A1. The buses were multiplexed between screens before every print instruction. Figure 7 depicts the screens output after implementing.

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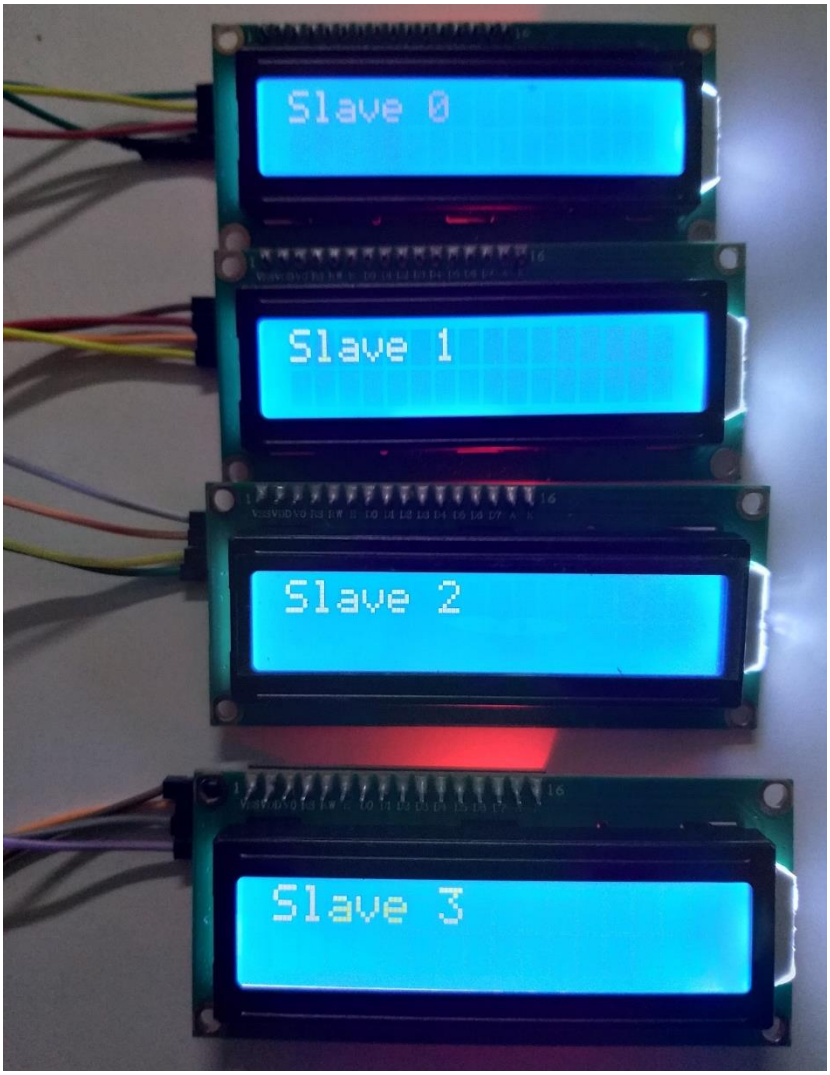

Figure 7: I²C-LCDs Outputs After Implementation

9 Conclusions

In this app note, a 2-bit multiplexer circuit has been built using an SLG46826 IC and the GreenPAK Designer Software. A level-shifting implementation is also easily realizable with the SLG46826.

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