Application Note

SLG46580/2/3 LDO Key Feature Set

AN-CM-254

Abstract

This application note introduces the key features of the SLG4658/2/3's low-dropout (LDO) regulator. These features include enable control within the GreenPAK's connection matrix, a low power mode, overcurrent limiting and short circuit detection, as well as many other features. The LDO's integration into the connection matrix provides the electrical designer with powerful tools to configure the LDO's behavior for a variety of applications. Most of the information within this document address the SLG46580 specifically, but the features described apply to the SLG46582 and SLG46583 as well.

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1 Terms and Definitions

ACMP	Analog Comparator
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
HP	High Power
IC	Integrated circuit
LDO	Low drop out
LP	Low Power
TS	Temperature Sensor

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/products/greenpak

Download our free GreenPAK™ Designer software [1]. Use the GreenPAK development tools [2] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [3] featuring design examples as well as explanations of features and blocks within the IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics

[2] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[3] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

[4] SLG46580, Datasheet, Renesas Electronics

Author: Craig Cary

3 Introduction

This application note introduces the low-dropout (LDO) regulator features of the SLG46580 GreenPAK IC. This IC integrates four configurable 150 mA LDO regulators with GreenPAK's configurable matrix, giving the designer greater flexibility to implement a wide variety of functions including the ability to customize and control power rails. The four LDOs have individually programmable voltage levels ranging from 0.9 V to 4.35 V. In addition, these LDOs feature enable control, slew rate selection, overcurrent limiting, short-circuit detection, thermal protection, input / output voltage monitoring, and low power mode selection. This application note will cover these features as well as some other useful design tips.

4 Background

LDO regulators are used to drop an input power supply voltage down to the supply voltage specifications of lower voltage ICs. A simple implementation using a PMOS transistor is shown in Figure 1. The output voltage is compared via a resistor divider to a reference voltage, and the error information is used for feedback control of the PMOS gate.

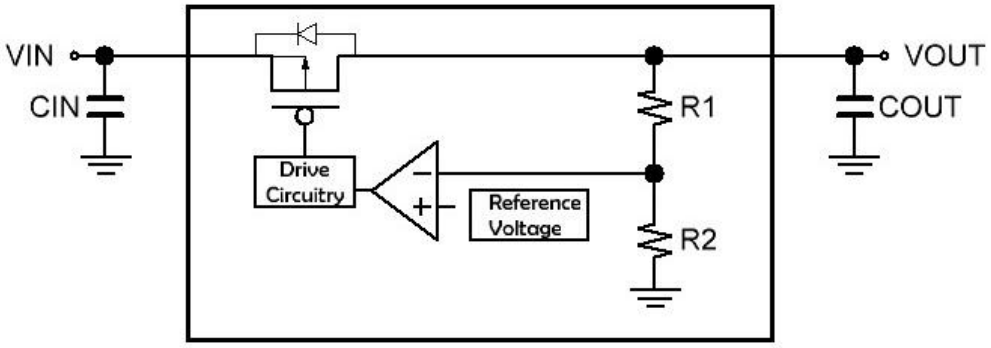

Figure 1: LDO Regulator Block Diagram

Using a PMOS transistor is one way to achieve the LDO's "low-dropout" capability. A typical non-LDO linear regulator can require 1 V of headroom from its input to its output whereas an LDO commonly requires only 200 to 300 mV. Say an LDO has a dropout voltage of 250 mV - if a designer wanted to regulate the LDO output to 3.3 V, the LDO input voltage would need to be at least 3.55 V. For the SLG46580, the dropout is spec'd at 300 mV max at full load. Note that at the lowest output voltage settings, minimum supply voltage is limited not by PMOS dropout, but simply by the minimum operational supply voltage of 2.3 V.

5 Basic LDO Functionality

The SLG46580 incorporates the configurability of GreenPAK ICs into LDOs by providing numerous programmable features. These LDOs have three modes of operation: bypass mode, high power (HP) mode, and low power (LP) mode. While LP and HP mode are both LDO regulator modes, bypass mode operates as a simple power switch connecting VIN to VOUT. Inside the LDO's property menu, you can select between "VOUT0/VOUT1" or "VOUT0/PWR switch" modes as shown in Figure 2. In "VOUT0/VOUT1" mode, you can select between regulating at VOUT0 or VOUT1 based on the LDO's VOUT0/VOUT1 matrix connection. A digital LOW will select VOUT0 while a digital HIGH will select VOUT1. Similarly, in "VOUT0/PWR switch" mode, you can select between VOUT0 and Bypass mode.

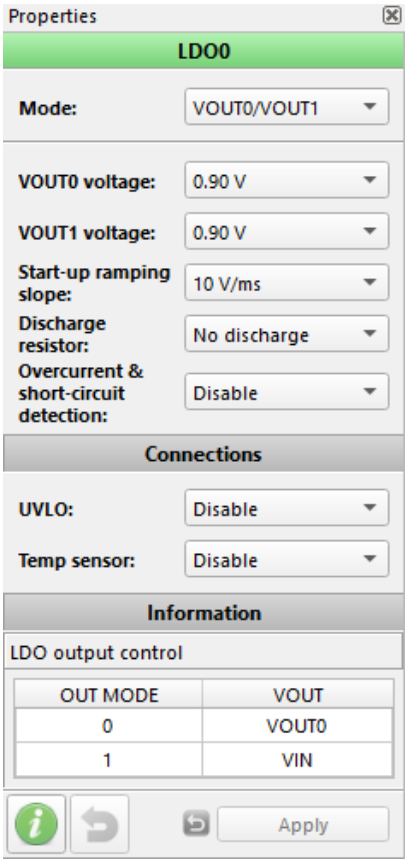

Figure 2: LDO Property Menu

In HP mode, the LDO operates in its standard 150 mA configuration. If you look at the common specifications for HP mode shown in Table 1, you can see that the quiescent current of this mode is approximately 32 µA for one LDO regulator in HP mode. As previously described, LDOs require a small dropout voltage spec'd at 250 mV typical. Please refer to the Electrical Characteristics table in the datasheet for official LDO related specifications.

Table 1: HP Mode Specifications

Symbol	Parameter	Condition / Note	Min.	Typ.	Max.	Unit
IOUT	Output Current Rating	Per LDO	--	--	150	mA
VIN	Voltage Input		2.3	--	VDD	V
VDO	Voltage Dropout		--	250	300	mV
IQ	Quiescent Current	One LDO Regulator in HP Mode	--	32	--	µA
ΔVOUT	Output Voltage Accuracy	Over PVT of VOUT > 1.5 V	-3	--	3	%
		Over PVT of VOUT ≤ 1.5 V	-60	--	60	mV

For low power applications that require less than 100 µA, LP mode can be used. In LP mode, the LDO uses a low power bandgap reference to generate the output voltage. Table 2 below shows some important LDO specifications including a 2 µA quiescent current spec for one LDO in LP mode. In addition, the dropout voltage has increased from 250 mV typical to 500 mV.

Table 2: LP Mode Specifications

Symbol	Parameter	Condition / Note	Min.	Typ.	Max.	Unit
IOUT	Output Current Rating	Per LDO	--	--	100	µA
VIN	Voltage Input		2.3	--	VDD	V
VDO	Voltage Dropout		--	500	750	mV
IQ	Quiescent Current	One LDO Regulator in LP Mode	--	2	4	µA
ΔVOUT	Output Voltage Accuracy	Over PVT	-10	--	10	%

In HP and LP modes, there are many other options that the user can configure. The designer can select an output voltage ranging from 0.9 V to 4.35 V. In addition, he or she can select the LDO output's start-up ramping slope and can connect or disconnect a 300 Ω discharge resistor to the LDO output. The following paragraphs will discuss these last two topics in a bit more detail.

5.1 Start-up Ramping Slope

The SLG46580 allows the user to select one of the following output slew rates: 1.25, 2.5, 10, and 20 V/ms. Like Renesas load switches, the slew rate control feature helps to limit inrush current to capacitive loads, thus preventing a weak power supply from drooping down to an unacceptably low voltage. To replicate a weak input source with a bench power supply, determine the effective output impedance or drive strength of your desired source and place a resistor in series between the bench power supply and the LDO inputs.

To accommodate for weak sources (IE: a coin cell), we recommend selecting a lower slew rate to limit inrush current and minimize voltage droop on the LDO's input capacitor. To use the faster start-up ramp slopes, increase the input capacitance or improve the drive strength of your input source.

5.2 Discharge Resistor

The designer can enable or disable a 300 Ω discharge resistor on each of the LDOs that connects to the LDO output when it is disabled. Depending on your application, you may or may not want to discharge the LDO outputs when it is disabled. It is important to notice that this resistor isn't connected to the LDO output when the LDO is enabled.

As previously mentioned, the SLG46580 can be configured to select between two preset voltages, VOUT0 and VOUT1. Let's say that you currently have VOUT0 and VOUT1 set to regulate to 1.5V and 2 V respectively. If you wanted to drop the LDO output voltage from VOUT1 (2 V) down to VOUT0 (1.5 V), you would need to toggle the VOUT0/VOUT1 matrix connection from high to low. You might expect the LDO output to drop instantaneously, but the LDO output is unable to sink current to pull charge off the output capacitor. If the SLG46580's LDO is disabled every time you switch voltages, you can use the internal 300 Ω resistor to sink this current, but if the LDO outputs are switched while the LDO is enabled, you will need to use an external load to discharge the output capacitor.

6 Basic Power Switch Functionality

As described in the "Basic LDO Functionality" section, the LDOs in the SLG46580 can be reconfigured as power switches. These power switches are designed to pass an input voltage directly from VIN to VOUT without regulating. The 300 Ω discharge resistor feature is available in power switch mode, but the start-up ramping slope and overcurrent limiting & short circuit detection features are unavailable.

7 Overcurrent Limiting & Short-Circuit Detection

When using the LDO in HP mode, the overcurrent limiting & short-circuit detection features can be enabled to limit the output current of the LDO to ~175 mA. If the output current is limited to 175 mA and the output voltage is less than 0.5 V, the LDOs will enter a fault state which will clamp the output current to ~20 mA. During this state, the “nFault” output of the LDO will be asserted low.

To automatically break out of this fault condition, the LDO’s output voltage must exceed 0.5 V while the LDO’s output current is clamped to ~20 mA. Through Ohm’s law, we can calculate that the minimum load resistance necessary to exceed the 0.5 V limit is 25 Ω. Through testing, we’ve observed that the LDO requires a resistive load that exceeds about 40 Ω. For resistive loads less than 40 Ω, a manual reset of the LDO through the connection matrix or I²C will be required.

When enabled in HP mode with overcurrent limiting and short-circuit detection enabled, the LDO temporarily bypasses the 20 mA current limiting feature to allow the output voltage to rise properly for high current applications. The blanking time ranges from 25 µs to 600 µs depending on the start-up ramping rate selection. In this configuration, the current will always be limited to 175 mA.

8 Thermal Protection

The SLG46580 has a built-in temperature sensor that can be used with an ACMP to disable the LDO if the chip exceeds a specified temperature threshold. The temperature sensor (TS) block produces an analog voltage that is linearly proportional to temperature. The relationship between temperature and voltage is shown in Equation (1) below.

$$V_{TS}(mV) = -4.935 * T + 1467.03 \quad (1)$$

If the TS output voltage drops below the ACMP’s IN- reference voltage and the temperature sensor is enabled in the ACMP, the ACMP output will drop low and will disable the LDO. The LDO will be automatically re-enabled when the voltage of the TS exceeds the ACMP’s IN- reference voltage.

9 Undervoltage Lockout / Power Good Monitoring

The SLG46580 ACMPs can be used to monitor the LDO input and output voltages. When connected to the LDO’s input, these ACMPs can do what is commonly referred to as undervoltage lockout. When the input voltage drops below a specified voltage, you can use the ACMP output to disable the LDO. Similarly, you can use an ACMP to monitor the output voltage of the LDOs. If the output voltage is shorted for example, you can use an ACMP to detect the output voltage falling below a certain voltage. Alternatively, when the output voltage rises above a threshold, you can enable other LDOs in a power sequencing application.

10 I2C Considerations

The I²C feature of the SLG46580 provides access to the internal registers of the LDO. These registers offer the designer additional configurability and control of the LDO’s enable, mode, selection, Vref selection, and many other settings within the LDO. Figure 3 lists some of the register locations and matrix output connections used by LDO0. For the block diagrams of the other LDOs, please refer to the “SLG46580 Low Dropout Regulators” section of the datasheet. In addition, please consult “Appendix A – SLG46580/2/3 Register Definition Package Top Marking System Definition” in the datasheet for more information on the register bits and matrix connections.

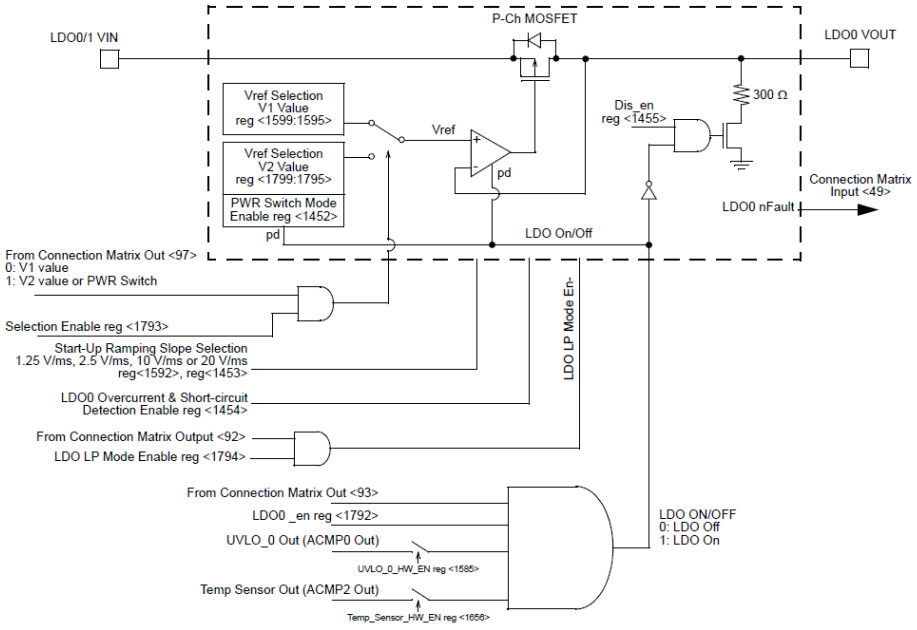

Figure 3: SLG46580 LDO0 Regulator Block Diagram

For more information on I²C, please reference AN-1090.

11 Typical Application Circuit: LDO Configuration

When designing with the LDOs inside the SLG46580, there are general guidelines that should be considered. These recommendations center around the input and output capacitors shown in Figure 4. The selection and placement of the input and output capacitors impact the LDO's input voltage droop, inrush current capabilities, turn on time, and stability.

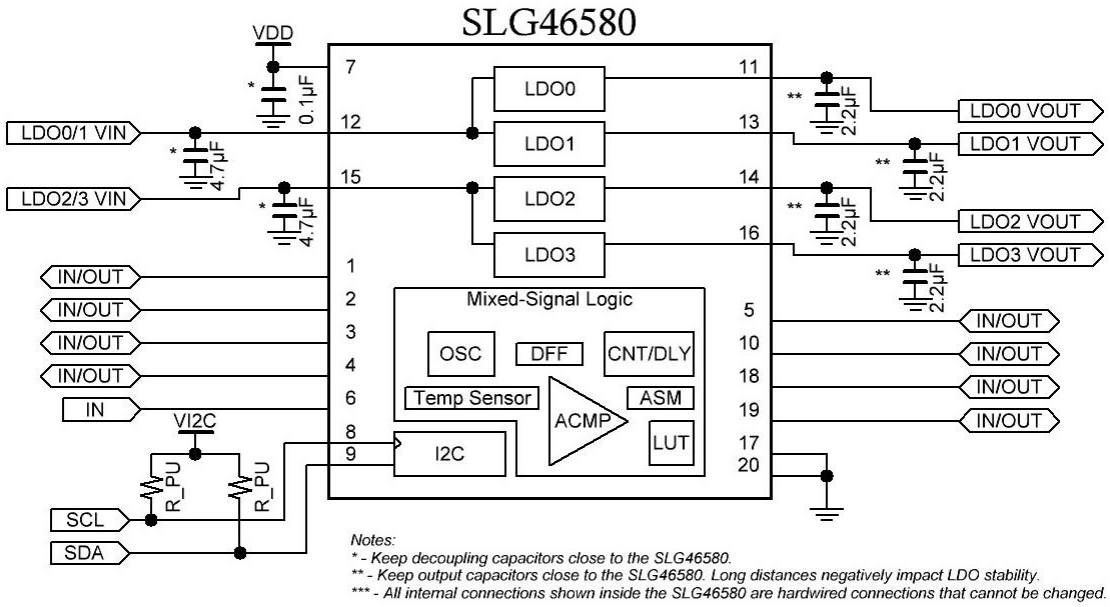

Figure 4: SLG46580 Typical Application Circuit ~ LDO Configuration

11.1 Output Capacitors:

For stable operation of an LDO within a circuit, most designs rely on a capacitor attached to the output of an LDO. This capacitance and the output's ESR (equivalent series resistance) / ESL (equivalent series inductance) introduce a zero into the phase response of the internal amplifier circuitry which helps improve the LDO's phase margin.

If the LDO's output capacitance is too small, the zero that is introduced to the system will occur past the unity gain frequency of the amplifier and will result in instability. As a result, we recommend placing a minimum of 2 µF of capacitance on each LDO output.

Similarly, if the output ESR and ESL are too big, the LDOs will become unstable. For LDO output voltages greater than 1.5 V, we recommend a maximum ESR and ESL of 20 mΩ and 2.5 nH respectively. We recommend using X5R and X7R ceramic capacitors because they have very little intrinsic ESR / ESL when compared to tantalum capacitors. By minimizing the distance between the SLG46580 LDO output pads and the capacitors, you can minimize the ESR and ESL values on the LDO outputs.

11.2 Input Capacitors:

When determining the appropriate input capacitance for a pair of LDOs (LDO0/1 or LDO2/3), start by adding the output capacitances. As a general "rule of thumb," use the sum of the output capacitances for an LDO pair as the minimum input capacitance. This recommendation is centered around the idea of charge transfer and inrush current from the LDO's input to its output when the LDO is enabled and the LDO output capacitors begin to charge.

When enabled, the LDO uses the charge stored in the input capacitor as a temporary power source until the power supply can react to the load change. If the input capacitor is too small and the start-up ramp rate is high, the current pulled from the input capacitor could cause the input voltage to droop significantly. By increasing the input capacitance, there would be a bigger pool of charge to pull from when the LDO is enabled.

There is a balance between the input voltage drive strength and the input capacitor value. Increasing the input capacitance can help with short term transient limitations, but the capacitor will be unable to source large currents to the load for extended periods of time. If the input capacitor and voltage source can't supply the inrush current required without significant voltage droop, decrease the input start-up ramp rate. For optimal performance, place the input capacitors close to the LDO input pins.

12 High-Power Recommendations

As an LDO is actively regulating, the SLG46580 can burn a significant amount of power. By using Equation (2), one can calculate the power dissipated across an LDO. The thermal limitation of the SLG46580 is limited to 600 mW at 85 °C and 800 mW at 70 °C.

$$P_{DIS} = (V_{LDO\,VIN} - V_{LDO\,VOUT}) * I_{LDO} \quad (2)$$

Since the SLG46580 is a flip chip device, the thermal conductivity for the power dissipated in an LDO is strongest though the input and output pins of the respective LDO. Therefore, by increasing the LDO input and output trace widths on the PCB, you can maximize the thermal transfer from the SLG46580 to the PCB.

13 SLG46582 and SLG46583 Behavior

The SLG46582 and the SLG46583 GreenPAK devices operate on the same principles described in this application note. The primary differences between the SLG46580 and these two IC's are the

number of LDOs and their current rating. The SLG46580 LDOs have been combined in the silicon to increase the maximum current specifications. Please see Table 3 for more information.

Table 3: LDO46580/2/3 Comparison

	LDO QTY	IMAX-per-LDO (mA)
SLG46580	4	150 mA
SLG46582	2	300 mA
SLG46583	1	600 mA

When creating the PCB layout for the SLG46582/3, please modify the typical application circuit and the high-power recommendations previously described in this application note. When externally shorting the LDO inputs and outputs together as described in the “Low Dropout Regulator(s)“ section of the datasheet, place the external shorts as close as possible to the IC. In addition, we recommend routing the combined LDO output trace from the middle of the external short. This is meant to match the output load impedance seen on each of the individual LDO output pins by minimizing the maximum distance between any LDO output pin and the load.

14 Conclusion

With four internal LDOs that can be reconfigured as power switches, the SLG46580 is perfect for low power applications that require multiple power rail voltages. By utilizing the voltage range, protection circuitry, I^2C functionality, and additional features of this IC, you can create a customized IC for use in many applications. By following the design tips and tricks provided in this application note, you now have the knowledge required to start designing with the SLG46580.

Revision History

Revision	Date	Description
1.0	29-Aug-2018	Initial Version

Revision	Date	Description
1.1	26-Aug-2019	Updated Format, Fixed Typos, Corrected the LDO Power Dissipation Equation
1.2	27-Sept-2019	Corrected GreenPAK Designer Screenshot in Figure 2

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