ClockMatrix: Selecting the Right Crystal

Introduction

The selection of a crystal for ClockMatrix™ devices is essential for optimizing performance and minimizing output jitter. This document describes the methods for selecting the right crystals for the ClockMatrix family of devices.

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1. Overview

The ClockMatrix family of devices uses a crystal as a reference for the analog PLL (APLL). All ClockMatrix outputs are synthesized from the APLL, thus the selection of crystal is essential for optimizing performance and minimizing output jitter. When selecting a crystal for a project, several crystal characteristics must be considered. The main characteristics to consider (in no order) are frequency, load capacitance, equivalent series resistance, operating temperature, frequency tolerance, aging, and drive level.

Table 1. Crystal Characteristics for ClockMatrix Devices

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Mode of Oscillation	-	Fundamental			-
Frequency	-	25	-	54	MHz
Equivalent Series Resistance (ESR)	C_L = 18pF, crystal frequency ≤ 40MHz	-	-	50	Ω
	C_L = 18pF, crystal frequency > 40MHz	-	-	25	
	C_L = 12pF	-	-	50	
Load Capacitance (C_L)	-	8	12	-	pF
Crystal Drive Level	-	-	250	-	µW

2. Frequency

ClockMatrix devices support crystals with frequencies in the range of 25MHz to 54MHz. Crystal oscillators with frequencies in the range of 25MHz to 62.5MHz may be used by enabling the doubler logic. If the doubler logic is disabled, crystal oscillators with frequencies between 50MHz and 125MHz may be used. For crystal frequencies below 62.5MHz, the use of the doubler is recommended.

For Clock Generator mode applications where the output frequency is derived from the APLL VCO frequency, to achieve lower jitter, it is recommended to select a crystal frequency that has an integer relationship to the desired output frequency.

For Jitter Attenuator mode applications where the output frequency is steered by the XO_DPLL input or a CLK input, it is recommended to avoid simple integer relationships (1:1, 1:2, 1:3, etc.) between the crystal and the output frequency. Avoiding simple integer relationships between the crystal and the output frequency reduces the likelihood of boundary spurs, which result in increased output jitter.

Commonly used crystal frequencies for ClockMatrix devices are 38.88MHz, 48MHz, 49.152MHz, 50MHz, and 54MHz.

3. Load Capacitance

For ClockMatrix devices, it is recommended that the selected crystal has a nominal load capacitance of 12pF; however, a nominal load capacitance value of 8pF, 10pF, or 18pF is also acceptable. Table 2 shows the recommended tuning capacitor values for the OSCI and OSCO pins for various load capacitance (C_L) values.

A load capacitance value smaller than specified for the crystal will slightly increase the specified crystal resonant frequency and a higher load capacitance value will slightly decrease the frequency. The frequency shift (delta f/f) has an inverse relation to C_L. For a small C_L, any change in C_L (for example from stray capacitance in the board and device) will result in a more significant change in frequency.

A smaller load capacitance may lower power dissipation in the crystal. Alternatively, a larger load capacitance will decrease the negative resistance loop gain of the oscillator and increase the drive level. For this reason, a smaller load capacitance is recommended. If the loop gain is reduced too much the oscillator may fail to start.

C_L is important to ensure reliable start-up of the oscillator. The oscillator may start up faster with a small C_L, but the oscillation may be more stable with a larger C_L.

Figure 1 shows the various capacitances that the crystal experiences. C_{S1} and C_{S2} are the stray capacitances for the first and second legs of the crystal, respectively. C_{L1} is the tuning capacitance for the first leg of the crystal and C_{L2} is the tuning capacitance for the second leg of the crystal. C_{V1} is the internal capacitance for one leg of the crystal and C_{V2} is the internal capacitance for the other leg. The load capacitance, C_L, is the $C_{S1}//C_{L1}//C_{V1}$ in series with C_{S2} //C_{L2}//C_{V2}, where "//" means "in parallel with". Therefore, the equation for the load capacitance is as follows:

$$C_L = \frac{(C_{S1} + C_{L1} + C_{V1})(C_{S2} + C_{L2} + C_{V2})}{C_{S1} + C_{L1} + C_{V1} + C_{S2} + C_{L2} + C_{V2}}$$

Table 2. ClockMatrix Recommended Tuning Capacitors for Crystal Input

Crystal Nominal C_L Value (pF)	Recommended Tuning Capacitor Value (pF) [1]	
	OSCI Capacitor (pF)	OSCO Capacitor (pF)
8	2.7	2.7
10	13	3.3
12	27	3.3
18 [2]	27	3.3

1. Recommendations are based on 4pF stray capacitance on each leg of the crystal. Adjust according to the PCB capacitance.
2. This will tune the crystal to a C_L of 12pF, which is fine when channels are running in jitter attenuator mode or referenced to an XO. It will present a positive ppm offset for channels running exclusively in synthesizer mode and referenced only to the crystal.

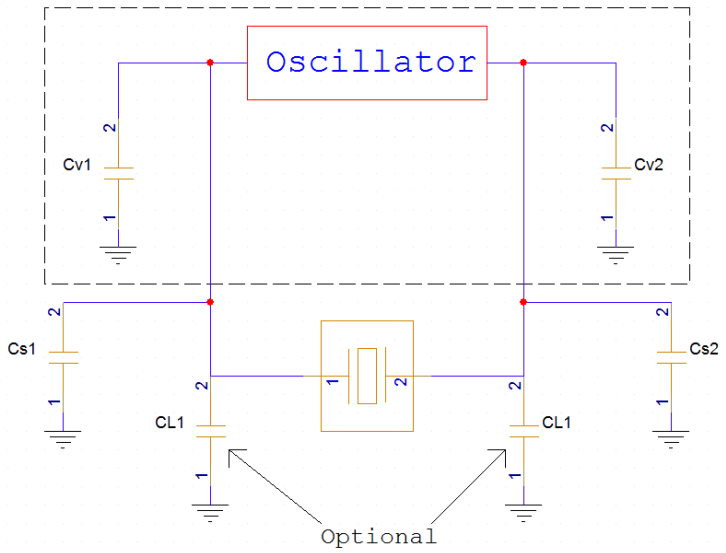

Figure 1. Crystal Capacitance

4. Equivalent Series Resistance

Equivalent series resistance (ESR) is the effective resistance component in series with the LC model of the crystal itself. ESR is determined by the crystal size, cut, frequency and mode of vibration. An AT cut crystal with a fundamental mode 50MHz resonance frequency in a 3225 package will have an ESR of around 50Ω, due to the size crystal that easily fits into this package size. ESR subtracts from the negative resistance in the oscillator. A very small package with a very small crystal may have too high an ESR for the driver, making it harder to start and sustain oscillation. A large package can fit a larger crystal (at the same cut, mode, and frequency) and will have a lower ESR.

ESR is proportional to the motional resistance (R_M) of the crystal and the shunt capacitance (C_O). It is also inversely proportional to the load capacitance (C_L). The ESR can be calculated as follows:

$$ESR = R_M \left(1 + \frac{C_O}{C_L}\right)^2$$

ESR is commonly expressed as a maximum value in ohms and is significant for 2 reasons. First, the loop gain needed for an oscillator to start up and maintain oscillation is proportional to the ESR. Secondly, the drive level of an oscillator is proportional to the ESR. Therefore, if the ESR is too large, the crystal can have trouble oscillating or the drive level can be exceeded which accelerates aging. Table 3 displays the maximum ESR values of ClockMatrix devices for several load capacitances and crystal frequencies.

Table 3. ClockMatrix Crystal ESR Recommendations Based on Load Capacitance

Parameter	Test Condition	Maximum Value (ohms)
Equivalent Series Resistance (ESR)	C_L= 18pF, crystal frequency ≤ 40MHz	50
	C_L = 18pF, crystal frequency > 40MHz	25
	C_L = 12pF	50

5. Drive Level

Confirm that the crystal maximum specified drive level will accommodate the drive level of the Clock Matrix product. For ClockMatrix products the typical drive strength is 250µW. To prevent exceeding the drive level of the crystal a series-damping resistor R_S may be added, but this series resistor will decrease the negative resistance and loop gain and will increase phase noise. It is preferred to select a crystal that can tolerate the 250µW drive strength. Adding an R_S, populated with 0 ohm shunt will allow the use of a series resistance if a suitable crystal cannot be sourced.

Exceeding the drive level of the crystal will accelerate aging. It is recommended to measure the power dissipated in the crystal, to ensure it is below the crystal maximum spec. For more information, see the Quartz Crystal Drive Level Application Note.

R_S and the two caps constituting C_L should be small surface mounted parts (example 0201 or 0402) to minimize stray capacitance. The two caps should be COG/NP0 for a lower temperature coefficient and less susceptibility to vibration and shock.

6. Using Crystal Oscillators with ClockMatrix

A crystal oscillator may be used in place of a crystal with ClockMatrix. To use a crystal oscillator with ClockMatrix, the crystal interface must be overdriven. The OSCI input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSCI input is internally biased at 1V. The OSCO pin should be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 1.8V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 2. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing to prevent signal interference with the power rail and to reduce internal noise. Please note that maximum allowable voltage on the OSCI and OSCO pins is 2.75V. Exceeding this voltage may damage the pin.

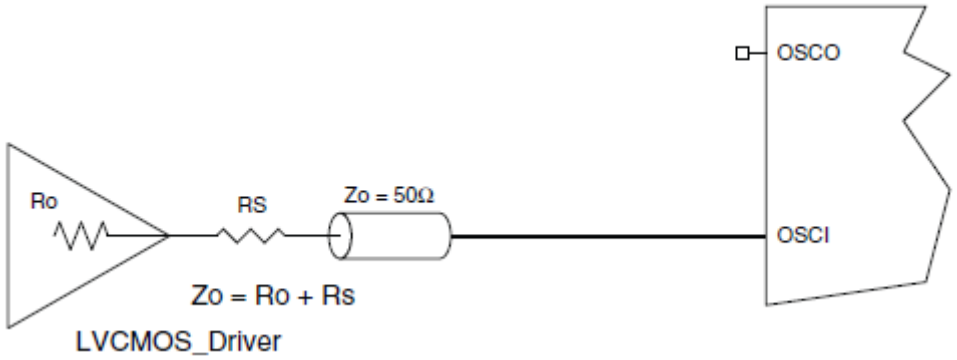

Figure 2. 1.8V LVCMOS Driver to XTAL Input Interface

Figure 3 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

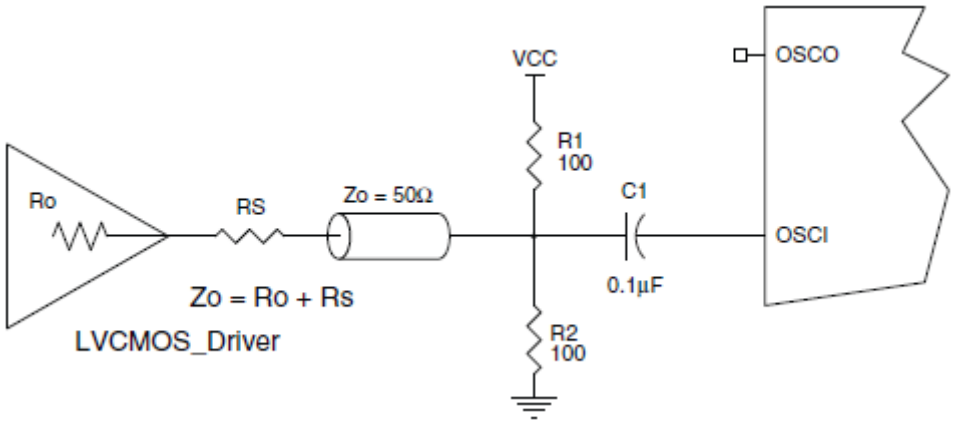

Figure 3. LVCMOS Driver to XTAL Input Interface

7. Operating Temperature

Select an operating temperature range for the crystal. Operating the crystal outside this range may prematurely age the crystal (increased ppm frequency change over time) or may damage the housing. A crystal operating outside of its temperature range can result in higher frequency offset caused by the temperature which can lead the frequency to exceed the crystal specifications. Crystal performance is typically not guaranteed beyond its specified temperature range. The recommended operating temperature range for ClockMatrix devices is -40°C to +85°C.

8. Frequency Tolerance

Select a manufacturing tolerance (maximum deviation from the specified resonant frequency at room temperature) and frequency shift over the operating temperature range (often called frequency stability) that will be acceptable for the application. When tight frequency tolerances (< 10ppm) over the operating temperature range are a requirement, it may be necessary to use a TCXO (temperature compensated crystal oscillator) or OCXO (oven-controlled crystal oscillator) instead.

Note that for Clock Matrix products, the crystal or crystal oscillator at OSCI is the jitter reference. It is preferred to use a crystal for low jitter instead of a generated clock signal.

The TCXO and OCXO at the XO_DPLL input is the frequency reference for the system DPLL. The TCXO or OCXO should be selected for accurate frequency and low frequency drift.

9. Aging

Confirm that the crystal aging tolerance (ppm per year) meets the application requirement. Exceeding the drive level on the crystal, shock and vibration and operating the crystal outside of its specified temperature range will accelerate aging. If the crystal will experience shock or vibration in its application, consider an oven-controlled SC-cut crystal, which is more tolerant of vibration.

10. Recommended Crystals (XTAL) and Crystal Oscillators (XO)

Table 4 provides a list of crystals that would be acceptable for applications using a ClockMatrix device. Similarly, Table 5 provides a list of crystal oscillators that would be acceptable for applications using a ClockMatrix device. The selection of the frequency will depend on the application. For additional crystal oscillator recommendations, see the Recommended Crystal Oscillators for Network Synchronization application note.

Table 4. Recommended Crystals for ClockMatrix Applications

Mfg.	Type	Recommend P/N	Product Size (mm)	Freq. (MHz)	ESR (ohm)	CL (pF)	Typical Drive Level (µW)	Frequency Tolerance (ppm)	Frequency Stability (ppm)	Aging (ppm/Year at 25°C)	Temperature Range
NDK	XTAL	EXS00A-CS17097	3.2 × 2.5	49.152	30	8	250	±10	±15	±1	-40 to +85°C
NDK	XTAL	EXS00A-CS17099	2.0 x 1.6	49.152	30	8	250	±10	±15	±1	-40 to +85°C
NDK	XTAL	EXS00A-CS17097	3.2 × 2.5	49.152	30	8	250	±10	±15	±1	-40 to +85°C
TXC	XTAL	8Y49172006	2.0 x 1.6	49.152	30	8	300	±10	±15	±1	-40 to +85°C
Epson	XTAL	TSX-3225 48.0000ME18X-W	3.2 × 2.5	48	40	12	200 (max)	±15	±18	±1	-40 to +85°C
Epson	XTAL	TSX-3225 38.8800MA20X-WX	3.2 × 2.5	38.88	40	12	200 (max)	±20	±20	±1	-40 to +85°C
Epson	XTAL	TSX-3225 38.8800MF18X-W0	3.2 × 2.5	38.88	40	12	200 (max)	±10	±18	±1	-40 to +85°C
Epson	XTAL	TSX-3225 38.4000MHz	3.2 × 2.5	38.4	40	8	200 (max)	±10	±15	±1	-40 to +85°C
Epson	XTAL	TSX-3225 38.40M-C0AANNG40RGX	3.2 × 2.5	38.4	40	12	200 (max)	±10	±20	±1	-40 to +85°C
Epson	XTAL	TSX-3225 25.0000MF20X-AJX	3.2 × 2.5	25	40	8	200 (max)	±10	±20	±1	-40 to +85°C
Epson	XTAL	TSX-3225 25.0000MF18X-WX	3.2 × 2.5	25	40	12	200 (max)	±10	±18	±1	-40 to +85°C
Epson	XTAL	TSX-3225 25.0000ME18X-AJX	3.2 × 2.5	25	40	12	200 (max)	±15	±18	±1	-40 to +85°C

Table 5. Recommended Crystal Oscillators for Clock Matrix Applications

Mfg.	Type	TXC Recommend P/N	Product Size (mm)	Frequency (MHz)	Voltage (V)	Total Frequency Stability (ppm)	Temperature Range
TXC	XO	8W48070007	2.5 × 2.0	48	3.3	±50	-40 to +105°C
TXC	XO	8W49170004	2.5 × 2.0	49.152	3.3	±25	-40 to +85°C
TXC	XO	8W50070006	2.5 × 2.0	50	3.3	±50	-40 to +105°C
TXC	XO	8W54070002	2.5 × 2.0	54	3.3	±50	-40 to +105°C
TXC	XO	8W62570006	2.5 × 2.0	62.5	3.3	±50	-40 to +105°C
Epson	XO	SG-8018Cg 62.5000M-TJHSAB	2.5 × 2.0	62.5	3.3	±50	-40 to +105°C
Epson	XO	FA-118T 48.0000MF20X-AJX	1.6 × 1.2	48	3.3	±30	-40 to +85°C
Epson	XO	SG2016CAN 48.0000M TJGA	2.0 × 1.6	48	3.3	±50	-40 to +85°C
Epson	XO	SG-8101CE 49.1520M TCHSA	3.2 × 2.5	49.152	3.3	±50	-40 to +105°C
Epson	XO	SG3225CAN 50.0000M TJHA	3.2 × 2.5	50	3.3	±50	-40 to +105°C
Epson	XO	SG8101CE 54.0000M TCHSA	3.2 × 2.5	54	3.3	±50	-40 to +105°C

11. Revision History

Revision	Date	Description
1.05	Sep 22, 2025	Updated Table 4 to add NDK EXS00A-CS17097 crystal
1.04	Jul 24, 2025	Updated Table 4 to add TXC 8Y49172006 crystal
1.03	May 12, 2025	Updated Table 4 to add 49.152MHz crystals from NDK
1.02	Apr 24, 2025	Updated Table 4 to remove all crystals with a drive level of 100µW
1.01	Jun 5, 2024	▪ Updated Figure 1 ▪ Updated last paragraph in Load Capacitance section
1.00	Oct 19, 2023	Initial release.

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