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SH7080 Group

Clearing the MTU2S Counter by Using a Flag Setting Source of the MTU2

Introduction

This application note describes the function to clear the counter of the multi-function timer pulse unit 2S (MTU2S) by using a flag setting source of the multi-function timer pulse unit 2 (MTU2). Please use this application note as a guide in designing user programs.

Although the programs given in this application note have been verified for correct operation, we strongly recommend that the user confirm correct operation before applying the programs in the actual application.

Target Device

SH7085

Contents

1. Specifications

In this sample application, the MTU2 is configured for compare-match operation, and the counter of the MTU2S is cleared when the MTU2's compare-match flag is set (MTU2-MTU2S synchronous counter clearing). Figure 1 shows the basic specifications of this sample task.

- Channel 0 of the MTU2 performs compare-match operation using timer counter 0 (TCNT_0) and timer general register A_0 (TGRA_0). It also generates a compare-match interrupt to the CPU on a match.
- The period for compare-match operation on channel 0 of the MTU2 is set to 100 ms.
- Timer counter_4S (TCNT_4S) on channel 4 of the MTU2S is cleared synchronously when the compare-match flag in channel 0 of the MTU2 is set.
- The synchronous clearing of the timer counter on channel 4 of the MTU2S is enabled by setting the timer synchronous clear register S (TSYCRS).

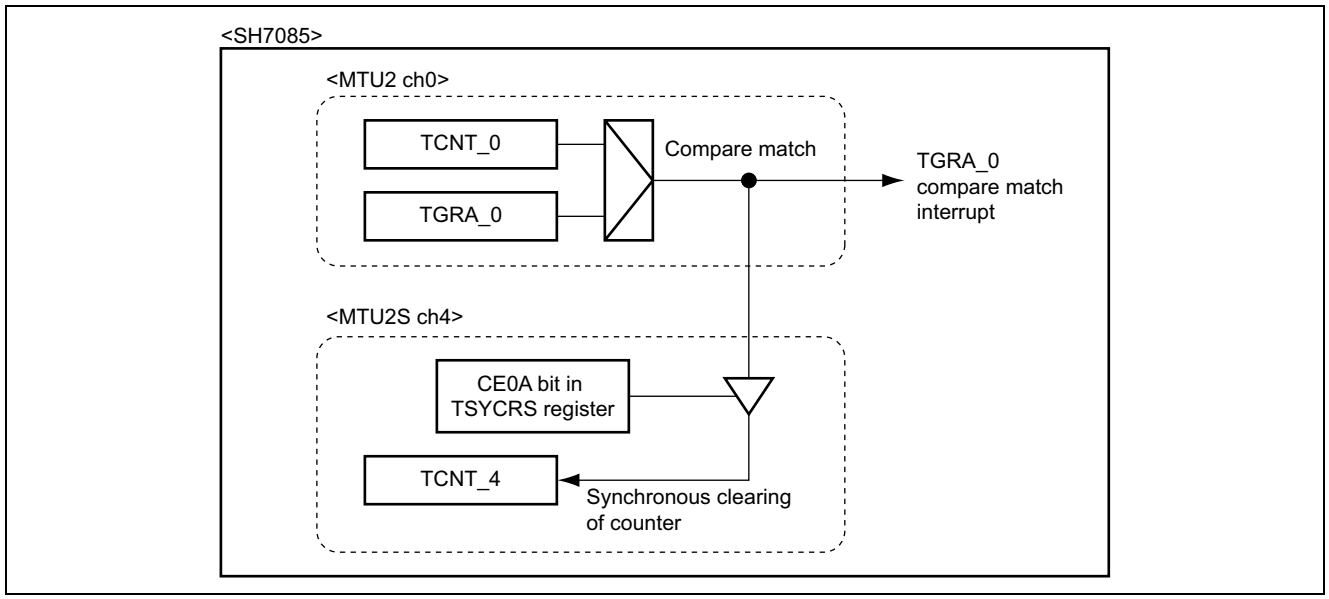


Figure 1 Operational Overview

2. Conditions for Application

Operating frequency:	Internal clock:	80 MHz
	Bus clock:	40 MHz
	Peripheral clock:	40 MHz
	MTU2 clock:	40 MHz
	MTU2S clock:	80 MHz
C compiler:	Version 7.1.04 from Renesas Technology Corp.	

3. MCU Functions Used

In this sample task, the MTU2 is configured for compare-match operation, and the counter of the MTU2S is cleared synchronously on compare-match flag setting in the MTU2. Figure 2 outlines the operation.

Timer counter_0 (TCNT_0) of the MTU2 is cleared on compare match with timer general register A_0 (TGRA_0), and a compare-match interrupt (TGIA_0 interrupt) is generated to the CPU. Timer counter_4S (TCNT_4S) of the MTU2S is also cleared synchronously on the compare match that occurs in channel 0 of the MTU2. The synchronous clearing can be set by the timer synchronous clear register S (TSYCRS).

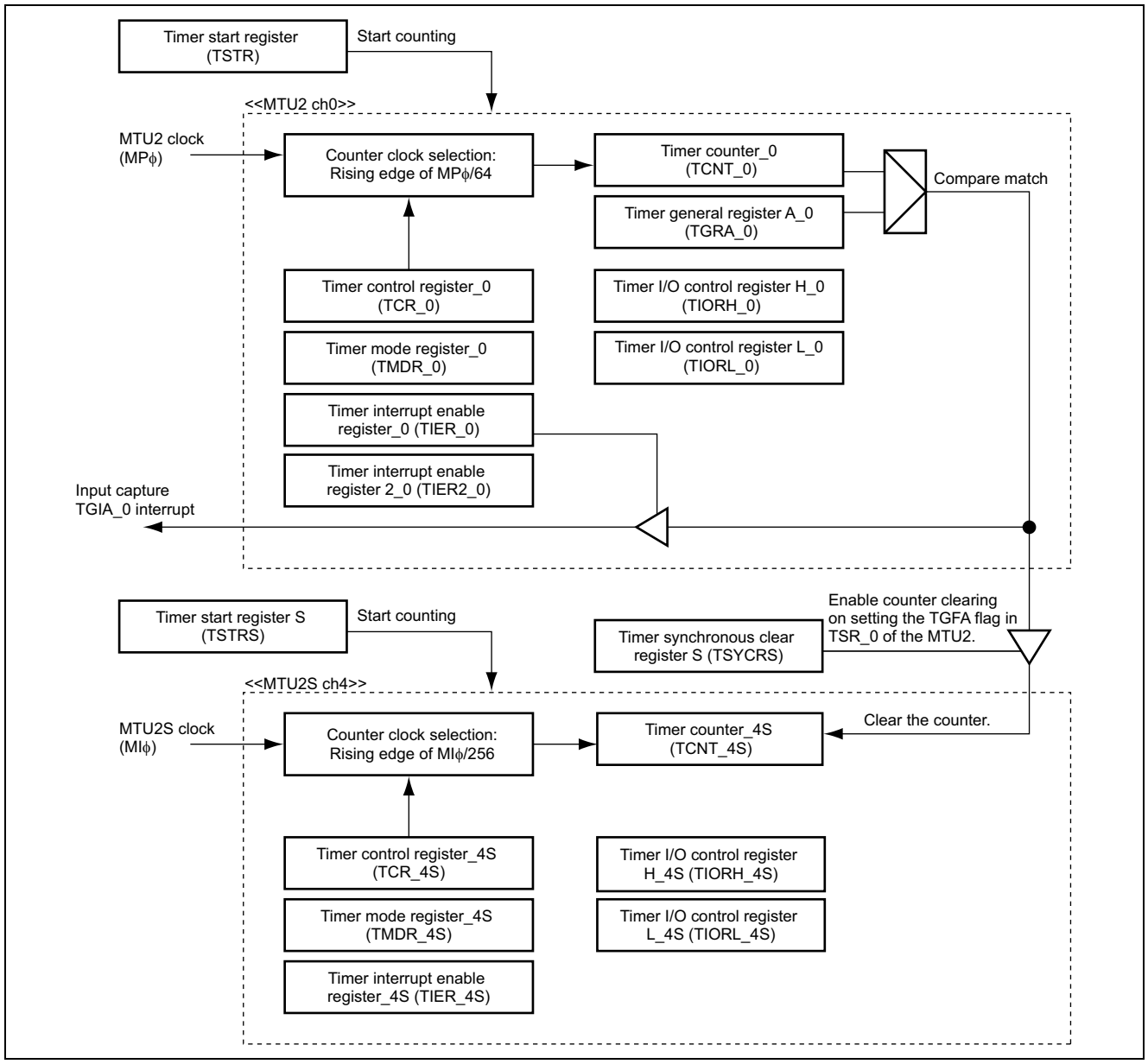


Figure 2 Operational Block Diagram of Channel 0 of MTU2 and Channel 4 of MTU2S

- Timer counter_0 (TCNT_0) is a 16-bit readable/writable counter. Counting by TCNT_0 is driven by the MTU2 clock (MPϕ).
- Timer general register A_0 (TGRA_0) is a 16-bit readable/writable register. TGRA_0 operates as an output compare register. The period for compare-match operation is set in TGRA_0.
- Timer I/O control register H_0 (TIORH_0) is an 8-bit readable/writable register that specifies the functions of TGRA_0 and TGRB_0. TGRA_0 is set to operate as an output compare register.
- Timer I/O control register L_0 (TIORL_0) is an 8-bit readable/writable register that specifies the functions of TGRC_0 and TGRD_0.
- Timer interrupt enable register_0 (TIER_0) is an 8-bit readable/writable register. TIER_0 enables/disables interrupt requests caused by registers TGRA_0 to TGRD_0 and the TCFV overflow flag, and also enables/disables the A/D converter start requests by TGRA_0 and TGRE_0.
- Timer interrupt enable register 2_0 (TIER2_0) is an 8-bit readable/writable register. TIER2_0 enables/disables interrupt requests caused by registers TGRE_0 and TGRF_0, and A/D converter start requests by TGRE_0.
- Timer mode register_0 (TMDR_0) is an 8-bit readable/writable register that specifies the operating mode. Channel 0 is placed in normal operation mode.
- Timer control register_0 (TCR_0) is an 8-bit readable/writable register that controls the operation of TCNT_0. TCNT_0 is cleared on compare match with TGRA_0.
- Timer start register (TSTR) is an 8-bit readable/writable register that starts/stops TCNTs of channels 0 to 4.
- Timer counter_4S (TCNT_4S) is a 16-bit readable/writable counter. Counting by TCNT_4S is driven by the MTU2S clock (MIϕ). TCNT_4S is cleared on compare match with TGRA_0 on channel 0 of the MTU2.
- Timer I/O control register H_4S (TIORH_4S) is an 8-bit readable/writable register that specifies the functions of TGRA_4S and TGRB_4S.
- Timer I/O control register L_4S (TIORL_4S) is an 8-bit readable/writable register that specifies the functions of TGRC_4S and TGRD_4S.
- Timer interrupt enable register_4S (TIER_4S) is an 8-bit readable/writable register. TIER_4S enables/disables interrupt requests caused by registers TGRA_4S to TGRD_4S and the TCFV overflow flag, and also enables/disables the A/D converter start requests by TGRA_0 and an underflow of TCNT_4.
- Timer mode register_4S (TMDR_4S) is an 8-bit readable/writable register that specifies the operating mode.
- Timer control register_4S (TCR_4S) is an 8-bit readable/writable register that controls the operation of TCNT_4S. TCR_4S specifies the clearing source for TCNT_4S, clock edge, and counter clock.
- Timer synchronous clear register S (TSYCRS) is an 8-bit readable/writable register. TSYCRS specifies the conditions for clearing TCNT_3S and TCNT_4S in the MTU2S from the MTU2.
- Timer start register S (TSTRS) is an 8-bit readable/writable register. TSTRS starts/stops TCNTs of channels 3 and 4.

4. Operation

Figure 3 shows the operation of the sample application, and table 1 describes the software and hardware processing.

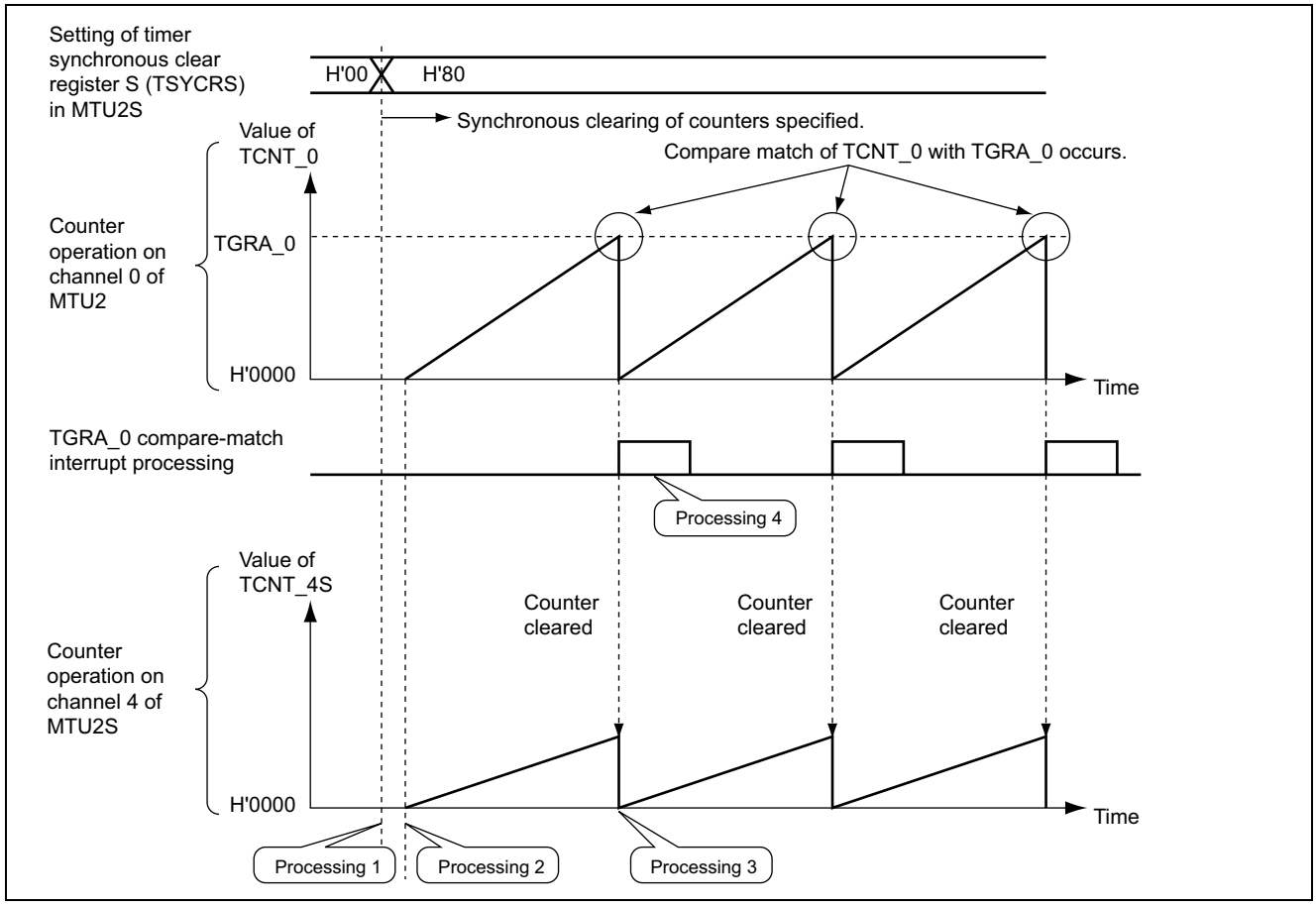


Figure 3 Operation

Table 1 Software and Hardware Processing

	Software Processing	Hardware Processing
Processing 1	Sets the flag setting source that causes counter clearing of TCNT_4S.	—
Processing 2	Starts the timer counters of the MTU2 and MTU2S.	—
Processing 3	—	Compare match with TGRA_0 occurs on channel 0 of the MTU2. Clears timer counter TCNT_4S on channel 4 of the MTU2S synchronously.
Processing 4	Clears the interrupt flag to 0. Stores the MTU2S timer counter value to a variable (to make sure that the counter has been cleared to 0).	Generates a TGRA_0 compare-match interrupt.

5. Software

5.1 Modules

Table 2 describes the modules used in the sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main()	Performs initial setting of the MTU2 and MTU2S. Starts the timers.
TGRA_0 compare-match interrupt routine	Int_mtu2_tgia0()	Processes the compare-match interrupt from channel 0 of the MTU2.

5.2 Variable

Table 3 shows the variable used in the sample task.

Table 3 Description of Variable

Label Name of Variable	Function	Used in
unsigned short Count_value	The counter value on channel 4 of the MTU2S is stored.	int_mtu2_tgia0()

5.3 Register Settings

The register settings used in the sample application are described below. Note that the set values are specifically used in the sample task and that they are different from the initial values.

5.3.1 Setting for Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
  - Setting value: H'0241
  - Function: Specifies the frequency division ratio.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	IFC[2] to IFC[0]	000	Frequency division ratio for internal clock (Iϕ) 000: ×1 (80 MHz when input clock is 10 MHz)
11 to 9	BFC[2] to BFC[0]	001	Frequency division ratio for bus clock (Bϕ) 001: ×1/2 (40 MHz when input clock is 10 MHz)
8 to 6	PFC[2] to PFC[0]	001	Frequency division ratio for peripheral clock (Pϕ) 001: ×1/2 (40 MHz when input clock is 10 MHz)
5 to 3	MIFC[2] to MIFC[0]	000	Frequency division ratio for MTU2S clock (MIϕ) 000: ×1 (80 MHz when input clock is 10 MHz)
2 to 0	MPFC[2] to MPFC[0]	001	Frequency division ratio for MTU2 clock (MPϕ) 001: ×1/2 (40 MHz when input clock is 10 MHz)

5.3.2 Settings for Power-Down Modes

- Standby Control Register 4 (STBCR4)
  - Setting value: H'3f
  - Function: Controls the operation of the modules in power-down modes.

Bit	Bit Name	Value	Description
7	MSTP23	0	0: The MTU2S runs.
6	MSTP22	0	0: The MTU2 runs.
5	MSTP21	1	1: Stops supply of the clock signal to the CMT.
4, 3	—	11	Reserved
2	MSTP18	1	1: Stops supply of the clock signal to the A/D_2.
1	MSTP17	1	1: Stops supply of the clock signal to the A/D_1.
0	MSTP16	1	1: Stops supply of the clock signal to the A/D_0.

5.3.3 Settings for Channel 0 of Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Control Register_0 (TCR_0)
  - Setting value: H'23
  - Function: Controls TCNT of channel 0.

Bit	Bit Name	Value	Description
7 to 5	CCLR[2] to CCLR[0]	001	001: TCNT is cleared on compare match with TGRA.
4, 3	CKEG[1], CKEG[0]	00	00: TCNT is incremented on the rising edge of the clock.
2 to 0	TPSC[2] to TPSC[0]	011	011: Counting is driven by internal clock MPϕ/64.

- Timer Mode Register_0 (TMDR_0)
  - Setting value: H'00
  - Function: Sets the operating mode of channel 0.

Bit	Bit Name	Value	Description
7	—	0	Reserved
6	BFE	0	0: TGRE and TGRF operate normally.
5	BFB	0	0: TGRB and TGRD operate normally.
4	BFA	0	0: TGRA and TGRC operate normally.
3 to 0	MD[3] to MD[0]	0000	These bits select the operating mode of the timer. 0000: Normal mode

- Timer Counter_0 (TCNT_0)
  - Setting value: H'0000
  - Function: 16-bit counter
- Timer General Register A_0 (TGRA_0)
  - Setting value: H'f423
  - Function: Sets the period of compare match to 100 ms.
- Timer General Register B_0 (TGRB_0)
  - Setting value: Not set
  - Function: General register B
- Timer General Register C_0 (TGRC_0)
  - Setting value: Not set
  - Function: General register C
- Timer General Register D_0 (TGRD_0)
  - Setting value: Not set
  - Function: General register D
- Timer General Register E_0 (TGRE_0)
  - Setting value: Not set
  - Function: General register E

- Timer General Register F_0 (TGRF_0)
  - Setting value: Not set
  - Function: General register F

- Timer I/O Control Register H_0 (TIORH_0)
  - Setting value: H'00
  - Function: Controls TGRA and TGRB.

Bit	Bit Name	Value	Description
7 to 4	IOB[3] to IOB[0]	0000	0000: TGRB_0 operates as an output compare register. TheTIOC0B pin retains its output level.
3 to 0	IOA[3] to IOA[0]	0000	0000: TGRA_0 operates as an output compare register. TheTIOC0A pin retains its output level.

- Timer I/O Control Register L_0 (TIORL_0)
  - Setting value: H'00
  - Function: Controls TGRC and TGRD.

Bit	Bit Name	Value	Description
7 to 4	IOD[3] to IOD[0]	0000	0000: TGRD_0 operates as an output compare register. TheTIOC0D pin retains its output level.
3 to 0	IOC[3] to IOC[0]	0000	0000: TGRC_0 operates as an output compare register. TheTIOC0C pin retains its output level.

- Timer Interrupt Enable Register_0 (TIER_0)
  - Setting value: H'01
  - Function: Enables/disables interrupt requests from channel 0.

Bit	Bit Name	Value	Description
7	TTGE	0	0: Disables generation of A/D converter start requests.
6	—	0	Reserved in channels 0 to 3
5	—	0	Reserved in channels 0, 3, and 4
4	TCIEV	0	0: Disables interrupt requests (TCIV) by the TCFV flag.
3	TGIED	0	0: Disables interrupt requests (TGID) by the TGFD flag.
2	TGIEC	0	0: Disables interrupt requests (TGIC) by the TGFC flag.
1	TGIEB	0	0: Disables interrupt requests (TGIB) by the TGFB flag.
0	TGIEA	1	1: Enables interrupt requests (TGIA) by the TGFA flag.

- Timer Interrupt Enable Register 2_0 (TIER2_0)
  - Setting value: H'00
  - Function: Enables/disables interrupt requests from channel 0.

Bit	Bit Name	Value	Description
7	TTGE2	0	0: Disables generation of A/D converter start requests on compare match with TGRE_0.
6 to 2	—	00000	Reserved
1	TGIEF	0	0: Disables interrupt requests (TGIF) by the TGFE flag.
0	TGIEE	0	0: Disables interrupt requests (TGIE) by the TGEE flag.

5.3.4 Settings Common to All Channels of Multi-Function Timer Pulse Unit 2 (MTU2)

- Timer Start Register (TSTR)
  - Setting value: H'01
  - Function: Starts/stops TCNTs of channels 0 to 4.

Bit	Bit Name	Value	Description
7	CTS4	0	0: Stops counting by TCNT_4.
6	CTS3	0	0: Stops counting by TCNT_3.
5 to 3	—	000	Reserved
2	CTS2	0	1: Stops counting by TCNT_2.
1	CTS1	0	1: Stops counting by TCNT_1.
0	CTS0	1	0: Starts counting by TCNT_0.

5.3.5 Settings for Channel 4 of Multi-Function Timer Pulse Unit 2S (MTU2S)

- Timer Control Register_4S (TCR_4S)
  - Setting value: H'64
  - Function: Controls TCNT of channel 4.

Bit	Bit Name	Value	Description
7 to 5	CCLR[2] to CCLR[0]	011	011: TCNT is cleared by counter clearing on another channel performing synchronous clearing or synchronous operation.*
4, 3	CKEG[1], CKEG[0]	00	00: TCNT is incremented on the rising edge of the clock.
2 to 0	TPSC[2] to TPSC[0]	100	011: Counting is driven by internal clock MPϕ/256.

Note: * Synchronous operation can be specified by setting the SYNC bit in TSYR to 1.

- Timer Mode Register_4S (TMDR_4S)
  - Setting value: H'00
  - Function: Sets the operating mode of channel 4.

Bit	Bit Name	Value	Description
7	—	0	Reserved
6	—	0	Reserved in channels 1 to 4
5	BFB	0	0: TGRB and TGRD operate normally.
4	BFA	0	0: TGRA and TGRC operate normally.
3 to 0	MD[3] to MD[0]	0000	These bits select the operating mode of the timer. 0000: Normal mode

- Timer Counter_4S (TCNT_4S)
  - Setting value: H'0000
  - Function: 16-bit counter

- Timer General Register A_4S (TGRA_4S)
  - Setting value: Not set
  - Function: General register A

- Timer General Register B_4S (TGRB_4S)
  - Setting value: Not set
  - Function: General register B
- Timer General Register C_4S (TGRC_4S)
  - Setting value: Not set
  - Function: General register C
- Timer General Register D_4S (TGRD_4S)
  - Setting value: Not set
  - Function: General register D
- Timer I/O Control Register H_4S (TIORH_4S)
  - Setting value: H'00
  - Function: Controls TGRA and TGRB.

Bit	Bit Name	Value	Description
7 to 4	IOB[3] to IOB[0]	0000	0000: TGRB_4S operates as an output compare register. TheTIOC4BS pin retains its output level.
3 to 0	IOA[3] to IOA[0]	0000	0000: TGRA_4S operates as an output compare register. TheTIOC4AS pin retains its output level.

- Timer I/O Control Register L_4S (TIORL_4S)
  - Setting value: H'00
  - Function: Controls TGRC and TGRD.

Bit	Bit Name	Value	Description
7 to 4	IOD[3] to IOD[0]	0000	0000: TGRD_4S operates as an output compare register. TheTIOC4DS pin retains its output level.
3 to 0	IOC[3] to IOC[0]	0000	0000: TGRC_4S operates as an output compare register. TheTIOC4CS pin retains its output level.

- Timer Interrupt Enable Register_4S (TIER_4S)
  - Setting value: H'00
  - Function: Enables/disables interrupt requests from channel 4.

Bit	Bit Name	Value	Description
7	TTGE	0	0: Disables generation of A/D converter start requests.
6	TTGE2	0	0: Disables generation of A/D converter start requests by TCNT_4 underflow (trough).
5	—	0	Reserved in channels 0, 3, and 4
4	TCIEV	0	0: Disables interrupt requests (TCIV) by the TCFV flag.
3	TGIED	0	0: Disables interrupt requests (TGID) by the TGFD flag.
2	TGIEC	0	0: Disables interrupt requests (TGIC) by the TGFC flag.
1	TGIEB	0	0: Disables interrupt requests (TGIB) by the TGFB flag.
0	TGIEA	0	0: Disables interrupt requests (TGIA) by the TGFA flag.

5.3.6 Settings Common to All Channels of Multi-Function Timer Pulse Unit 2S (MTU2S)

- Timer Start Register S (TSTRS)
  - Setting value: H'80
  - Function: Starts/stops TCNTs of channels 3 and 4.

Bit	Bit Name	Value	Description
7	CTS4	1	1: Starts TCNT_4 count operation.
6	CTS3	0	0: Stops TCNT_3 count operation.
5 to 3	—	000	Reserved
2 to 0	—	000	Reserved in the MTU2S

- Timer Synchronous Clear Register (TSYCR)
  - Setting value: H'80
  - Function: Specifies conditions for clearing of MTU2S's TCNT_3 and TCNT_4 in synchronization with the MTU2.

Bit	Bit Name	Value	Description
7	CE0A	1	1: Enables counter clearing by TGFA flag setting in TSR_0.
6	CE0B	0	0: Disables counter clearing by TGFB flag setting in TSR_0.
5	CE0C	0	0: Disables counter clearing by TGFC flag setting in TSR_0.
4	CE0D	0	0: Disables counter clearing by TGFD flag setting in TSR_0.
3	CE1A	0	0: Disables counter clearing by TGFA flag setting in TSR_1.
2	CE1B	0	0: Disables counter clearing by TGFB flag setting in TSR_1.
1	CE2A	0	0: Disables counter clearing by TGFA flag setting in TSR_2.
0	CE2B	0	0: Disables counter clearing by TGFB flag setting in TSR_2.

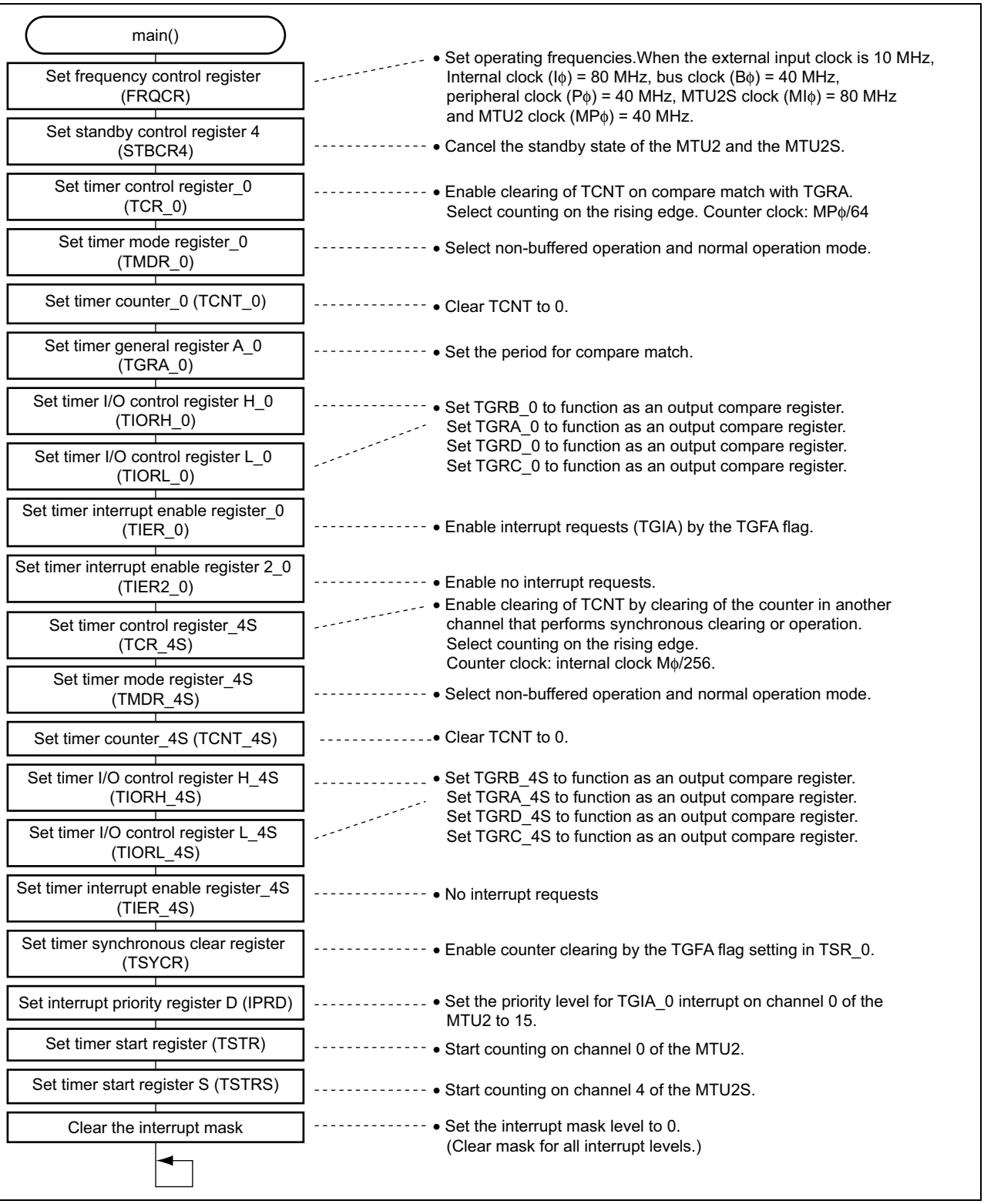
5.3.7 Settings for Interrupt Controller (INTC)

- Interrupt Priority Register D (IPRD)
  - Setting value: H'f000
  - Function: Sets priority levels of the corresponding interrupt requests.

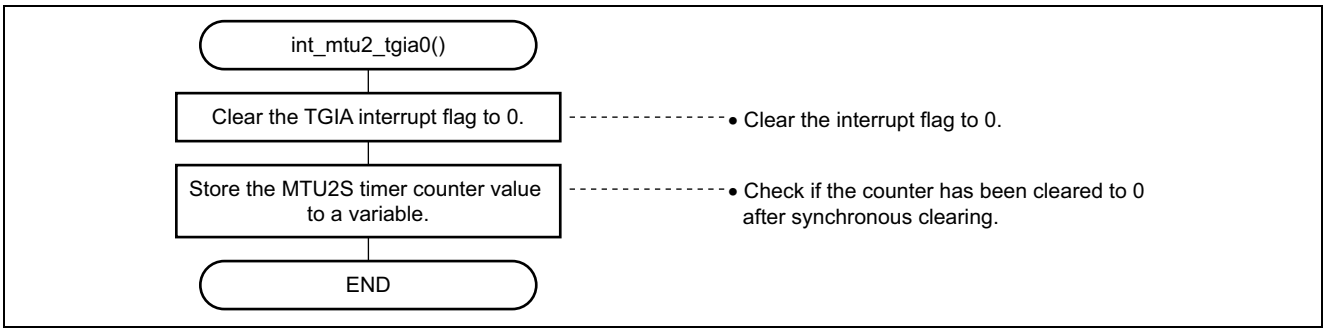
Bit	Bit Name	Value	Description
15 to 12	IPR[15] to IPR[12]	1111	Priority level 15 is set for the TGIA_0 interrupt on channel 0 of the MTU2
11 to 8	IPR[11] to IPR[8]	0000	Priority level 0 is set for the corresponding interrupts.
7 to 4	IPR[7] to IPR[4]	0000	Priority level 0 is set for the corresponding interrupts.
3 to 0	IPR[3] to IPR[0]	0000	Priority level 0 is set for the corresponding interrupts.

6. Flowcharts

6.1 Main Routine



6.2 TGRA_0 Compare-Match Interrupt Routine



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Rev.	Date	Page	Summary
1.00	Sep.05.05	—	First edition issued

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