Choosing the Correct Crystal or XO for FemtoClock 4 and FemtoClock 4 Wireless

This document highlights the characteristics to consider when choosing a crystal or XO for FemtoClock™4 (FC4) and FemtoClock™4 (FC4W) devices. It also contains lists of recommended crystals and XOs to be used with FC4.

Contents

1. Introduction 2

2. Frequency 4

2.1 FC4 Frequency Parameters 4

2.1.1 FC4 A1 Frequency Parameters 4

2.1.2 FC4 A200 Frequency Parameters 4

2.2 FC4W Frequency Parameters 5

2.2.1 FC4W A100 Frequency Parameters 5

2.2.2 FC4W A200 Frequency Parameters 5

3. Load Capacitance 6

4. Equivalent Series Resistance 7

5. Drive Level 7

6. Using a Crystal Oscillator (XO) with FC4 and FC4W 7

7. Operating Temperature 9

8. Frequency Tolerance 9

9. Aging 9

10. Recommended Crystals (XTAL) and Crystal Oscillators (XO) 10

11. Revision History 13

Tables

Table 1. FC4 XIN Input Parameters 2

Table 2. REF_CLK Characteristics 3

Table 3. Recommended Output Frequency / Crystal Frequency Pairs for FC4 A100 Devices 4

Table 4. Recommended Output Frequency / Crystal Frequency Pairs for FC4 A200 Devices 5

Table 5. Recommended Output Frequency / Crystal Frequency Pairs for FC4W A100 Devices 5

Table 6. Recommended Output Frequency / Crystal Frequency Pairs for FC4W A200 Devices 5

Table 7. Recommended Crystals for FC4 and FC4W Applications 10

Table 8. Recommended Crystal Oscillators for FC4 and FC4W Applications 12

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1. Introduction

The FemtoClock 4 (FC4 and FC4W) family of devices uses a crystal (XTAL), or crystal oscillator (XO) as a reference for the analog PLL (APLL). All FC4 and FC4W outputs are synthesized from the APLL. When using a XTAL, the signal pins of the crystal will be connected to the XIN and XOUT pins of the FC4 or FC4W device. When using a XO, the signal pin of the XO can be connected to the REF_CLK pin of the FC4 or FC4W device. When using the REF_CLK pin, the XIN and XOUT pins should be left floating. Alternatively, the XO can be connected to the XIN pin of the FC4 or FC4W device while leaving the XOUT pin floating (overdriving the XIN pin). The recommendation is to use the REF_CLK pin instead of overdriving the XIN pin. For more details about using an XO, refer to section 6 of this document.

When choosing the crystal or XO for a FC4 or FC4W device, several characteristics must be considered to ensure optimal performance and minimized output jitter. The following sections highlight these crystal or XO characteristics so that the correct crystal is chosen for a given project. Table 1 provides a summary of the FC4 and FC4W crystal input (XIN) requirements.

Table 1. FC4 XIN Input Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
-	Mode of Oscillation	-	Fundamental			-
F_{IN}	Input Frequency	With a quartz crystal resonator between XIN and XOUT	25	-	80	MHz
		(Over-)Driving XIN with oscillator	25	-	100	MHz
f_{VCO}	Analog PLL VCO Operating Frequency	A1xx devices	9.8	-	10.35	GHz
		A2xx devices	9.25	-	9.85	GHz
Requirements for Crystals						
ESR	Equivalent Series Resistance	$8pF \leq C_L \leq 10pF$	-	-	50	Ω
C_O	Shunt Capacitance	-	-	-	4	pF
C_L	Load Capacitance	-	-	8	10	pF
Drive	Drive Level	C_L = 8pF	-	246	-	µW
		C_L = 10pF	-	342	-	µW
F_{TOL} [1] [5] [3] [4]	Frequency Tolerance	-	-450	-	450	PPM
Requirements for XOs (When Overdriving the XIN pin)						
V_{BIAS}	Bias Point for XIN	Over-driving crystal input	-	0.6	-	V
V_{IVS}	Input Voltage Swing for XIN	Over-driving crystal input	0.5	-	1.2	V
Vslew [5]	Input Slew Rate for XIN	Over-driving crystal input	0.6	-	-	V/ns

1. F_TOL refers to the frequency accuracy of the APLL frequency reference, either a crystal connected between XIN and XOUT, or an oscillator connected to the REF_CLK pin. The APLL can reliably lock to a reference that meets the F_TOL limits.
2. Inclusive of initial tolerance at 25°C, temperature stability, and aging.
3. The APLL frequency steering range (±F_STEER) available for a DPLL or DCO to digitally steer the APLL is determined by the following expression: F_STEER = |F_TOL| - |F_ACC|; where F_ACC is the frequency accuracy of the APLL frequency reference. For example, if the frequency accuracy of the APLL frequency reference is ±100PPM. then the APLL frequency steering range will be ±350PPM.
4. These parameters are customer/application dependent. Common maximum values are F_{TOL} = ±20ppm, F_{STAB} = ±20ppm, and Aging = ±5ppm/10years. The customer is free to adjust these parameters to their particular requirements.

5. The slew rate is calculated by measuring at the midpoint of the rising waveform using a window of ±200mV.

Table 2. REF_CLK Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum
F_{IN}	REF_CLK Input Frequency	Single-ended input	25 MHz	-	100 MHz
V_{SR}	Input Voltage Slew Rate for REF_CLK pin	-	0.7 V/ns	-	-
V_{IH}	Input High Voltage	-	1.0 V	-	3.6 V
V_{IL}	Input Low Voltage	-	-0.3 V	-	0.3 V
V_{BIAS}	Bias Point for the REF_CLK pin	-	-	0.65 V	-

2. Frequency

FC4 and FC4W are each supported in two different hardware revisions, A100 and A200. The A100 revision supports a VCO range of 9.8GHz to 10.35GHz, and the A200 revision supports a VCO range of 9.25GHz to 9.85GHz. Both hardware revisions support crystals with frequencies in the range of 25MHz to 80 MHz, and frequencies in the range of 25MHz to 100MHz when overdriving the crystal inputs.

For applications that have DPLLs in synthesizer mode, the best performance is obtained by selecting a frequency that is an integer multiple of the VCO frequency to allow all dividers to run in integer mode.

For applications that have DPLLs in jitter attenuator mode, the best performance is obtained by selecting a crystal frequency that is not an integer of the VCO or the output frequency. Following this recommendation will reduce the likelihood of boundary spurs. Attention should also be paid to the harmonic frequencies of the crystal and outputs to avoid boundary spurs. Boundary spurs are produced when the phase-locked loop (PLL) feedback loop fractional divider ratio is programmed to a value that is close to an integer. Boundary spurs occur because the harmonics of the phase and frequency detector (PFD) frequency mix with the VCO (or its harmonics) and the resultant intermodulation frequency components fall within the loop bandwidth. Ideally, the ratio of an output frequency or its harmonics to the crystal frequency (or the crystal frequencies harmonics) should not have a fractional component close to 0.0 or 0.5, with the best cases being a fractional component of 0.25 or 0.75. For a detailed explanation of boundary spurs, see the application note, *Integer Boundary Spurs in Fractional Feedback Phase-Locked Loops (PLLs)*.

2.1 FC4 Frequency Parameters

2.1.1 FC4 A1 Frequency Parameters

Table 3 shows several recommended crystal frequencies for common output frequencies. The recommended crystal frequencies differ depending on whether synthesizer mode or jitter attenuator mode is being used. For 50MHz, 100MHz, 156.25MHz, 312.5MHz, and 625MHz synthesizer applications, it is recommended that a crystal frequency of 62.5MHz and VCO frequency of 10GHz be used as a primary option. As a secondary option, a crystal frequency of 78.125MHz and a VCO frequency of 10GHz can be used. These crystal frequency/VCO frequency combinations ensure that there is an integer relationship between the crystal frequency and the VCO, as well as between the VCO and the output frequency. These integer relationships decrease the likelihood of fractional spurs.

Table 3. Recommended Output Frequency / Crystal Frequency Pairs for FC4 A100 Devices

Mode	Output Frequencies (MHz)	Recommended Crystal Frequencies (MHz)	Recommended VCO Frequency (GHz)
Synthesizer	625, 312.5, 156.25, 100, 50	62.5, 78.125	10
	625, 312.5, 156.25	62.5, 78.125	10.3125
Jitter Attenuator	625, 312.5, 156.25, 100, 50	49.152, 54	10
	625, 312.5, 156.25	49.152, 68	10.3125

For jitter attenuator applications using output frequencies of 156.25MHz, 312.5MHz, and 625MHz, it is recommended that a crystal frequency of 68MHz and a VCO frequency of 10.3125GHz be used as the primary option. 49.152MHz can be selected as a secondary option with a VCO frequency of 10.3125GHz. This ensures that the APLL is not operating in integer mode and reduces the likelihood of integer boundary spurs.

2.1.2 FC4 A200 Frequency Parameters

Table 4 shows several recommend crystal frequencies for common output frequencies. The recommended crystal frequencies differ depending on whether synthesizer mode or jitter attenuator mode is being used. For 156.25MHz, 312.5MHz, and 625MHz synthesizer applications, it is recommended that a crystal frequency of 62.5MHz and VCO frequency of 9.375GHz be used as a primary option. These crystal frequency/VCO frequency

combinations ensure that there is an integer relationship between the crystal frequency and the VCO, as well as between the VCO and the output frequency. These integer relationships decrease the likelihood of fractional spurs.

For jitter attenuator applications using output frequencies of 122.88MHz, 491.52MHz, and 122.88MHz, it is recommended that a crystal frequency of 68MHz and a VCO frequency of 9.3804GHz be used as the primary option. 73MHz can be selected as a secondary option with a VCO frequency of 9.3804GHz. This ensures that the APLL is not operating in integer mode and reduces the likelihood of integer boundary spurs.

Table 4. Recommended Output Frequency / Crystal Frequency Pairs for FC4 A200 Devices

Mode	Output Frequencies (MHz)	Recommended Crystal Frequencies (MHz)	Recommended VCO Frequency (GHz)
Synthesizer	625, 312.5, 156.25	62.5	9.375
Jitter Attenuator	245.76, 122.88	60, 68	9.33888
	491.52, 245.76, 122.88	68, 73	9.8304

2.2 FC4W Frequency Parameters

2.2.1 FC4W A100 Frequency Parameters

Table 5 shows several recommended crystal frequencies for common output frequencies used on FC4W A100 devices. For best overall performance with FC4W A100 devices, Renesas recommends using a 68MHz crystal.

Table 5. Recommended Output Frequency / Crystal Frequency Pairs for FC4W A100 Devices

DPLL Mode	Output Frequency (MHz)	Recommended XTAL Frequencies (MHz)	Recommended VCO Frequency (GHz)
Jitter Attenuator	491.52, 245.76, 122.88	68, 73	9.8304
	491.52, 245.76, 122.88	60	10.32192

2.2.2 FC4W A200 Frequency Parameters

Table 6 shows several recommended crystal frequencies for common output frequencies used on FC4W A200 devices. For the best overall performance with FC4W A200 devices, Renesas recommends using a 68MHz crystal for jitter attenuator mode applications and a 62.5MHz crystal for synthesizer mode applications.

Table 6. Recommended Output Frequency / Crystal Frequency Pairs for FC4W A200 Devices

DPLL Mode	Output Frequency (MHz)	Recommended XTAL Frequencies (MHz)	Recommended VCO Frequency (GHz)
Jitter Attenuator	245.76, 122.88	60, 68	9.33888
	491.52, 245.76, 122.88	68, 73	9.8304

3. Load Capacitance

For FC4, Renesas recommends using a crystal that has a nominal load capacitance between 8pF and 10pF. FC4 does not use external tuning capacitors, but instead use an internal, adjustable load capacitance. The internal load capacitance can be adjusted in the programmed configuration file or via register writes to the device.

The total load capacitance can be modeled as seen in Figure 1, where C_{pcb1} and C_{pcb2} are the stray capacitance of the circuit board, C_{f1} and C_{f2} are the fixed capacitance internal to FC4/FC4W on each leg of the oscillator, C_{s1} and C_{s2} are the internal stray capacitance of the FC4/FC4W device, and C_{d1} and C_{d2} are the internal tuning caps (digicaps) of the FC4/FC4W device. For all capacitances, C_{xx1} refers to capacitances on the XIN pin and C_{xx2} refers to capacitances on the XOUT pin.

The load capacitance (C_L) for the XIN pin is:

$$C_L = \frac{1}{\frac{1}{C_{totalXIN}} + \frac{1}{C_{totalXOUT}}}$$

where

$$C_{totalXIN} = C_{f1} + C_{s1} + C_{d1} + C_{pcb1}$$

$$C_{totalXOUT} = C_{f2} + C_{s2} + C_{d2} + C_{pcb2}$$

For FC4 and FC4W devices, $C_{s1} = C_{s2} = 9.7$pF. By default, it is assumed that $C_{pcb1} = C_{pcb2} = 3.3$pF for both FC4 and FC4W evaluation boards. The circuit board stray capacitance values can be manually changed by setting the values of **xin_pcb_capacitance** and **xout_pcb_capacitance** in the RICBox GUI.

For FC4 and FC4W devices, $C_{f1} = C_{f2} = 5.965$pF and can be enabled/disabled via the **TOP.XO.XO_CNFGxo_fixedcap_0** (XIN fixed capacitance) and **TOP.XO.XO_CNFG.xo_fixedcap_1** (XOUT fixed capacitance). By default, the fixed capacitance is enabled.

For both FC4 and FC4W, the capacitance of the internal tuning capacitor for XIN can be controlled via the **TOP.XO.XO_CNFG.xobuf_digicap_x1** register and the capacitance of the internal tuning capacitor for XOUT can be controlled via the **TOP.XO.XO_CNFG.xobuf_digicap_x2** register. The default value for each internal tuning capacitor is 0.00pF.

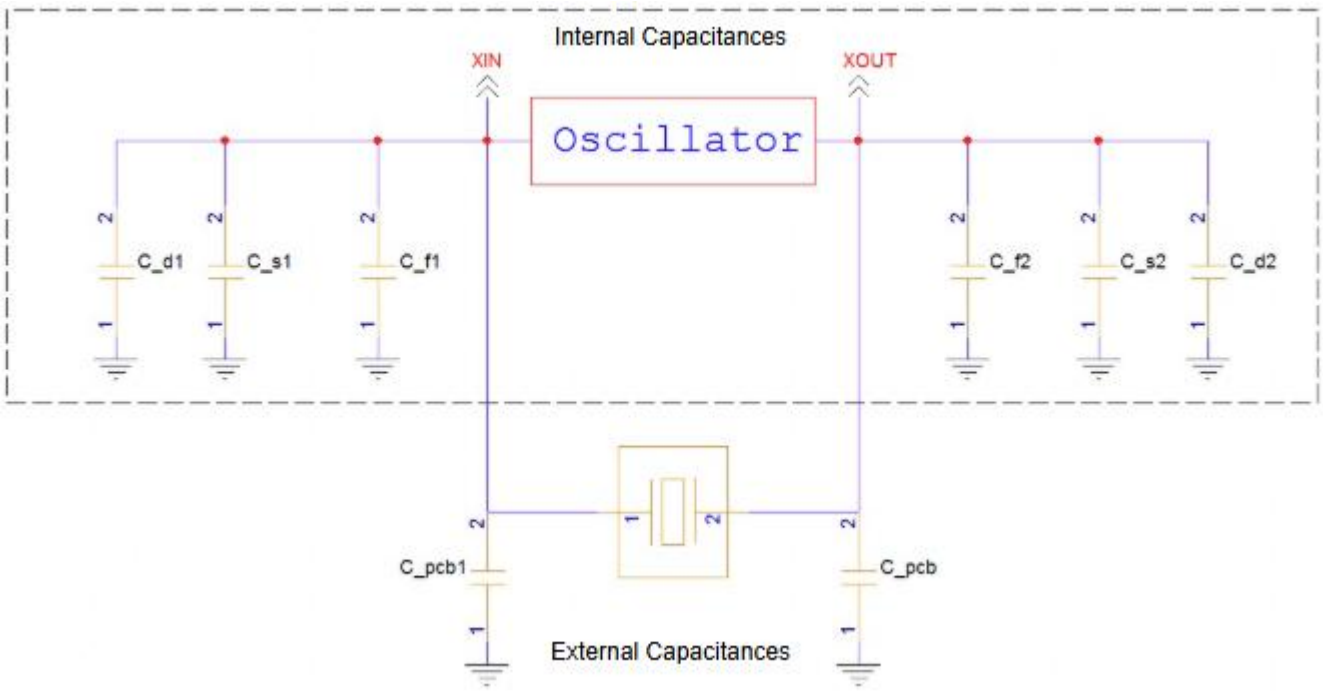


Figure 1. Crystal Capacitance

4. Equivalent Series Resistance

Equivalent series resistance (ESR) is the effective resistance component in series with the LC model of the crystal itself. ESR is determined by the crystal size, cut, frequency, and mode of vibration. An AT-cut crystal with a fundamental mode 50MHz resonance frequency in a 3225 package will have an ESR of around 50Ω, due to the size of crystal that easily fits into this package size. ESR subtracts from the negative resistance in the oscillator. A small package with a very small crystal may have too high an ESR for the driver, making it harder to start and sustain oscillation. A large package can fit a larger crystal (at the same cut, mode, and frequency) and will have a lower ESR.

ESR is proportional to the motional resistance (R_M) of the crystal and the shunt capacitance (C_O). It is also inversely proportional to the load capacitance (C_L). The ESR can be calculated as follows:

$$ESR = R_M\left(1 + \frac{C_O}{C_L}\right)^2$$

ESR is commonly expressed as a maximum value in ohms and is significant for two reasons.

1. The loop gain needed for an oscillator to start up and maintain oscillation is proportional to the ESR.
2. The drive level of an oscillator is proportional to the ESR. Therefore, if the ESR is too large, the crystal can have trouble oscillating or it can lead to a drive level which exceeds the rating that accelerates aging.

For FC4 and FC4W devices, the maximum ESR value that is recommended is 50Ω.

5. Drive Level

Confirm that the crystal maximum specified drive level will accommodate the drive level of the product. For FC4 and FC4W products, the typical drive strength is 160µW for a load capacitance of 8pF and 225µW for a load capacitance of 10pF. To prevent exceeding the drive level of the crystal, a series-damping resistor (R_S) can be added, but this series resistor will decrease the negative resistance, and loop gain will increase phase noise. It is preferred to select a crystal that can tolerate the required drive strength. Adding an R_S, populated with a 0-ohm shunt allows the use of a series resistance if a suitable crystal cannot be sourced.

Exceeding the drive level on the crystal accelerates aging. Renesas recommends measuring the power dissipated in the crystal to ensure it is below the crystal maximum specification. For more information, see the *Quartz Crystal Drive Level Application Note*.

R_S should be a small surface mounted part (example 0201 or 0402) to minimize stray capacitance.

6. Using a Crystal Oscillator (XO) with FC4 and FC4W

A crystal oscillator (XO) can be used in place of a crystal with FC4 or FC4W. To use a XO with FC4 or FC4W there are 2 options. The XO can be connected to the REF_CLK pin of FC4/FC4W, or it can be connected to the XIN pin (overdriving the crystal interface). The recommendation is the utilize the REF_CLK pin.

The REF_CLK pin accepts single ended singles with parameters defined in Table 2.

To connect a XO to the XIN pin of FC4 or FC4W, the crystal interface must be overdriven. When overdriving the crystal interface, the XOUT pin should be floated with no trace attached and the XIN input overdriven by an AC coupled LVCMOS driver, or, by one side of an AC coupled differential driver. The XIN pin is internally biased to 0.6V. The voltage swing on XIN should be between 0.5V peak-to-peak and 1.2V peak-to-peak; the slew rate should not be less than 0.2V/ns. The slew rate is calculated by measuring at the midpoint of the rising waveform using a window of ±200mV.

Note: The maximum allowable voltage on the XIN pin is 1.32V. Exceeding this voltage may damage the pin.

Figure 2 shows a 1.8V or 2.5V LVCMOS driver overdriving the XIN pin. For V_{DD} = 1.8V, considering the output impedance of the driver (R_O), the values of the series resistance (R_S) and R_1 should be chosen so that the voltage swing on XIN will be below 1.2V peak-to-peak. For V_{DD} = 2.5V, the sum of the output impedance of the driver (R_O) and the series resistance (R_S) can be made higher than R_1 so that the voltage swing on XIN will be below 1.2V peak-to-peak. Figure 3 shows one side of an LVPECL driver overdriving the XIN pin.

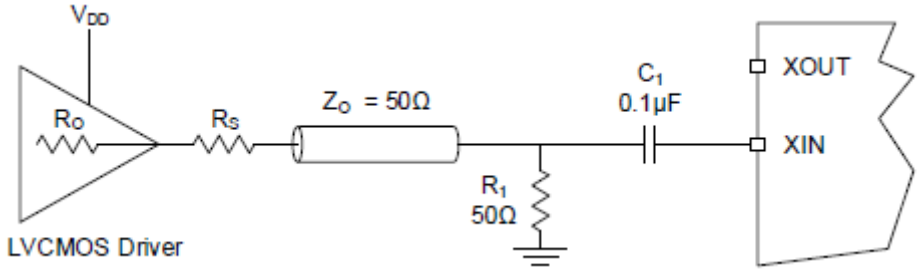


Figure 2. LVCMOS Driver to Crystal Input Interface

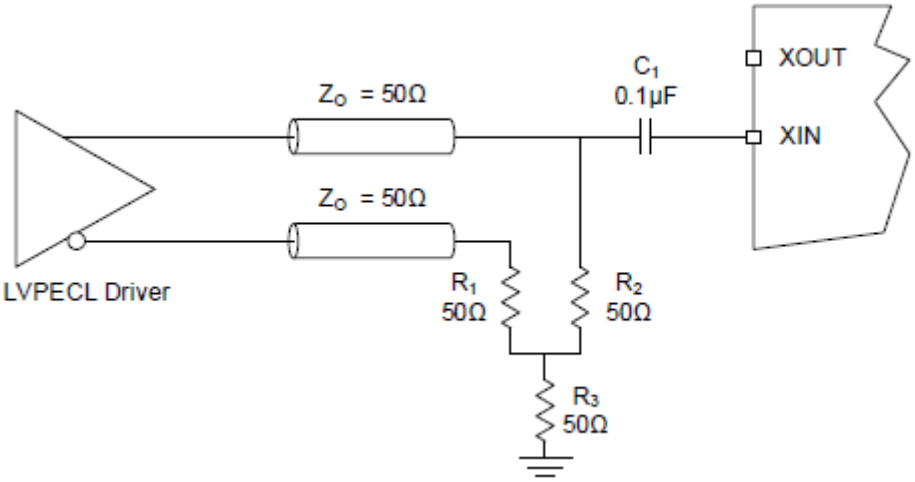


Figure 3. LVPECL Driver to Crystal Input Interface

It is recommended to AC couple the XIN pin of the FC4 or FC4W device by using a 0.1µF capacitor close to the device. The maximum XIN voltage is 1.3V peak-to-peak, and the recommended XIN voltage is 1.2V peak-to-peak. The XIN voltage can be controlled by using a 50ohm to ground voltage divider close to the device, but before the AC coupling capacitor. If the 50ohm to ground resistor does not provide enough resistance to meet the voltage limit, a series resistance can be place along the XIN trace between the XO and the 50ohm resistor. The value of the series resistance required will vary between XOs due to internal resistance from the XO. The series resistance can be calculated using voltage division. Figure 4 shows a generalized diagram of the path from the XO to the XIN pin on FC4 and FC4W.

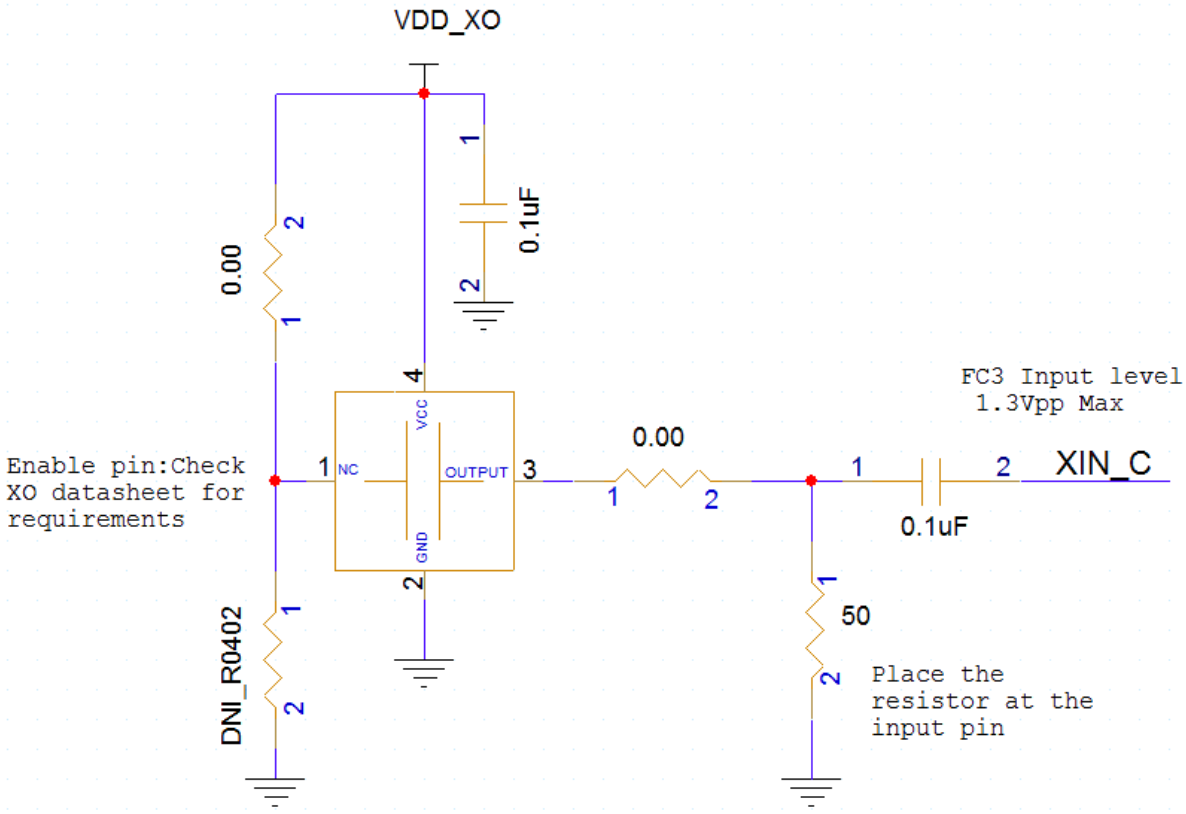


Figure 4. Generalization of Path from XO to the XIN Pin on FC4 and FC4W

7. Operating Temperature

Operating a crystal outside of its specified operating temperature range may prematurely age the crystal (increased ppm frequency change over time) or may damage the housing. A crystal operating outside of its temperature range can result in higher jitter frequency offset caused by the temperature. Crystal performance is typically not guaranteed beyond its specified temperature range. The recommended ambient operating temperature range for FC4 and FC4W devices is -40°C to +85°C.

8. Frequency Tolerance

Select a manufacturing tolerance (maximum deviation from the specified resonant frequency at room temperature) and frequency shift over the operating temperature range (often called frequency stability) that is acceptable for the application. When tight frequency tolerances (< 10ppm) over the operating temperature range are a requirement, it may be necessary to use a TCXO (temperature compensated crystal oscillator) or OCXO (oven-controlled crystal oscillator) instead. For FC4 and FC4W devices, the crystal input frequency tolerance range is ±450ppm.

Note: For FC4 and FC4W products, the crystal or crystal oscillator at XIN is the jitter reference. The preference is to use a crystal for low jitter instead of a generated clock signal.

9. Aging

Confirm that the crystal aging tolerance (ppm per year) meets the application requirement. Exceeding the drive level on the crystal, as well as shock, vibration and operating the crystal outside of its specified temperature range, accelerates aging. If the crystal will experience shock or vibration in its application, consider an oven-controlled SC-cut crystal that is more tolerant of vibration.

10. Recommended Crystals (XTAL) and Crystal Oscillators (XO)

Table 7 provides a list of acceptable crystals for applications using a FC4 or FC4W device. Table 8 provides a list of acceptable crystal oscillators for applications using a FC4 or FC4W device.

Table 7. Recommended Crystals for FC4 and FC4W Applications

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	ESR (Ω)	CL (pF)	Typical Drive Level (µW)	Max. Drive Level (µW)	Freq. Tolerance (ppm)	Freq. Stability (ppm)	Aging (ppm/ year at 25°C)	Temp. Range (ºC)
NDK	XTAL	EXS00A-CS15517	2.0 × 1.6	49.152	50	9	10	200	±27			-40 to +85
NDK	XTAL	EXS00A-CS16476	2.0 × 1.6	50	30	9	10	200	±25			-40 to +85
NDK	XTAL	EXS00A-CS15524	2.0 × 1.6	54	30	9	10	200	±40			-40 to +85
NDK	XTAL	EXS00A-CS15287	2.0 × 1.6	60	30	9	10	200	±25			-40 to +85
NDK	XTAL	EXS00A-CS15295	2.0 × 1.6	62.5	35	9	10	200	±30			-40 to +85
NDK	XTAL	EXS00A-CS15306	2.0 × 1.6	68	50	9	10	200	±30			-40 to +85
NDK	XTAL	EXS00A-CS15308	2.0 × 1.6	73	50	9	10	200	±30			-40 to +85
NDK	XTAL	EXS00A-CS15310	2.0 × 1.6	78.125	50	9	10	200	±30			-40 to +85
TXC	XTAL	7M49172003	3.2 × 2.5	49.152	20	8	100	300	±10	±15	±1	-40 to +85
TXC	XTAL	8Y49172005	2.0 x 1.6	49.152	30	12	100	300	±10	±15	±1	-40 to +85
TXC	XTAL	8Y49172006	2.0 x 1.6	49.152	30	8	100	300	±10	±15	±1	-40 to +85
TXC	XTAL	7M50072003	3.2 × 2.5	50	22	8	100	200	±10	±15	±1	-40 to +85
TXC	XTAL	8Y50072010	2.0 x 1.6	50	30	8	100	200	±10	±15	±1	-40 to +85
TXC	XTAL	8Y49172005	2.0 × 1.6	49.152	30	12	100	300	±10	±15	±1	-40 to +85
TXC	XTAL	7M54072002	3.2 × 2.5	54	50	8	100	200	±10	±15	±1	-40 to +85
TXC	XTAL	8Z54072008	2.5 x 2.0	54	40	8	100	200	±10	±10	±1	-40 to +85
TXC	XTAL	8Y54072007	2.0 x 1.6	54	40	8	100	300	±25			-40 to +85
TXC	XTAL	7M60072004	3.2 x 2.5	60	25	8	100	300	±10	±20	±1	-40 to +95
TXC	XTAL	8Y60072004	2.0 x 1.6	60	40	8	100	300	±20	±30	±1	-40 to +105
TXC	XTAL	8Y60072005	2.0 × 1.6	60	40	8	100	300	±25			-40 to +85
TXC	XTAL	7M62572001	3.2 x 2.5	62.5	50	8	100	300	±10	±20	±1	-40 to +85
TXC	XTAL	8Y62572001	2.0 x 1.6	62.5	40	8	100	300	±20	±30	±1	-40 to 105
TXC	XTAL	8Y62572002	2.0 × 1.6	62.5	40	8	100	300	±25			-40 to +85
TXC	XTAL	8Z62572001	2.5 × 2.0	62.5	40	8	100	300	±25			-40 to +85
TXC	XTAL	8Y68072001	2.0 × 1.6	68	40	8	100	300	±25			-40 to +85

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	ESR (Ω)	CL (pF)	Typical Drive Level (µW)	Max. Drive Level (µW)	Freq. Tolerance (ppm)	Freq. Stability (ppm)	Aging (ppm/ year at 25°C)	Temp. Range (ºC)
TXC	XTAL	8Y73072002	2.0 × 1.6	73	40	8	100	300	±25			-40 to +85
TXC	XTAL	8Y73072001	2.0 x 1.6	73	40	8	100	300	±20	±30	±1	-40 to +105
TXC	XTAL	8Y78172001	2.0 × 1.6	78.125	40	8	100	300	±20	±30	±1	-40 to +105
TXC	XTAL	8Y78172002	2.0 × 1.6	78.125	40	8	100	300	±25			-40 to +85
KYOCERA	XTAL	CX2016SA50000	3.2 × 2.5	50	50	8	10	200	±15	±50	±1	-40 to +125

Table 8. Recommended Crystal Oscillators for FC4 and FC4W Applications

Manufacturer	Type	Part Number	Product Size (mm)	Frequency (MHz)	Voltage (V)	Total Frequency Stability (ppm)	Temperature Range (°C)
TXC	XO	8W48070009	2.5 x 2.0	48	3.3	±25	-40 to +85
TXC	XO	8W48070007	2.5 x 2.0	48	3.3	±50	-40 to +105
TXC	XO	8W49170004	2.5 × 2.0	49.152	3.3	±25	-40 to +85
TXC	XO	8W50070009	2.5 x 2.0	50	3.3	±25	-40 to +85
TXC	XO	8W50070006	2.5 x 2.0	50	3.3	±50	-40 to +105
TXC	XO	8W54070002	2.5 x 2.0	54	3.3	±50	-40 to +105
TXC	XO	8W62570006	2.5 × 2.0	62.5	3.3	±50	-40 to +105
TXC	XO	8W62570007	2.5 x 2.0	62.5	3.3	±25	-40 to +85
TXC	XO	8W68070001	2.5 × 2.0	68	3.3	±50	-40 to +105
TXC	XO	8W73070001	2.5 × 2.0	73	3.3	±50	-40 to +105
NDK	XO	RNA5025A	2.5 × 2.0	48	3.3	±50	-40 to +105
NDK	XO	RNA5029A	2.5 × 2.0	49.152	3.3	±50	-40 to +105
NDK	XO	RNA5027A	2.5 × 2.0	50	3.3	±50	-40 to +105
NDK	XO	RNA5024A	2.5 × 2.0	54	3.3	±50	-40 to +105
NDK	XO	CUS5094F	2.5 × 2.0	56	3.3	±50	-40 to +105
NDK	XO	RNA5024E	2.5 × 2.0	62.5	3.3	±50	-40 to +105
NDK	XO	RNA5024F	2.5 × 2.0	68	3.3	±50	-40 to +105
NDK	XO	RNA5024G	2.5 × 2.0	73	3.3	±50	-40 to +105
Taitien	XO	R0093-L-001-3	2.5 × 2.0	54	3.3	±25	-40 to +85
Taitien	XO	R0093-L-002-3	2.5 × 2.0	62.5	3.3	±25	-40 to +85
Taitien	XO	R0093-L-003-3	2.5 × 2.0	68	3.3	±25	-40 to +85

11. Revision History

Revision	Date	Description
1.00	Oct 29, 2026	Initial release.

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