Characteristics of Renesas GaN Power Switches

This document describes the characteristics of Renesas GaN Power Switches, including the cascode structure and the operation space. The ability of the GaN Power Switch to operate in three quadrants with a low reverse recovery charge allows superior performance in comparison to existing Silicon technology

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1. INTRODUCTION

Renesas Gallium Nitride (GaN) Power Switches comprise a normally-off low voltage (LV) Silicon (Si) MOSFET and a normally-on high voltage GaN High Electron Mobility Transistor (HEMT) in cascode configuration (Figure 1).

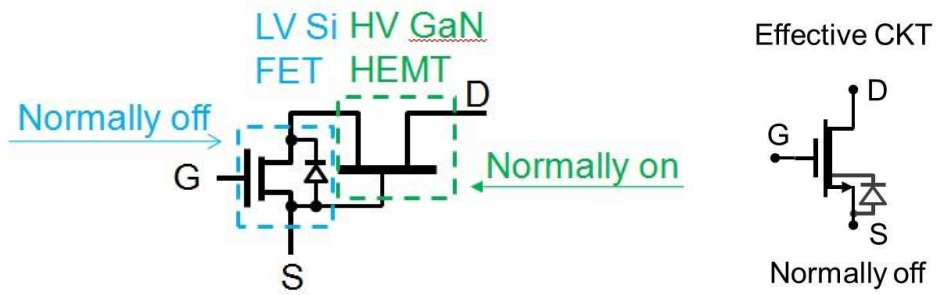

Figure 1: Renesas GaN Switch

Packaged in this configuration, the Si MOSFET and the GaN HEMT together behave as a single transistor- the GaN switch. The gate and the source of the GaN switch are given by the gate and the source of the Si MOSFET, while the drain of the GaN switch is given by the drain of the GaN HEMT. In Renesas's standard packages, the drain of the Si MOSFET, the Source of the GaN HEMT, and the gate of the GaN HEMT are not accessible from the outside of the package.

In applications, Renesas GaN switches behave like ultra-fast FETs with low-charge body diodes.

The "body diode" is a p-n junction that is inherent to MOSFETs and is in parallel to the MOSFET channel. The body diode can conduct current from the source to the drain (the MOSFETs' reverse direction) when the MOSFET is turned off, and can act as a freewheeling diode in applications.

However, as a bi-polar device, the body diode stores minority carriers in its forward conduction mode. Especially in high voltage MOSFETs, where a large amount of minority carriers is stored during forward conduction, this leads to poor reverse characteristics of the MOSFET such as high reverse recovery current and long reverse recovery time.

In contrast, Renesas GaN switches consist of a HV GaN HEMT, which is a majority carrier device, and a LV MOSFET, which inherently has only little stored minority carriers during forward conduction. Therefore, Renesas GaN switches store only a small amount of minority carriers during reverse conduction while providing the same reverse conductance as MOSFETs. Without the losses of a high voltage body diode, Renesas GaN switches demonstrate great performance advantages with low recovery charge and short recovery time. In addition, Renesas GaN switches operate extremely fast with fall and rise times <10 ns, therefore minimizing switching losses in applications.

2. OPERATION OF GAN SWITCHES

To better understand the operation of the GaN switch (Fig. 1), three modes of operation can be distinguished:

1. Forward Blocking (V_{GS}=0, V_{DS}>0)
    a. $0<V_{DS} < -V_{t,GaN}$
    b. $0<-V_{t,GaN}<V_{DS}$
2. Forward conduction ($V_{GS} > V_{t,Si}$,V_{DS}>0)

3. Reverse conduction (V_{DS}<0)
    a. Reverse Turn on
        i. V_{GS}=0
        ii. V_{GS}>$V_{t,Si}$
    b. Reverse Turn Off

where $V_{t,Si}$ is the threshold voltage of the LV Si MOSFET, the threshold voltage of the GaN HEMT $V_{t,GaN}$ <0, the drain voltage V_{DS}, the drain current I_D, and $V_{GS,GaN}$ + $V_{DS,Si}$=0.

2.1 Forward Blocking

2.1.1 V_{GS}=0, 0 < V_{DS} < -$V_{t,GaN}$

At V_{GS}=0, the Si MOSFET is switched off, and no current flows either through the channel of the Si MOSFET or through the channel of the GaN HEMT (I_D=0). As V_{DS} < -$V_{t,GaN}$ and I_D~0, the drain potential of the Si MOSFET is equal to the drain potential of the GaN switch, $V_{DS,Si}$ = V_{DS}. In this operating area, the entire drain voltage V_{DS} of the switch is blocked by the Si MOSFET.

2.1.2 V_{GS}=0, 0 < -$V_{t,GaN}$ < V_{DS}

As V_{DS} increases, the gate voltage of the GaN HEMT becomes more negative with respect to its source voltage, gradually turning off the GaN HEMT. At V_{DS} =–$V_{t,GaN}$, the GaN HEMT is turned off. For voltages V_{DS}>–$V_{t,GaN}$, the voltage drop across the GaN HEMT is V_{DS}+$V_{t,GaN}$, with $V_{t,GaN}$ <0.

2.2 Forward Conduction

V_{GS}> $V_{t,Si}$, I_D,V_{DS} > 0

With the Si MOSFET turned on (V_{GS}>$V_{t,Si}$), the voltage drop across the GaN switch in the linear region is

$$V_{DS}=I_D (R_{DS(on),Si} + R_{DS(on),GaN}) \quad \text{(Eq. 1)}$$

where $R_{DS(on),Si}$ and $R_{DS(on),GaN}$ are the on-resistance of the Si MOSFET and the GaN HEMT, respectively.

2.3 Reverse Conduction (V_{DS} < 0)

2.3.1 Reverse Turn On

2.3.1.1 V_{DS} < 0, V_{GS}=0

When the GaN switch is turned off (the LV Si MOSFET is turned off) and a reverse voltage is applied to GaN switch, a current flows through the body diode of the LV Si MOSFET and the channel of the normally-on HV GaN HEMT (Fig. 2).

The reverse voltage drop V_{SD} across the GaN switch during this reverse conduction is the sum of the Si MOSFETs' body diode voltage drop V_{SD-Si}, and the conduction voltage drop across the GaN channel. The voltage drop across the GaN channel can be described as the product of the current I_F, and the Drain-Source On-resistance $R_{DS(on)-GaN}$ of the GaN HEMT. Therefore,

$$V_{SD} = V_{SD-Si} + I_F*R_{DS(on)-GaN} \quad \text{(Eq. 2)}$$

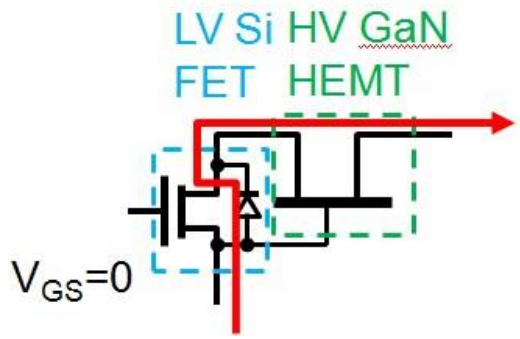

Figure 2: Reverse turn-on of Renesas GaN Switch, V_{GS} =0V

2.3.1.2 V_{DS} < 0, V_{GS}>$V_{t,Si}$

As (Eq.2) shows, the reverse voltage drop of the Renesas GaN switch is a function of current, and is higher than the Si MOSFET's body diode voltage drop. However, to improve the performance in the application, the reverse voltage drop can be reduced by turning on the low voltage Si MOSFET during reverse conduction. This is typically done after a small dead time to avoid shoot through.

By applying a gate voltage higher than the threshold voltage $V_{t,Si}$ of the GaN switch (here V_{GS}>4V), the LV Si MOSFET is turned on and the reverse current I_F flows through the Si channel (with its channel resistance $R_{DS(on),S}$) and the GaN channel (with $R_{DS(on),GaN}$) (Figure 3). Therefore, at reasonable current levels, I_F*$R_{DS(on),Si}$ < $V_{SD\text{-}Si}$, and the reverse voltage drop across the GaN switch reduces to

$$V_{SD} = I_F * (R_{DS(on),GaN}+R_{DS(on),Si}) \qquad \text{(Eq. 3)}$$

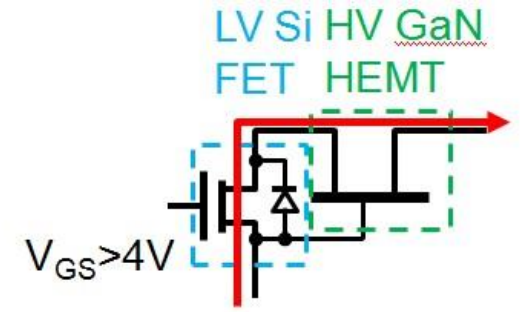

Figure 3: Reverse turn-on of Renesas GaN Switch, V_{GS}=4V

2.3.2 Reverse Turn Off (Reverse Recovery Behavior)

To demonstrate the smaller reverse recovery losses of the GaN switch in comparison to high voltage MOSFETs, the reverse recovery of the GaN switch can be tested.

Figure 4 shows the reverse recovery test circuit that can be used for this test. It consists of the device under test (DUT), the inductor L1 and the control switch Q1.

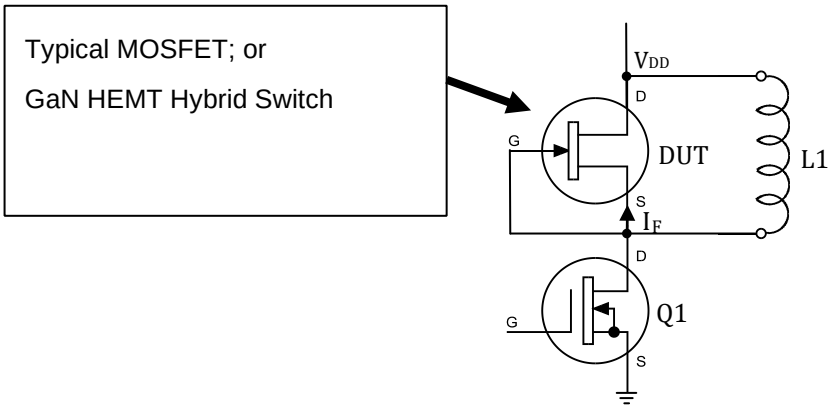

Figure 4

The test starts when Q1 is turned on. Subsequently, a current establishes through L1 and Q1, with the reverse current of the DUT I_F=0 (Figure 4). Q1 is then turned off, but the current remains flowing through L1 and creates I_F≠0. Therefore, modulating Q1 allows setting the current I_F that flows from the inductor to the source then drain of the DUT. To observe the reverse recovery of the DUT after establishing I_F, Q1 is turned on again and the DUT transitions from reverse conduction to forward blocking.

To better understand the advantage of the GaN switch over existing Silicon technology, reverse recovery tests have been performed on a 600V Renesas GaN switch and a 600V CFD2-type (low Qrr design) CoolMOS Si MOSFET with comparable on-resistances. Fig 5.2 and Fig 5.1 show the reverse turn-off waveforms of the GaN switch and the MOSFET, respectively.

Both DUTs were tested at an initial current I_F=9A and a reverse bias voltage V_{DD}=400V. While the Renesas GaN switch was tested at 450A/us with little ringing, the CoolMOS was not stable at 450A/us. Therefore, its turn off di/dt was reduced to 100A/us for stability. (Further tests showed, that the Q_{rr} of the GaN switch is unchanged with different di/dt from 100 A/us to 480 A/us, therefore allowing a comparison between the two measurements.)

The test waveforms in Fig. 5 and Fig 5.1 show the DUTs recovery charges Q_{rr} of 40 nC and 1000 nC for the GaN switch and low Q_{rr} MOSFET, respectively. The GaN switch has an impressively low Q_{rr} that is 25 times less than the Q_{rr} of the fast recovery design CoolMOS.

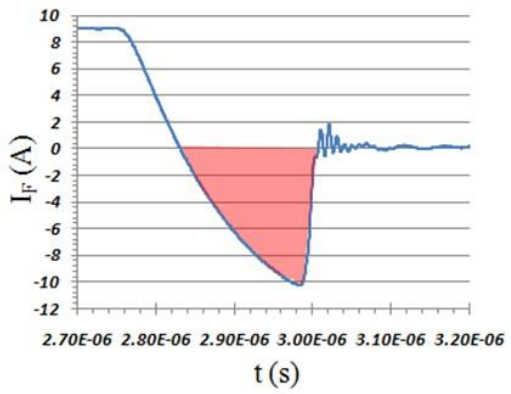

Fig. 5.1 Reverse turn-off of CoolMOS, 9A, 400V, 100A/us; Q_{rr} = 1000nC

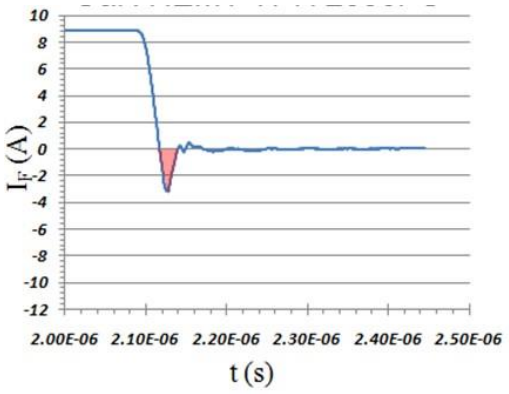

Fig. 5.2 Reverse turn-off of Renesas GaN device, 9A, 400V, 450A/us; Q_{rr} = 40nC

To further analyze the reverse recovery charge of the GaN switch, the reverse recovery charge can be split into two components: First, the capacitive charge of the GaN HEMT, and second, the reverse recovery charge of the low voltage Si MOSFET.
At I_F=0A, the reverse recovery of the Si MOSFET is zero, therefore any observed current can only stem from discharging the switch's capacitance Q_C. Fig. 66.1 and Figure 6.2 show the measurements for I_F=0A at different switch speeds of Q1. It can be observed that Qc ~35nC, which constitutes about 86% of total Q_{rr}. In other words, the minority charge component is only 14% of the overall Q_{rr}.

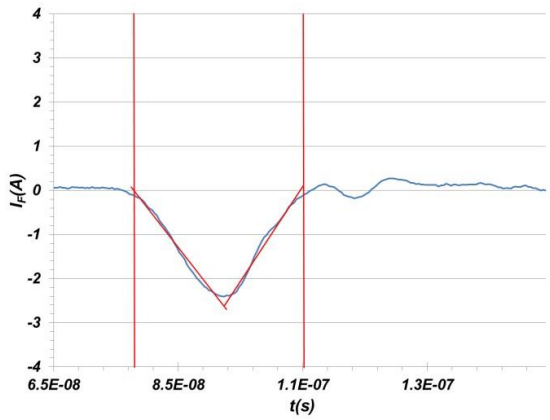

Fig. 6.1 di = 2.6A, dt = 26.9ns, Q_C = 35.6nC

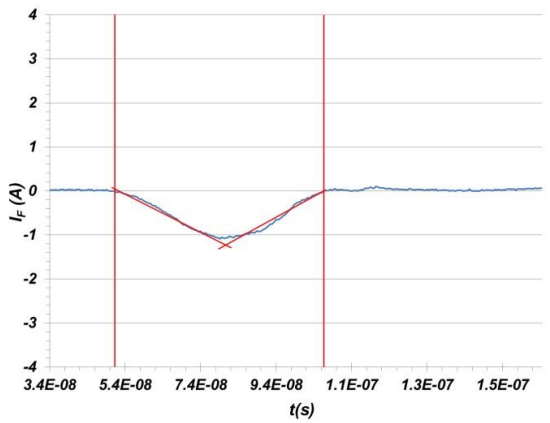

Figure 6.2 di = 1.25A, dt = 55.2ns, Q_C = 34.5nC

3. CONCLUSION

Renesas's GaN switches are capable of three modes of operation including forward blocking, forward conduction, and reverse conduction. Their switching is very fast with remarkably superior reverse turn-off characteristic compared to Si MOSFETs. These characteristics make the GaN device especially suitable for hard-switched diode-free bridge applications, such as motor-drive inverters, PV inverters, totem-pole PFCs, and other related applications.