Capacitive Touch Sensor Microcontrollers

Overview of CTSU Functional Safety Self Test

Introduction

This application note describes the software for CTSU functional safety self test.

For the operating principle of CTSU, refer to Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide

Target Devices

RX Family, RA Family, and RL78 Family MCUs embedding the CTSU

(“CTSU” includes CTSU2, CTSU2L, CTSU2La, CTSU2SL, CTSU2SLa, and so on)

From the next page, please refer to CTSU1 for CTSU/CTSUa/CTSUb and CTSU2 for CTSU2L/CTSU2La/CTSU2SL/CTSU2SLa.

Target Development Environments

- IDE e^2 studio 2025-12 or later
- Renesas QE for Capacitive Touch V4.3.0 or later
- FSP V6.5.0 or later
- FIT V3.30 or later
- SIS V2.30 or later

Contents

1. Overview

Today, as automatic electronic control systems continue to expand into many diverse applications, the requirement of reliability and safety are becoming an ever-increasing factor in system design.

For example, the introduction of the IEC60730 safety standard for household appliances requires manufacturers to design automatic electronic controls that ensure safe and reliable operation of their products.

In IEC 60730, automatic electronic control functions are classified into the following classes.

Class A

Control functions that are not intended to be relied upon for the safety of the equipment

Examples: Room thermostats, humidity controllers, lighting controllers, timers, and switches

Class B

Control functions that are intended to prevent unsafe operation of the controlled equipment

Examples: Thermal cutoff and door locking for laundry machines

Class C

Control functions that are intended to prevent special hazards

Examples: Automatic burner control and thermal cutoff for sealed equipment

Appliances such as washing machines, dishwashers, dryers, refrigerators, freezers, and Cookers / Stoves will tend to fall under the classification of Class B.

This application note describes the CTSU diagnostic software and supports compliance with IEC 60730 Class B.

The CTSU-embedded MCUs include functions to diagnose its internal circuits. This software controls these internal circuits and provides APIs for performing diagnosis. These APIs are implemented as part of the CTSU modules in the RX Family Firmware Integration Technology (FIT) | Renesas, the RA Family Flexible Software Package (FSP) | Renesas, and the RL78 Family Software Integration System (SIS) for MCUs equipped with the CTSU.

The diagnostic items differ between the CTSU1-embedded MCUs and the CTSU2-embedded MCUs.

This software provides seven types of diagnostics for CTSU1 and nine types of diagnostics for CTSU2. For details, refer to “2. CTSU1 Diagnostic Function” and “3. CTSU2 Diagnostic Function”.

The diagnosis can be performed by calling API functions, in addition to normal measurement operations. For details, refer to “4. API Specifications” and “5. Sample Application Flowchart”.

When using the diagnosis function, it is recommended to output the config using “QE for Capacitive Touch”. By using the QE, you can create a project, set a configuration, and output a sample application. Refer to “6. Project Creation using QE for Capacitive Touch” for details on the setting procedures.

In addition, it is possible to accelerate the acquisition of IEC/UL60730 certification for final products which support capacitive touch by using "Renesas Functional Safety Solutions for Home Appliances" together. (It is also possible to use your own program instead of Renesas Functional Safety Solutions for Home Appliances.)

ASIL-B by implementing both this sample program and another sample program. For detailed information on the functional safety for automotive, refer to ISO 26262 Functional Safety for Automotive | Renesas.

2. CTSU1 Diagnostic Function

This chapter describes the specifications of the diagnostic function implemented in CTSU1. Seven diagnostic items are provided for the target internal circuits, and each item has different execution timing and operating conditions. This chapter is divided into sections for each diagnostic item and describes the measurement operation, the execution condition, and the determination method for each. For the list of diagnostic items and their execution timing, refer to Table 2-1. Note that the diagnostic process described in this chapter covers the measurement start, measurement operation, and acquisition of measurement data.

Figure 2-1 shows a circuit diagram for the CTSU1 diagnostic function. In addition, when using an MCU other than one incorporating CTSUb, the TS pin used for “Sensor Offset Diagnosis (with TS pin)” must be connected to ground through a 560 Ω resistor and a 27 pF or 33 pF capacitor. For details, refer to section 2.6.

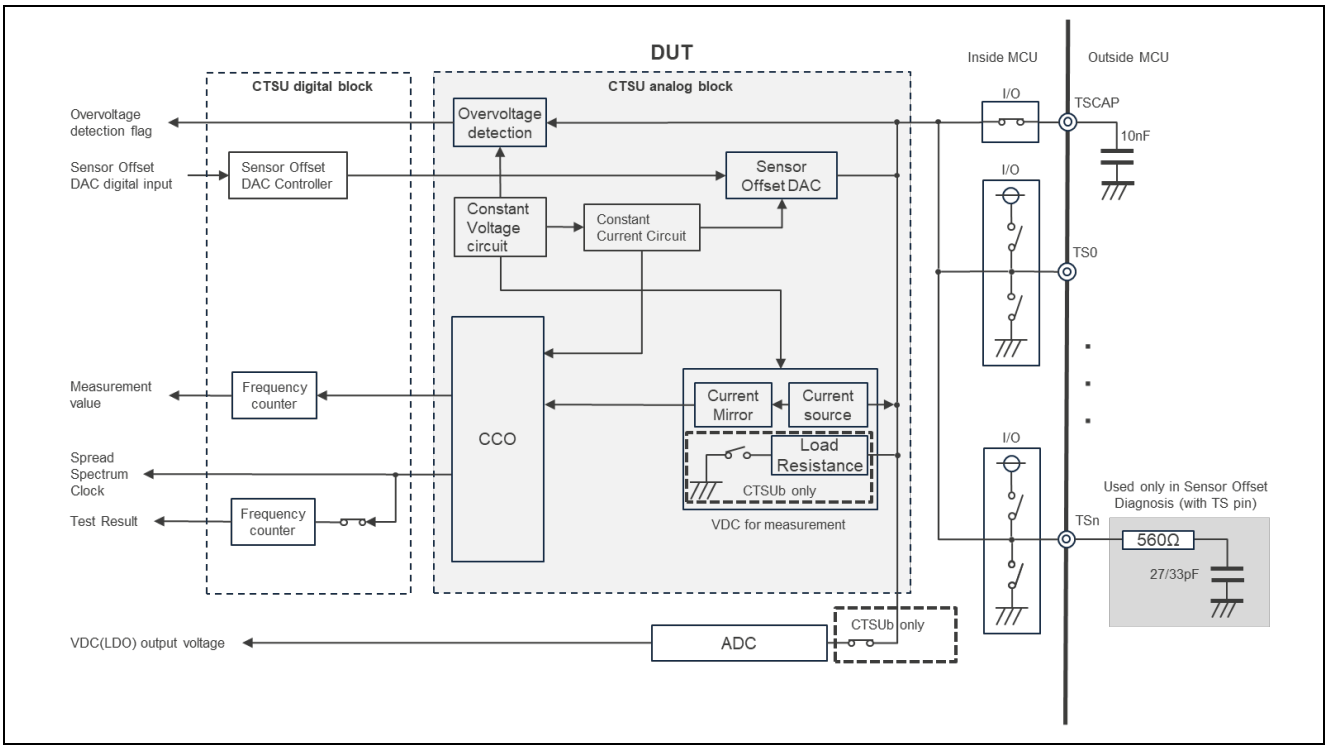

Figure 2-1 Circuit Diagram for CTSU1 Diagnostic Function

Table 2-1 Diagnostic Items and Execution Timing

Order	Diagnostic Name	One-time or Repeat Note 1
1	Output voltage diagnosis Note 3	Repeat
2	Overvoltage detection diagnosis	Repeat
3	CCO high diagnosis	Repeat
4	CCO low diagnosis	Repeat
5	SSCG diagnosis	Repeat
6	Sensor offset diagnosis (with TS pin) Note 3	Repeat
7	Sensor offset diagnosis (without TS pin) Note 2	Repeat

Note 1: “One-time” assumes diagnosis is performed once after reset. “Repeat” assumes periodic measurements.
2: These diagnostics are supported only on MCUs with CTSUb.
3: This diagnostic is not supported on MCUs with CTSUb.

In this chapter, when evaluating a CTSU1 diagnostic function under multiple conditions, the term “Test” refers to an individual evaluation unit corresponding to each condition (e.g., Test 1, Test 2)

Table 2-2 shows the settings for CTSU1 power supply operation mode. In this application note, the CTSU1 operating voltage states selected by the CTSUATUNE0 bit are referred to as Normal (NM) mode and Low Voltage (LV) mode.

Table 2-2 CTSU1 Power Supply Operating Mode Settings

CTSU Power Supply Operating Mode	CTSUCR1.CTSUATUNE0	MCU Power Supply Voltage (V)
NM mode	0	2.4 to 5.5
LV mode Note	1	1.8 to 5.5

Note: Register and bit field specifications vary depending on the product used. For details on how to configure the registers, refer to the User’s Manual (Hardware) for the MCU in use.

The CTSU1 diagnostic function assumes the use in NM mode. Set the CTSUCR1.CTSUATUNE0 bit to “0”.

In principle, the register settings described in this chapter must not be changed, except for those related to the MCU power supply voltage, ADC thresholds, and the TS pin used to connect an external capacitor for Sensor Offset Diagnosis (with TS pin).

This diagnosis function uses the ADC module. Therefore, if the ADC is used in the user system, conflicts with ADC processing may occur during the diagnostic operation. Before executing the diagnostic function, stop the ADC on the user side or control it so that no conflict occurs with the diagnosis function.

2.1 Output Voltage Diagnosis

Figure 2-2 shows the circuit for output voltage diagnosis. The TSCAP pin is connected to a current source used for CTSU measurement, and the TSCAP voltage is regulated to a constant level. The diagnosis evaluates this TSCAP voltage when the current from this source flows through the load resistance. The internally connected TSCAP voltage is measured using the ADC, and a current source failure is diagnosed based on whether the measured value falls within the specified range.

The current CTSU1 output voltage diagnosis assumes a fixed MCU power supply voltage of 5.0 V. Therefore, if the MCU power supply voltage in the user system differs from 5.0 V, the user must change the ADC reference voltage (Vref) and the corresponding threshold for determination according to the system conditions. Set the threshold considering the ADC measurement error given in the User's Manual (Hardware) for the MCU in use.

Note: This diagnostic is supported only on CTSUb.

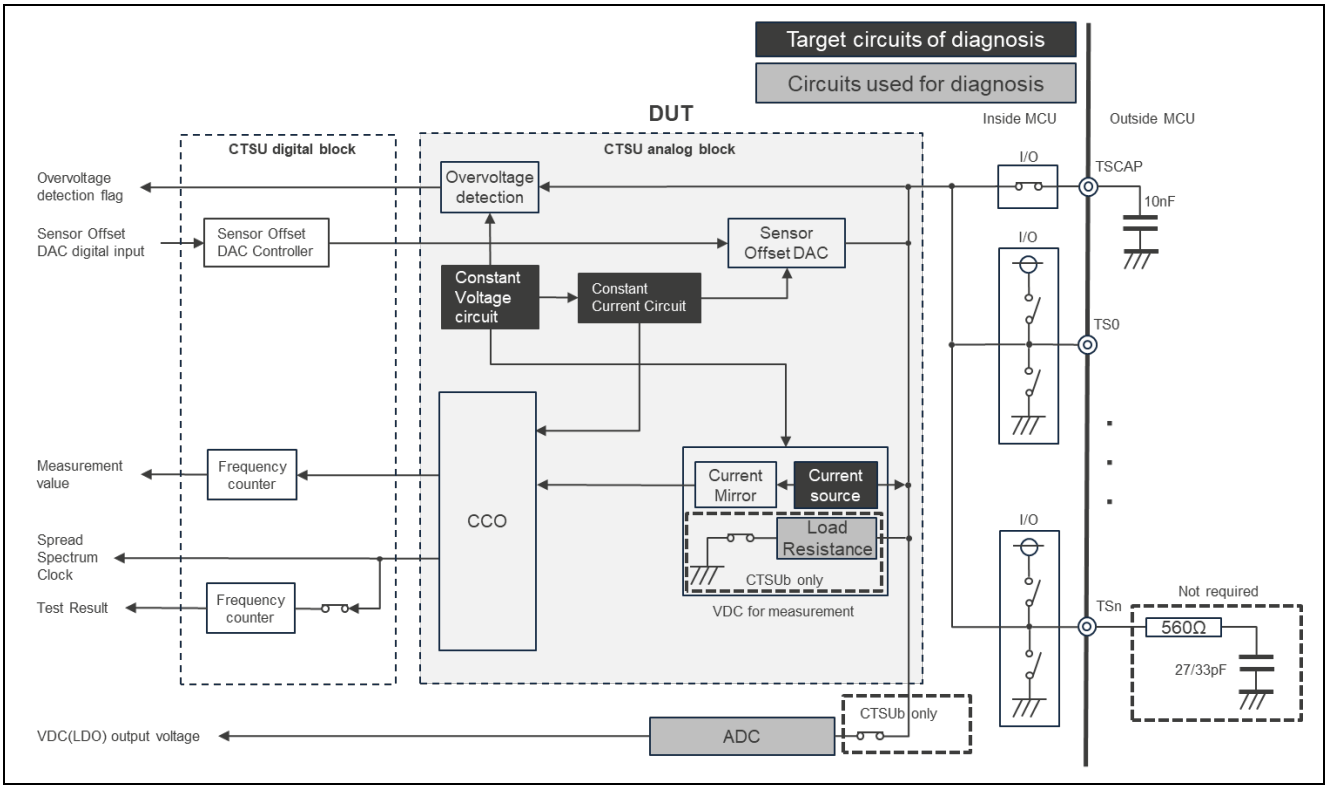

Figure 2-2 Circuit Diagram for Output Voltage Diagnosis

2.1.1 Measurement

For each current measurement range, ADC measurements are performed using the MCU power supply voltage as Vref and the TSCAP voltage as the input voltage Vin to calculate the TSCAP voltage. For the current measurement range, refer to "3.4 Current Range" in the "QE for Capacitive Touch Advanced Mode Parameter Guide"

Table 2-3 and Table 2-4 show the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-3 Register Settings for Output Voltage Diagnosis (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock setting
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	11b	Calibration setting
	CTSUDRV	1	
	CTSUTSOC	1	
CTSUDCLKC	CTSUSSMOD[1:0]	00b	High-frequency noise reduction setting
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSO0	CTSUSO[9:0]	0x000	Offset current setting
	CTSUSNUM[5:0]	000111b	Measurement count setting: 8

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to “0”.

Table 2-4 Register Settings during Output Voltage Diagnostic Operation

Test	Register	Bit	Value
1	CTSUCR1	CTSUATUNE1	0
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	1
2	CTSUCR1	CTSUATUNE1	0
	CTSUERRS	CTSUR01EN	1
		CTSUR02EN	0
3	CTSUCR1	CTSUATUNE1	1
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	1
4	CTSUCR1	CTSUATUNE1	1
	CTSUERRS	CTSUR01EN	1
		CTSUR02EN	0

2.1.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2)

2.1.3 Determination

Check whether the average measured value falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

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2.2 Overvoltage Detection Diagnosis

Figure 2-3 shows the circuit for overvoltage detection diagnosis. A circuit for detecting overvoltage at the TSCAP pin is provided in the device. When the TSCAP voltage exceeds a specified level, an overvoltage condition is detected, the measurement operation is interrupted, and the internal circuitry is protected.

This diagnosis verifies the overvoltage detection circuit. Normal-voltage and overvoltage conditions are reproduced using the sensor offset DAC and the load resistance, and the ability of the circuit to correctly distinguish between these conditions is verified.

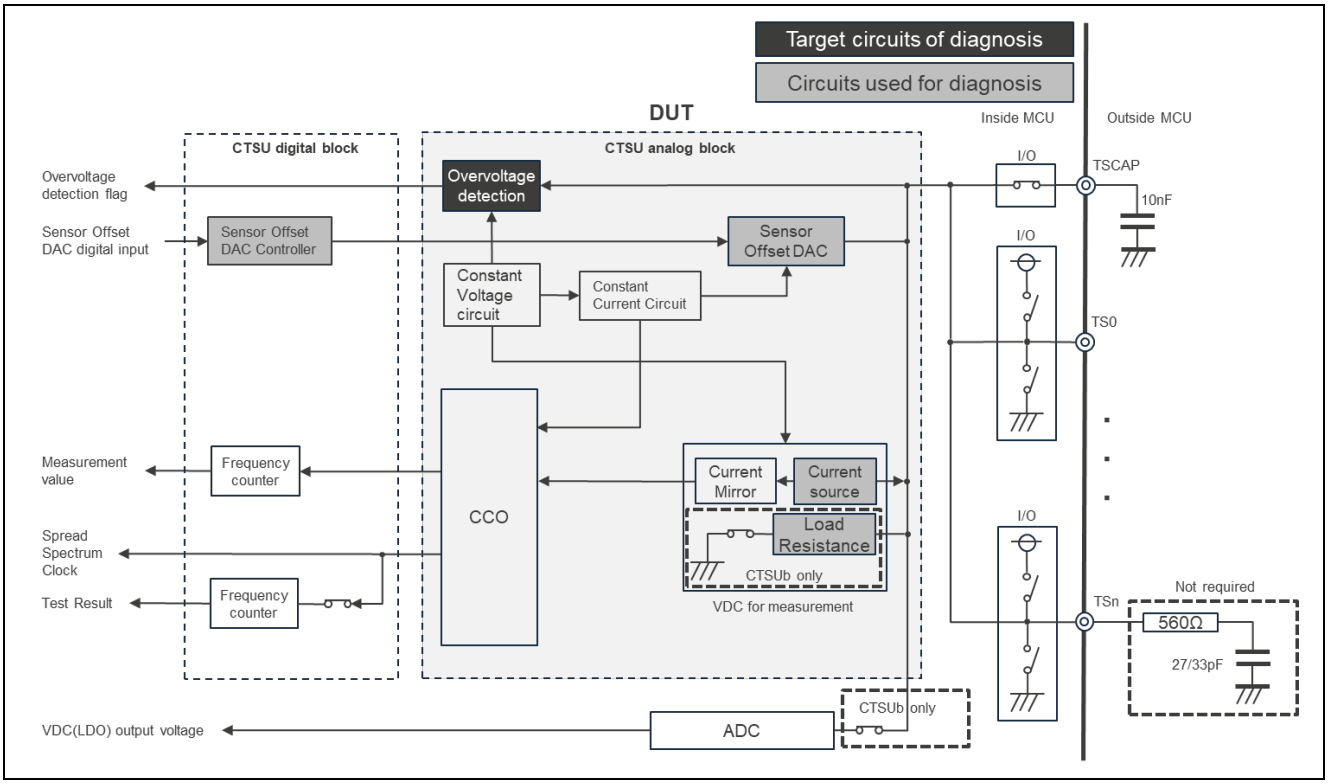

Figure 2-3 Circuit Diagram for Overvoltage Detection Diagnosis

2.2.1 Measurement

After setting the sensor offset to 0x3FF, measurement values are obtained to verify that an overvoltage is correctly detected (CTSUICOMP = 1) under overvoltage conditions.

Table 2-5 shows the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-5 Register Settings for Overvoltage Detection Diagnosis (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock setting
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	10b	Calibration setting
	CTSUDRV	1	
	CTSUTSOC	1	
CTSUSSC	CTSUSSDIV[3:0]	111b	Spread-spectrum clock division setting
CTSUDPRS	CTSUSOFF	0	High-frequency noise reduction setting
CTSUDCLKC	CTSUSSMOD[1:0]	00b	
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSOx	CTSUSO[9:0]	0x3FF	Offset current setting
	CTSUSNUM[4:0]	00111b	Measurement count setting: 8

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to “0”.

2.2.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2)

2.2.3 Determination

At the measurement completion interrupt, processing is performed according to the result.

If no overvoltage is detected (CTSUICOMP = 0) under overvoltage conditions, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_VOLTAGE. If an overvoltage is detected (CTSUICOMP = 1), R_CTSU_Diagnosis returns FSP_SUCCESS.

2.3 CCO High Diagnosis

Figure 2-4 shows the circuit diagram for CCO high diagnosis. CTSU1 repeatedly charges and discharges the capacitance of the electrode over a fixed period, the current mirror output proportional to the charging current is input to a current-controlled oscillator (CCO). The CCO generates a frequency signal corresponding to the input current, and this signal is counted by the counter. The resulting count is used as the CTSU measurement value.

In this diagnosis, by inputting a current corresponding to the upper limit of the CCO input to the CCO, the CCO is verified based on whether the measured value falls within the specified range.

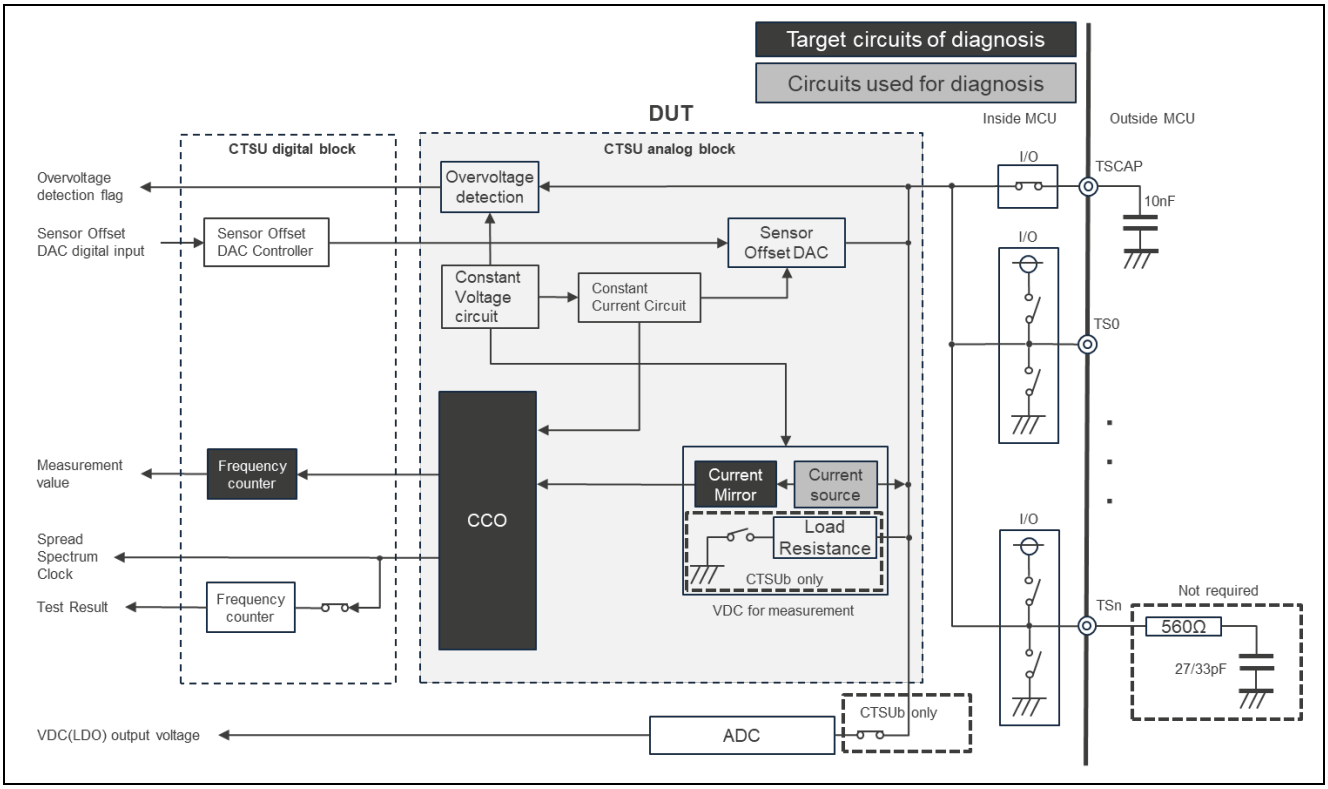

Figure 2-4 Circuit Diagram for CCO High Diagnosis

2.3.1 Measurement

A specified current is input to the CCO to obtain the measurement value.

Table 2-6 shows the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-6 Register Settings for CCO High Diagnosis (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock setting
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	10b	Calibration setting
	CTSUTSOC	1	
CTSUSSC	CTSUSSDIV[3:0]	0111b	Spread-spectrum clock division setting
CTSUDPRS	CTSUSOFF	0	High-frequency noise reduction setting
CTSUDCLKC	CTSUSSMOD[1:0]	00b	
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSO0	CTSUSO[9:0]	0x000	Offset current setting
	CTSUSNUM[5:0]	000111b	Measurement count setting: 8

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to “0”.

2.3.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2).

2.3.3 Determination

Check whether the measured value falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ CCO_HIGH. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

2.4 CCO Low Diagnosis

Figure 2-5 shows a circuit diagram for CCO low diagnosis. In this diagnosis, a current corresponding to the lower limit of CCO input is input to the CCO similarly to section 2.3, and the CCO is verified based on whether the measured value falls within the specified range.

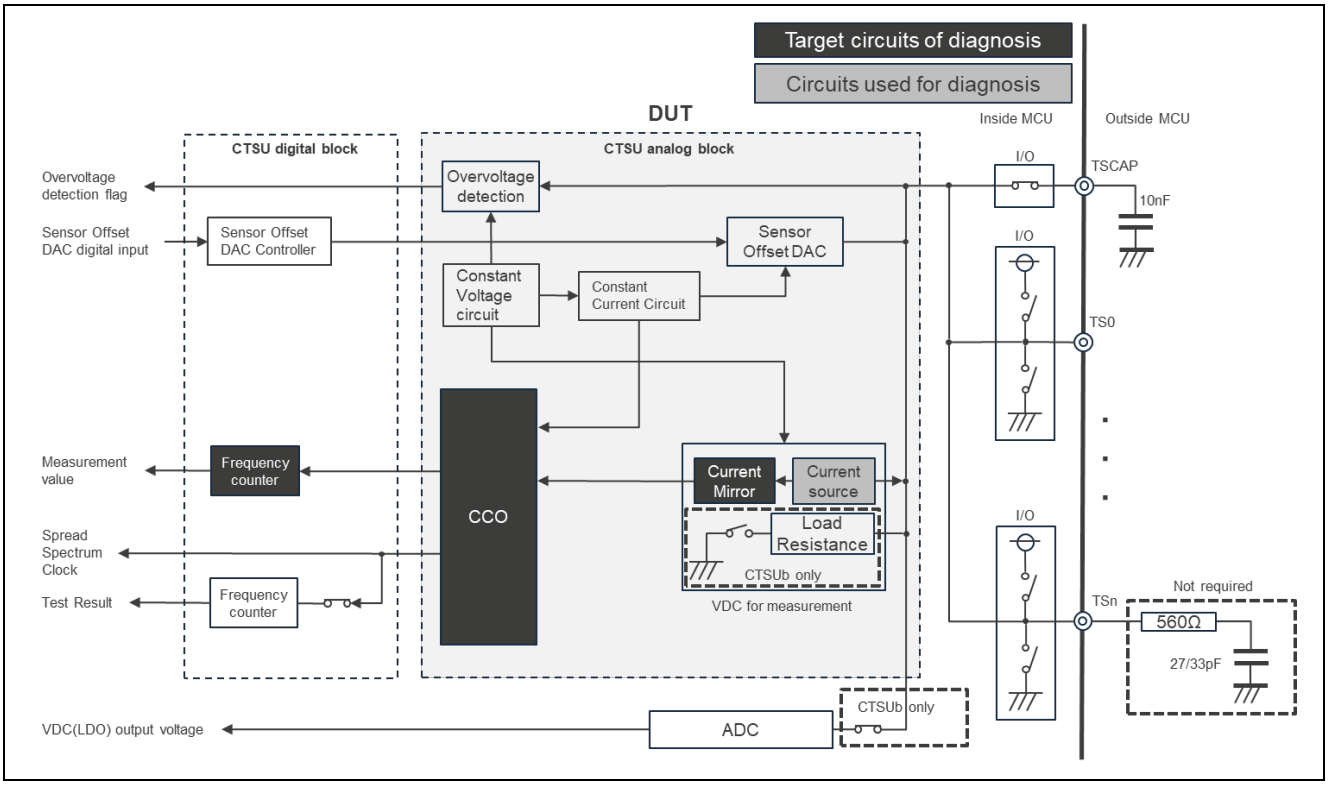

Figure 2-5 Circuit Diagram for CCO Low Diagnosis

2.4.1 Measurement

A specified current is input to the CCO to obtain the measured value.

Table 2-7 shows the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-7 Register Settings for CCO Low Diagnosis (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock setting
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	10b	Calibration setting
	CTSUTSOC	1	
CTSUSSC	CTSUSSDIV[3:0]	0111b	Spread-spectrum clock division setting
CTSUDPRS	CTSUSOFF	0	High-frequency noise reduction setting
CTSUDCLKC	CTSUSSMOD[1:0]	00b	
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSO0	CTSUSO[9:0]	0x000	Offset current setting
	CTSUSNUM[5:0]	000111b	Measurement count setting: 8

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to “0”.

2.4.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2).

2.4.3 Determination

Check whether the measured value falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ OSCILLATOR_LOW. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

2.5 SSCG Diagnosis

Figure 2-6 shows a circuit diagram for SSCG (spread spectrum clock generator) diagnosis. When outputting sensor drive pulses for current measurement, CTSU1 uses a SSCG to generate pulses with randomized frequency modulation, thereby reducing the impact of noise.

In this diagnosis, a measured value is obtained through the standard measurement using a SSCG. The diagnosis verifies the SSCG based on whether the measured value falls within the specified range .

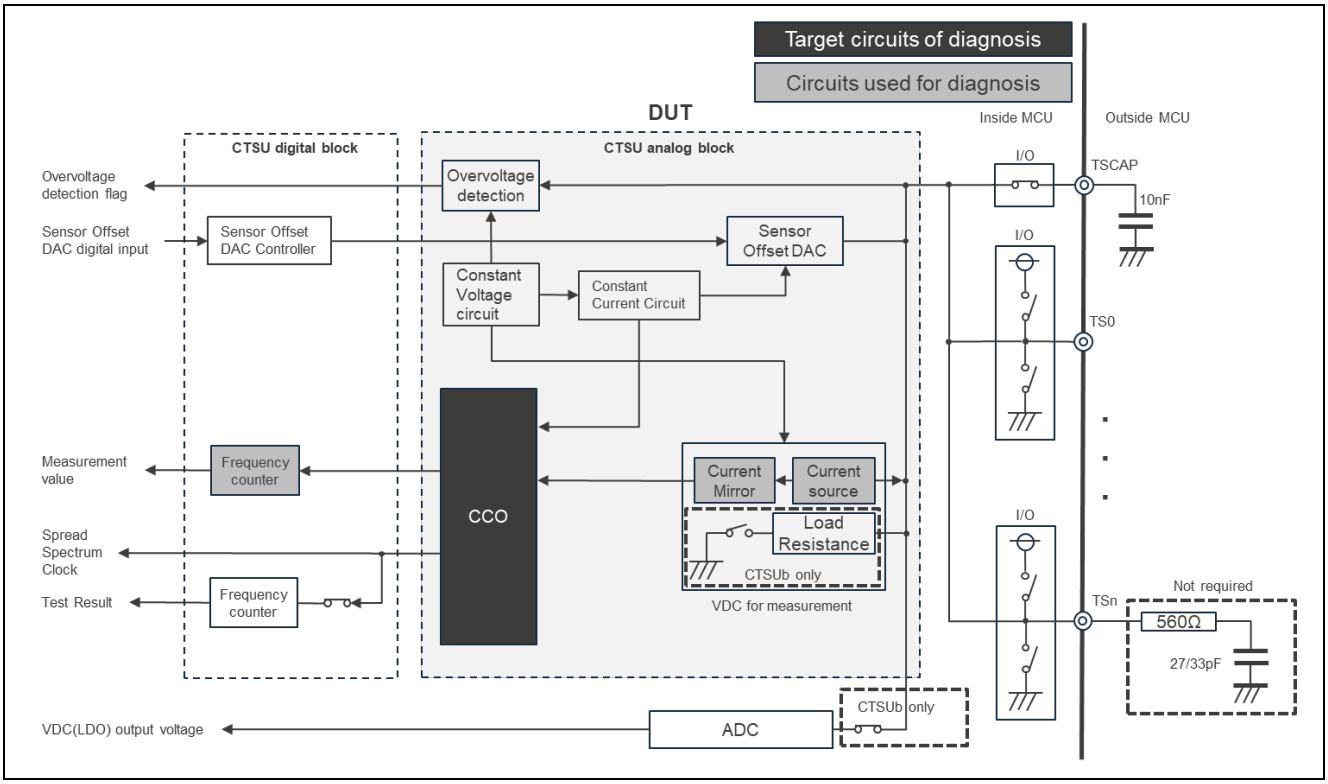

Figure 2-6 Circuit Diagram for SSCG Diagnosis

2.5.1 Measurement

Measurement is performed with the SSCG enabled to obtain the measured value.

Table 2-8 shows the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-8 Register Settings for SSCG Diagnosis (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock setting
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	00b	Calibration setting
	CTSUTSOC	1	
	CTSUCLKSEL1	1	
CTSUDPRS	CTSUSOFF	0	High-frequency noise reduction setting
CTSUDCLKC	CTSUSSMOD[1:0]	00b	
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSO0	CTSUSO[9:0]	0x000	Offset current setting
	CTSUSNUM[5:0]	000111b	Measurement count setting: 8

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to “0”.

2.5.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2).

2.5.3 Determination

Check whether the measured value falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ SSCG . If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

2.6 Sensor Offset Diagnosis (with TS Pin)

Figure 2-7 shows a circuit diagram for sensor offset diagnosis. The CTSU1 sensor offset function is a function that supplies an offset current adjusted by the sensor offset DAC to compensate for the charge corresponding to the parasitic capacitance of the electrode. For details on the sensor offset function, refer to section “2. Capacitance Detection” in Capacitive Sensor Microcontrollers CTSU Capacitive Touch Introduction Guide.

In this diagnosis, the sensor offset value is decreased stepwise from the value determined by offset tuning down to -0x100. The resulting changes in the sensor offset current are monitored using measurement values, and it is verified that the measurement value falls within the specified range at each step. Therefore, the TS pin must be connected to ground through a 560Ω resistor and a capacitor with sufficient capacitance to ensure that the sensor offset value does not become negative even when decreased to -0x100. Recommended external capacitor values for each MCU are listed in Table 2-9. Connect an external capacitor such that the total capacitance, including the board parasitic capacitance, becomes 27 pF or 33 pF.

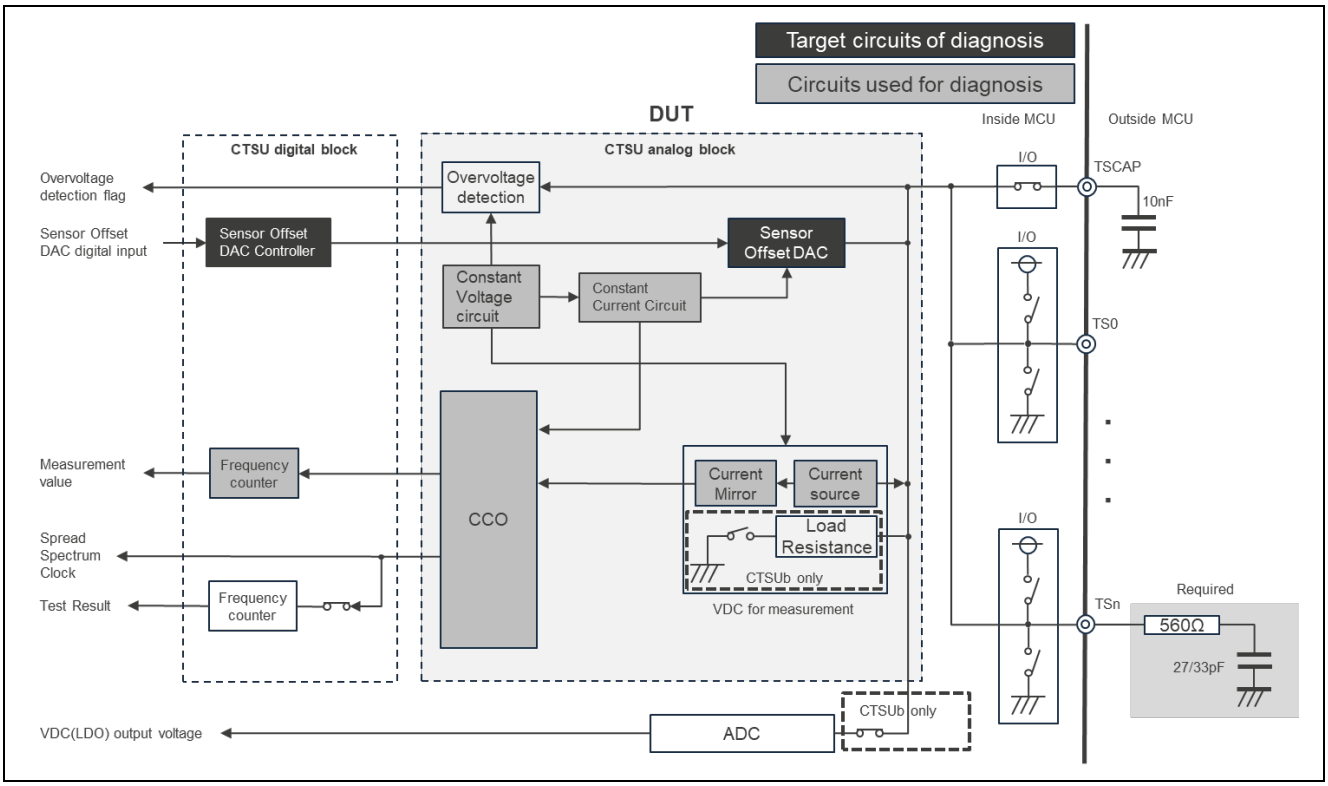

Figure 2-7 Circuit Diagram for Sensor Offset Diagnosis (with TS Pin)

Table 2-9 Recommended Capacitance of TS Pin Used for Diagnostis

Microcontroller	Recommended capacitance
RA2A1, RA4M1, RA4W1, RX130, RX230, RX231, RX23W	27 pF
RA4M2, RA4M3, RA6M1, RA6M2, RA6M3, RA6M4, RA6M5, RX671	33 pF

2.6.1 Measurement

Offset tuning is performed with the TS pin connected to an arbitrary electrode, then the sensor offset value is stepwise decreased in each test to obtain the measured values.

Table 2-10 and Table 2-11 show the register setting values for used for the diagnosis. In addition, enable the TS pin used for this diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-10 Register Settings for Sensor Offset Diagnosis (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock setting
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	00b	Calibration setting
	CTSUTSOC	1	
CTSUSSC	CTSUSSDIV[3:0]	0010b	Spread-spectrum clock division setting
CTSUDPRS	CTSUSOFF	0	High-frequency noise reduction setting
CTSUDCLKC	CTSUSSMOD[1:0]	00b	
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSO0	CTSUSNUM[5:0]	000111b	Measurement count setting: 8
CTSUSO1	CTSUSDPA[4:0]	00111b	Base clock setting: 1/16 of the CTSU operating clock

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to "0".

Table 2-11 Register Settings during Sensor Offset Diagnostic Operation

Test	Register	Bit	Value
1	CTSUSO0	CTSUSO[9:0]	(Note)
2	CTSUSO0	CTSUSO[9:0]	(CTSUSO value in Test 1) - 0x010
3	CTSUSO0	CTSUSO[9:0]	(CTSUSO value in Test 1) - 0x020
4	CTSUSO0	CTSUSO[9:0]	(CTSUSO value in Test 1) - 0x040
5	CTSUSO0	CTSUSO[9:0]	(CTSUSO value in Test 1) - 0x080
6	CTSUSO0	CTSUSO[9:0]	(CTSUSO value in Test 1) - 0x100

Note : Use the sensor offset value obtained after offset tuning.

2.6.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2).

2.6.3 Determination

Check whether the measured value obtained in each test falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ DAC. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

2.7 Sensor Offset Diagnosis (without TS Pin)

Figure 2-8 shows a circuit diagram for sensor offset diagnosis without TS pin. In CTSUb, the sensor offset function can be evaluated using only the MCU internal circuitry, without using external elements connected to TS pins, by means of a load resistance circuit and ADC measurement.

In this diagnosis, the current supplied by the sensor offset DAC is adjusted, and ADC measurement is performed. The diagnosis verifies the sensor offset function based on whether the measured value falls within the specified range.

Note: This diagnosis is supported only on CTSUb.

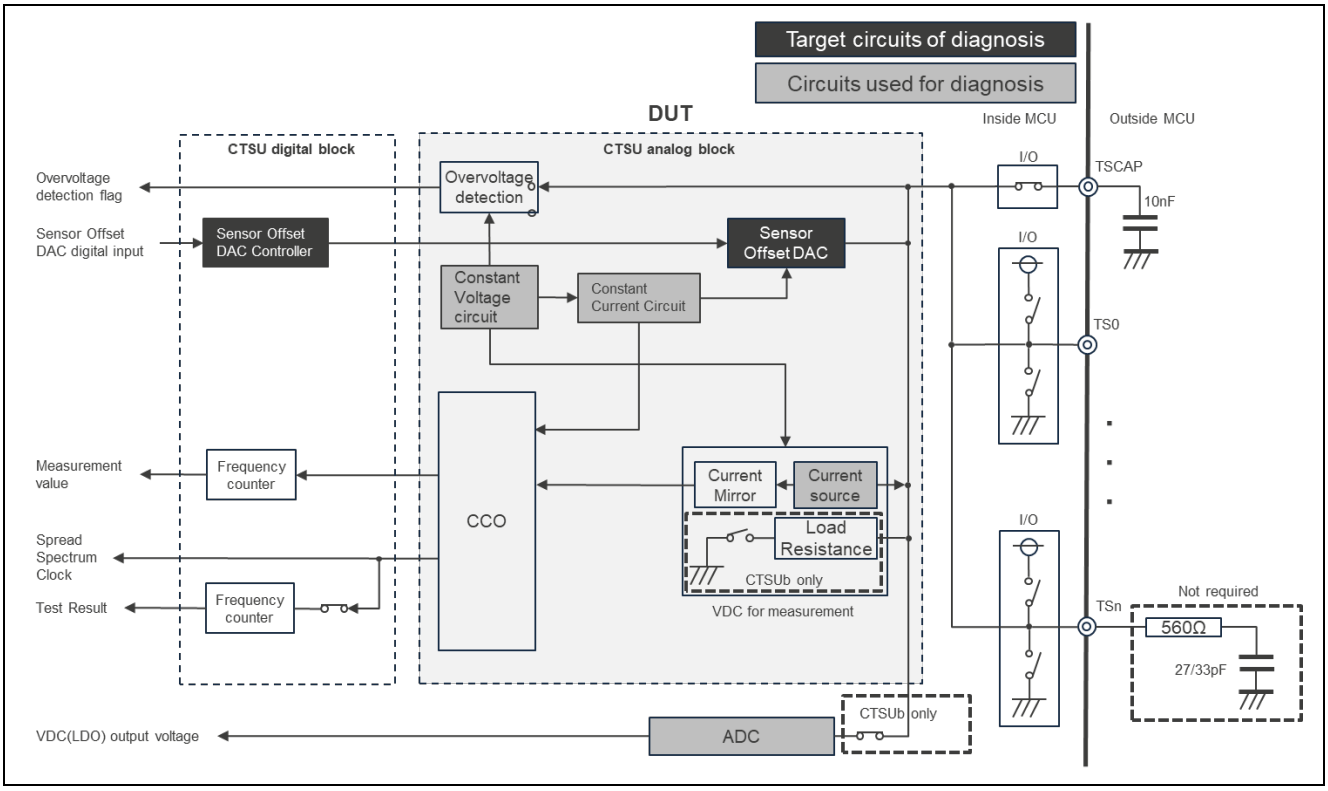

Figure 2-8 Circuit Diagram for Sensor Offset Diagnosis (without TS Pin)

2.7.1 Measurement

The load resistance and the sensor offset value are configured, and measurements are obtained by ADC measurement (see Table 2-13).

Table 2-12 and Table 2-13 show the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 2-12 Register Settings for Sensor Offset Diagnosis (without TS Pin) (Common)

Register	Bit	Value	Purpose
CTSUCR1 Note	CTSUMD[1:0]	00b	Self-capacitance single scan setting
	CTSUCLK[1:0]	00b	CTSU operating clock
CTSUERRS	-	0x0000	Initialization of calibration register settings
	CTSUSPMD[1:0]	00b	Calibration setting
	CTSUTSOC	1	
CTSUSSC	CTSUSSDIV[3:0]	0011b	Spread-spectrum clock division setting
CTSUDPRS	CTSUSOFF	0	High-frequency noise reduction setting
CTSUDCLKC	CTSUSSMOD[1:0]	00b	
	CTSUSSCNT[1:0]	11b	
CTSUSST	CTSUSST[7:0]	0x10	Sensor stabilization wait-time setting
CTSUSO0	CTSUSNUM[4:0]	00111b	Measurement count setting: 8

Note: Configure the CTSUCR1 register while CTSUCR0.CTSUSTRT is set to “0”.

Table 2-13 Register Settings during Sensor Offset Diagnostic Operation (without TS Pin)

TEST	Register	Bit	Value
1	CTSUSO0	CTSUSO[9:0]	0x200
	CTSUERRS	CTSUR01EN	1
		CTSUR02EN	0
		CTSUR03EN	0
2	CTSUSO0	CTSUSO[9:0]	0x100
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	1
		CTSUR03EN	0
3	CTSUSO0	CTSUSO[9:0]	0x080
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	0
		CTSUR03EN	1
4	CTSUSO0	CTSUSO[9:0]	0x070
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	0
		CTSUR03EN	1
5	CTSUSO0	CTSUSO[9:0]	0x060
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	0
		CTSUR03EN	1
6	CTSUSO0	CTSUSO[9:0]	0x050
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	0
		CTSUR03EN	1
7	CTSUSO0	CTSUSO[9:0]	0x030
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	0
		CTSUR03EN	1
8	CTSUSO0	CTSUSO[9:0]	0x088
	CTSUERRS	CTSUR01EN	0
		CTSUR02EN	0
		CTSUR03EN	1

2.7.2 Condition

Set the CTSU power supply operation to NM mode (see Table 2-2).

2.7.3 Determination

Check whether the measured value obtained in each test falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ DAC. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

2.8 Diagnosis API

The determination for each diagnostic item is performed sequentially. If an abnormality is detected, the diagnostic process is terminated at that time, and R_CTSU_Diagnosis returns the corresponding error value. If all diagnostic items are normal, R_CTSU_Diagnosis returns FSP_SUCCESS. Even if an abnormality is detected in diagnosis, diagnosis can be executed again without user operation.

2.9 Relation to Other Functions

If R_CTSU_Stop is called, the diagnostic test is suspended, and the current diagnostic state is retained. When measurement is restarted, the diagnostic test resumes from the point at which it was suspended.

If R_CTSU_Close is called, the diagnostic test is terminated, and the diagnostic state is initialized.

3. CTSU2 Diagnostic Function

This chapter describes the specifications of the diagnostic function implemented in CTSU2. Nine types of diagnostic items are provided for the target internal circuits, and each item has different execution timing and operating conditions. This chapter is divided into sections for each diagnostic item and describes the measurement operation, the execution condition, and the determination method for each. For the list of diagnostic items and their execution timing, refer to Table 3-1. Note that the diagnostic process described in this chapter covers the measurement start, measurement operation, and acquisition of measurement value.

Figure 3-1 shows a circuit diagram for the CTSU2 diagnostic function.

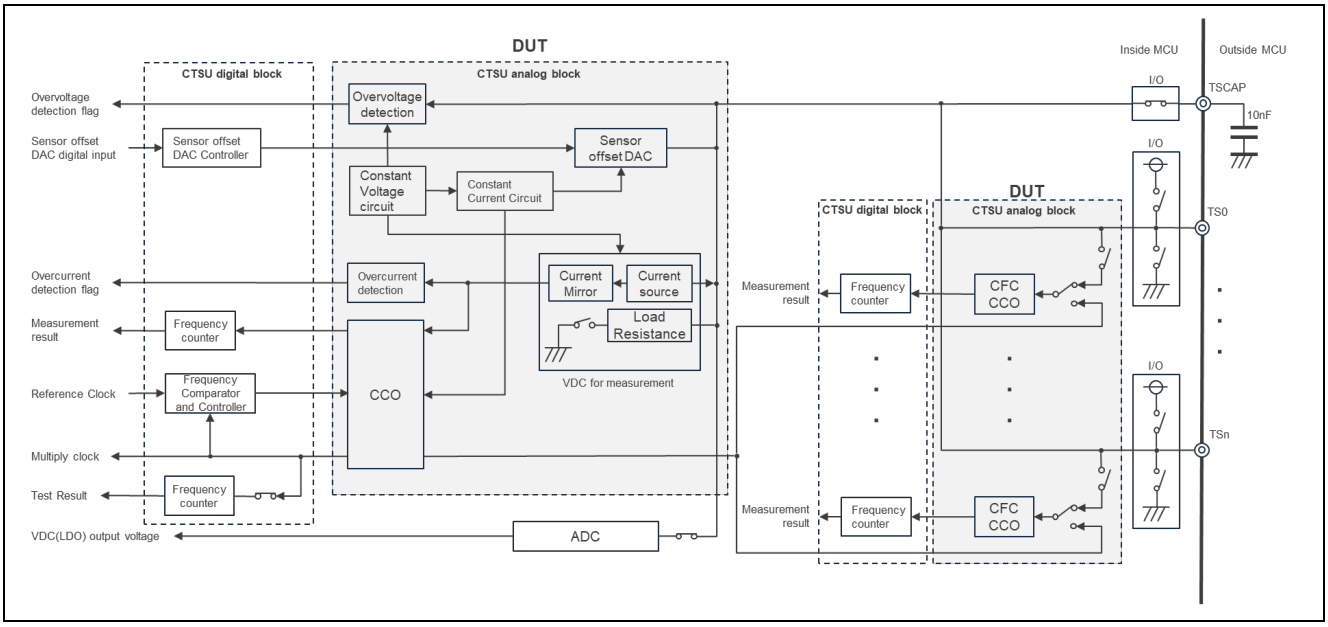

Figure 3-1 Circuit Diagram for CTSU2 Diagnostic Function

Table 3-1 Diagnostic Items and Execution Timing

Order	Diagnostic Name	One-time or Repeat Note
1	Output voltage diagnosis	Repeat
2	Overvoltage detection diagnosis	One-time
3	Overcurrent detection diagnosis	One-time
4	Load resistance diagnosis	Repeat
5	Sensor offset diagnosis	One-time
6	CCO frequency diagnosis	Repeat
7	SUCLK frequency diagnosis	Repeat
8	SUCLK clock recovery diagnosis	Repeat
9	CFC oscillator diagnosis (CFC operation only)	Repeat

Note : “One-time” indicates execution once after reset. “Repeat” indicates periodic execution.

This function is enabled when CTSU_CFG_DIAG_SUPPORT_ENABLE is set to “1” and the touch interface configuration variable md of the instance is set to CTSU_MODE_DIAGNOSIS_SCAN.

To minimize the impact of diagnostic processing on normal touch measurement operation, use this function according to the steps described below.

1. Initialization of the normal measurement configuration
2. Initialization of the diagnostic configuration
3. Execution of diagnostics at initialization
   - Measurement for diagnosis and acquisition of the measurement value, followed by diagnosis
   - After the measurement data acquisition returns normal completion, the diagnostic API is called to obtain the diagnostic results
4. Execution of normal measurement and periodic diagnostics

The diagnostic determination is executed during measurement data acquisition. If an abnormal result is detected in the determination, the measurement data acquisition returns normal completion at that time, and the diagnostic API is called. Even if an abnormality is detected in diagnosis, diagnosis can be executed again without user operation.

In this chapter, when evaluating a CTSU2 diagnostic item under multiple conditions, the term “Test” refers to an individual evaluation unit corresponding to each condition (e.g., Test 1, Test 2)

Table 3-2 through Table 3-4 show common register settings for the diagnostic function described in this chapter.

The diagnosis described in this chapter is performed with single-frequency measurement to reduce processing time. Accordingly, set CTSUMCH.MCA0 to 1 and set MCA1 through MCA3 to “0”.

The hardware CCO correction (auto-correction) function is disabled during the diagnosis.

Table 3-2 CTSU2 Common Register Settings for Diagnostic Function (RA Family)

Register	Bit	Value	Setting
CTSUMCH CTSUMCHH CTSUMFAF	MCA0	1	Single-frequency measurement
	MCA1	0	
	MCA2	0	
	MCA3	0	
CTSUOPT CTSUOPTL CTSUAC	CCOCFEN	0	Auto-correction function OFF
CTSUCRA CTSUCRAH CTSUCRA2	SDPSEL	1	High-resolution pulse mode

Table 3-3 CTSU2 Common Register Settings for Diagnostic Function (RL78 Family)

Register	Bit	Value	Setting
CTSUMCHH	MCA0	1	Single-frequency measurement
	MCA1	0	
	MCA2	0	
	MCA3	0	
CTSUOPTL Note	CCOCFEN	0	Auto-correction function OFF
CTSUCRAH	SDPSEL	1	High-resolution pulse mode

Note: Register and bit field specifications vary depending on the product used. For details on how to configure the registers, refer to the User’s Manual (Hardware) for the MCU in use.

Table 3-4 CTSU2 Common Register Settings for Diagnostic Function (RX Family)

Register	Bit	Value	Setting
CTSUMCH	MCA0	1	Single-frequency measurement
	MCA1	0	
	MCA2	0	
	MCA3	0	
CTSUOPT	CCOCFEN	0	Auto-correction function OFF
CTSUCRA	SDPSEL	1	High-resolution pulse mode

Table 3-5 shows the settings for CTSU2 power supply operation mode. In this application note, the CTSU2 operating voltage states selected by the ATUNE0 bit are referred to as Normal (NM) mode and Low Voltage (LV) mode.

Table 3-5 CTSU2 Power Operating Mode Settings

CTSU Power Supply Operating Mode	CTSUCRA.ATUNE0 (RA and RX Families) CTSUCRAL.ATUNE0 (RL78 Family)	MCU Power Supply Voltage (V)
NM mode	0	2.4 to 5.5
LV mode	1	1.8 to 5.5

Note: Register and bit field specifications vary depending on the product used. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

In principle, the register settings described in this chapter must not be changed.

This diagnosis function uses the ADC module. Therefore, if the ADC is used in the user system, conflicts with ADC processing may occur during the diagnostic operation. Before executing the diagnostic function, stop the ADC on the user side or control it so that no conflict occurs with the diagnosis function.

3.1 Output Voltage Diagnosis

Figure 3-2 shows a circuit diagram for output voltage diagnosis. The TSCAP pin is connected to a current source used for CTSU measurement, and the TSCAP voltage is regulated to a constant level. The diagnosis evaluates this TSCAP voltage while the current from this source is flowing through the load resistance. To evaluate the TSCAP voltage independently of fluctuation in the MCU power supply voltage, the internal power supply voltage is first measured by the ADC using the MCU power supply voltage as the reference, and the MCU power supply voltage is calculated from the known ratio to the internal reference voltage. Next, TSCAP voltage is measured by the ADC using the MCU power supply voltage as the reference. A current source failure is diagnosed based on whether the measured value falls within the specified range.

This function is also applicable to systems in which the MCU power supply voltage varies, such as battery-powered systems.

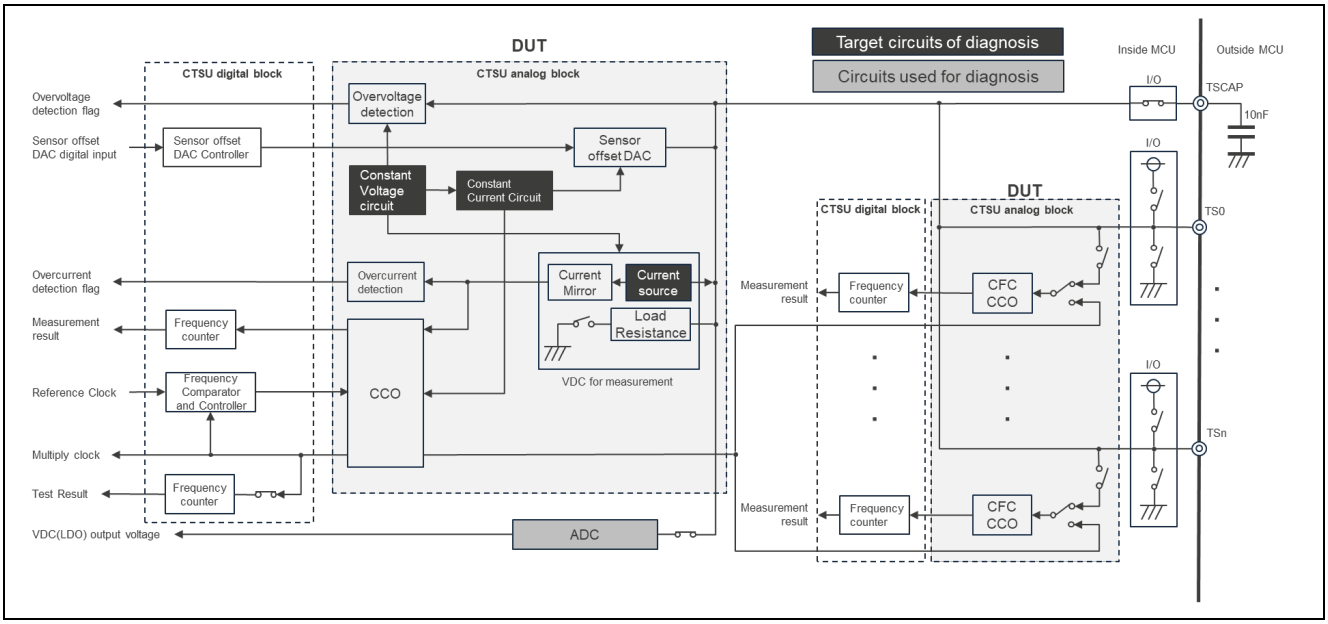

Figure 3-2 Circuit Diagram for Output Voltage Diagnosis

3.1.1 Measurement

In this diagnosis, the ADC is used to measure the TSCAP voltage independently of the MCU power supply voltage.

Since the ADC conversion result depends on the reference voltage, the MCU power supply voltage must be known in advance when used as the reference for TSCAP voltage measurement. Therefore, the internal reference voltage is measured by the ADC using the MCU power supply voltage as the reference, and the MCU power supply voltage is calculated from the known ratio to the internal reference voltage. The TSCAP voltage is then calculated using the MCU power supply voltage as the reference. Each voltage is obtained by performing ADC measurements four times, and the average value is used.

Table 3-6 to Table 3-8 show the register settings for output voltage diagnosis.

Table 3-6 Register Settings for Output Voltage Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCALIB CTSUBGR0	TSOC	1	Calibration mode setting
	DRV	1	Calibration mode setting
CTSUSO CTSUSO0	SO[9:0]	00 00000000b	No offset current
CTSUSO	SNUM[7:0]	0x07	Measurement time 128us
CTSUSO CTSUSO1	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK

Table 3-7 Register Settings for Output Voltage Diagnosis for RL78 Family (Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode setting
	DRV	1	Calibration mode setting
CTSUDBGR1	-	0x0000	Initialization of calibration register
CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK

Table 3-8 Register Settings for Output Voltage Diagnosis for RX Family(Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode setting
	DRV	1	Calibration mode setting
CTSUSO	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK

Table 3-9 show the register settings during output voltage diagnostic operation. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-9 Register Settings during Output Voltage Diagnostic Operation

TEST	Register	Bit	Value	Setting
1	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	00b	Constant-current load mode
		ATUNE2	1	Current range: 20 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	0	
2	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	00b	Constant-current load mode
		ATUNE2	0	Current range: 40 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	1	
3	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	00b	Constant-current load mode
		ATUNE2	0	Current range: 80 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	0	
4	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	00b	Constant-current load mode
		ATUNE2	1	Current range: 160 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	1	
5	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	01b→11b	Resistive load mode
		ATUNE2	1	Current range: 20 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	0	
6	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	01b→11b	Resistive load mode
		ATUNE2	0	Current range: 40 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	1	
7	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	01b→11b	Resistive load mode
		ATUNE2	0	Current range: 80 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	0	
8	CTSUCRA、CTSUCRAH CTSUCR2	LOAD[1:0]	01b→11b	Resistive load mode
		ATUNE2	1	Current range: 160 uA
	CTSUCRA、CTSUCRAL CTSUCR1	ATUNE1	1	

3.1.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings (see Table 3-5).

3.1.3 Determination

Check whether the average of measured values falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.2 Overvoltage Detection Diagnosis

Figure 3-3 shows a circuit diagram for overvoltage detection diagnosis. A circuit for detecting overvoltage at the TSCAP pin is provided in the device. When the TSCAP voltage exceeds a specified level, an overvoltage condition is detected, the measurement operation is interrupted, and the internal circuitry is protected.

This diagnosis verifies the overvoltage detection circuit. Normal-voltage and overvoltage conditions are reproduced using the sensor offset DAC and a load resistance, and the ability of the circuit to correctly distinguish between these conditions is verified.

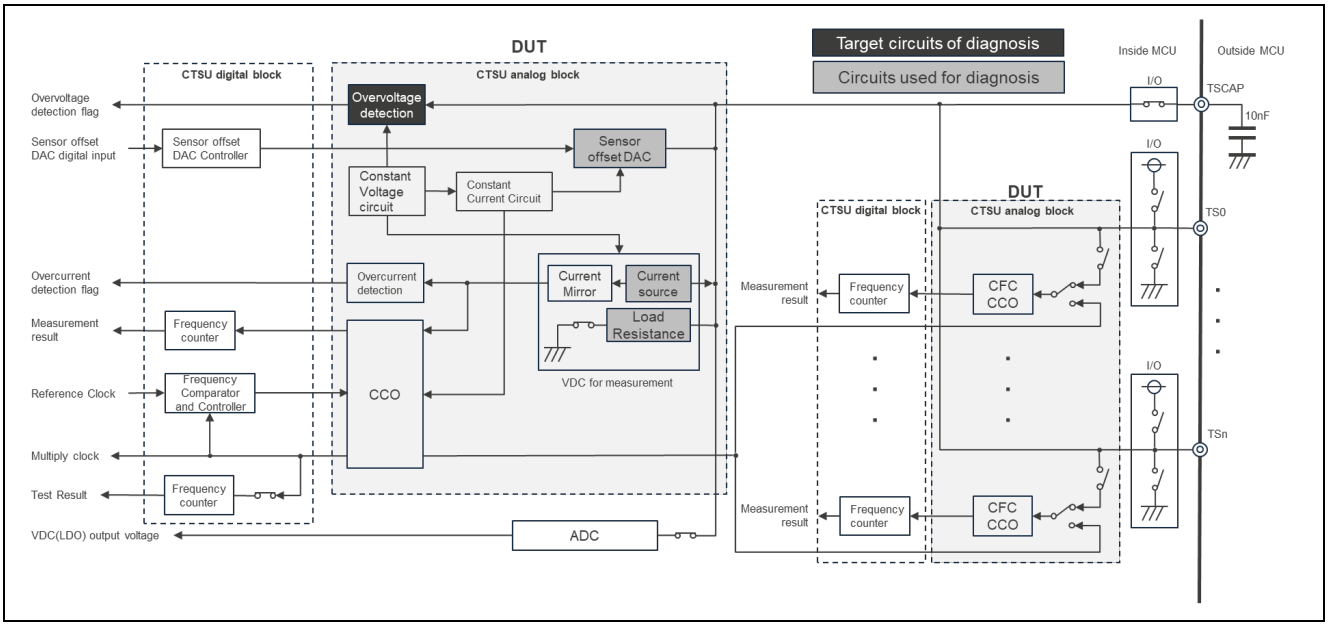

Figure 3-3 Circuit Diagram for Overvoltage Detection Diagnosis

3.2.1 Measurement

In Test 1, after setting the load resistance and the sensor offset to 0x000, the measurement value is obtained to verify that no overvoltage is detected under normal voltage conditions (ICOMP0 = 0).

In Test2, after setting the load resistance and the sensor offset to 0x200, the measurement value is obtained to verify that an overvoltage is detected under overvoltage conditions (ICOMP0 = 1). Then, after setting ICOMPRST to 1, it is verified that no overvoltage is detected (ICOMP0 = 0).

Normal voltage and overvoltage conditions are switched by CTSUSO register settings.

Table 3-10 to Table 3-12 show the register setting values used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-10 Register Settings for Overvoltage Detection Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCALIB CTSUBGR1	TSOC	1	Calibration mode
CTSUCRA CTSUCRAH CTSUCRA2	LOAD[1:0]	01b→11b	Resistive load mode
CTSUCRA CTSUCRAx (x: H, L, 2, 1)	ATUNE1	1	Current measurement range: 40uA mode
	ATUNE2	0	
CTSUSO	SNUM[7:0]	0x07	Measurement time 128us

Table 3-11 Register Settings for Overvoltage Detection Diagnosis for RL78 Family(Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUDBGR1	-	0x0000	Initialization of calibration register
CTSUCRAH	LOAD[1:0]	0x01→0x03	Resistive load mode
CTSUCRAL CTSUCRAH	ATUNE1 ATUNE2	1 0	Current measurement range: 40uA mode
CTSUSO0 CTSUSO1	SNUM[7:0]	0x07	Measurement time 128us

Table 3-12 Register Settings for Overvoltage Detection Diagnosis for RX Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUCRA	LOAD[1:0]	01b→11b	Resistive load mode
	ATUNE1	1	Current measurement range: 40uA mode
	ATUNE2	0	
CTSUSO	SNUM[7:0]	0x07	Measurement time 128us

3.2.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings (see Table 3-5).

3.2.3 Determination

At the measurement completion interrupt, the following processes are performed based on the overvoltage detection result under normal and over voltage conditions reproduced intentionally.

If an overvoltage is detected under normal voltage conditions (ICOMP0 = 1), R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_VOLTAGE. If no overvoltage is detected (ICOMP0 = 0), R_CTSU_Diagnosis returns FSP_SUCCESS.

If no overvoltage is detected under overvoltage conditions (ICOMP0 = 0), R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_VOLTAGE. If an overvoltage is detected (ICOMP0 = 1), R_CTSU_Diagnosis returns FSP_SUCCESS.

If an overvoltage is detected (ICOMP0=1) after detecting an overvoltage (ICOMP0=1) and setting ICOMPRST to 1, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_VOLTAGE. If no overvoltage is detected (ICOMP0 = 0), R_CTSU_Diagnosis returns FSP_SUCCESS.

3.3 Overcurrent Detection Diagnosis

Figure 3-4 shows a circuit diagram for overcurrent detection diagnosis. CTSU2 repeatedly charges and discharges the electrode capacitance using an internal current source for a fixed period, inputs the resulting charge current to a current-controlled oscillator (CCO). An overcurrent detection circuit is incorporated in the input current path to the CCO. When an instantaneous current exceeds a specified level, an overcurrent condition is detected, the measurement operation is suspended, and the internal circuitry is protected.

This diagnosis verifies the overcurrent detection circuit. Normal-current and overcurrent conditions are intentionally reproduced by changing the settings for the sensor offset, current measurement, and SDPA, the ability of the overcurrent detection circuit to correctly distinguish between these conditions is verified.

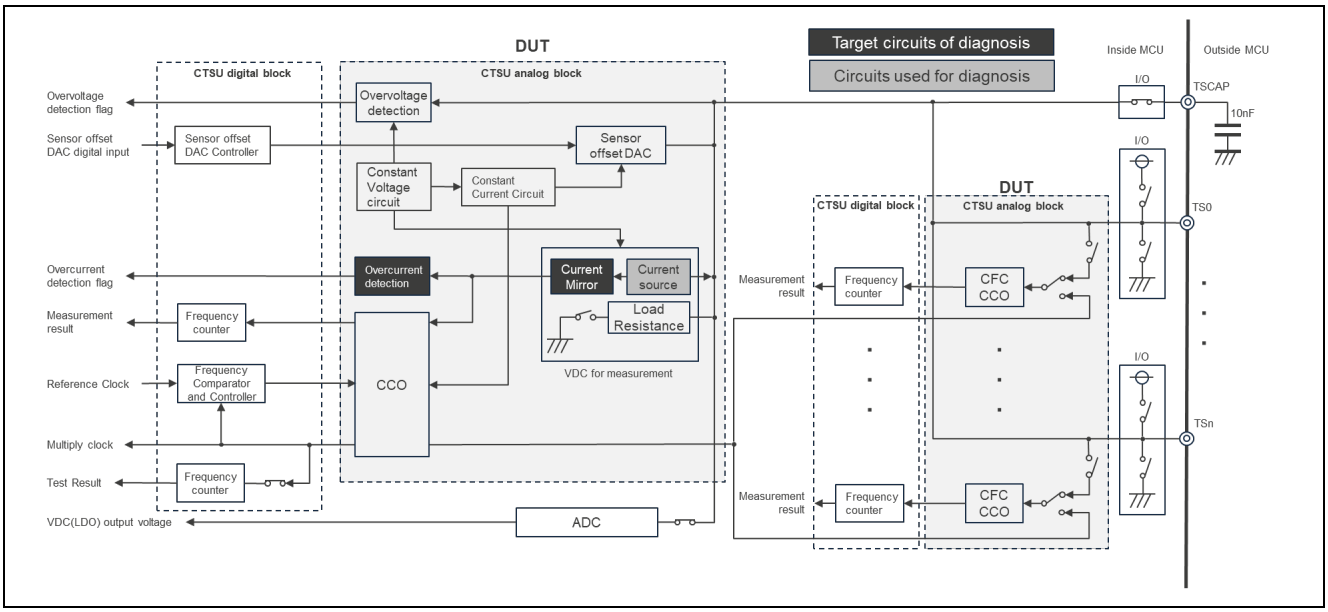

Figure 3-4 Circuit Diagram for Overcurrent Detection Diagnosis

3.3.1 Measurement

In Test 1 a measurement value is obtained under normal current conditions, and it is verified that no overcurrent is detected (ICOMP1 = 0) under normal current conditions.

In Test 2, a measurement value is obtained under overcurrent conditions, and it is verified that an overcurrent is detected (ICOMP1 = 1) under overcurrent conditions. Then, after setting ICOMPRST to 1, a measurement value is obtained, and it is verified that no overcurrent is detected (ICOMP1 = 0).

Table 3-16 shows register settings for normal and over current conditions

For the SDPA settings without using QE, refer to the following Application Notes on CTSU module.

RL78 Family CTSU module Software Integration System Rev.2.30

RX Family QE CTSU module Firmware Integration Technology

RA Flexible Software Package Documentation: CTSU(r_ctsu)

For the SDPA settings for the diagnosis, refer to “1.4.5 (d) Notes on configuration” when using RL family and RX family MCUs.

Table 3-13 to Table 3-16 show the register setting values used for the overcurrent detection diagnosis.

Table 3-13 Register Settings for Overcurrent Detection Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00	Initialization of calibration register
CTSUCRA CTSUCRAH CTSUCR2	LOAD[1:0]	01b	Load resistance OFF

Table 3-14 Register Settings for Overcurrent Detection Diagnosis for RL78 Family (Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
CTSUDBGR1	-	0x0000	Initialization of calibration register
CTSUCRAH	LOAD[1:0]	01b	Load resistance OFF

Table 3-15 Register Settings for Overcurrent Detection Diagnosis for RX Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCRA	LOAD[1:0]	01b	Load resistance OFF

Table 3-16 shows the CTSUSO register settings to switch between a normal current condition and an overcurrent condition. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-16 Register Settings for Normal and Over Current Conditions

Register	Bit	Value	Setting
Normal Current Condition			
CTSUSO CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128 us
	SDPA[7:0]	CTSU_CFG_SUMULTI0 value	Use the CTSU_CFG_SUMULTI0 value Note 1
CTSUCRA CTSUCRAL CTSUCR1	ATUNE1	1	Current measurement range: 160 uA
CTSUCRA CTSUCRAH CTSUCR2	ATUNE2	1	
Overcurrent Condition			
CTSUSO CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128 us
	SDPA[7:0]	(Note 2)	(Note 2)
CTSUCRA、 CTSUCRAL CTSUCR2	ATUNE1	0	Current measurement range: 20 uA
CTSUCRA、 CTSUCRAH CTSUCR1	ATUNE2	1	

Note 1: During normal current operation, the CTSU_CFG_SUMULTI0 value is stored in SDPA[7:0] to set the sensor drive pulse frequency to 0.5 MHz.

2: Set the SDPA assigned to a member of the diagnostic configuration output by QE.

3.3.2 Condition

The CTSU power supply operates in either Normal (NM) mode or Low Voltage (LV) mode depending on the user settings (see Table 3-5).

3.3.3 Determination

At the measurement completion interrupt, the following processes are performed based on the overcurrent detection result under normal and over current conditions reproduced intentionally.

If an overcurrent is detected under normal current conditions (ICOMP1 = 1), R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_CURRENT. If no overcurrent is detected (ICOMP1 = 0), R_CTSU_Diagnosis returns FSP_SUCCESS.

If no overcurrent is detected under overcurrent conditions (ICOMP1 = 0), R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_CURRENT. If an overcurrent is detected (ICOMP1 = 1), R_CTSU_Diagnosis returns FSP_SUCCESS.

If an overcurrent is detected after detecting an overcurrent condition (ICOMP1 = 1) and setting ICOMPRST to 1, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_OVER_CURRENT. If no overcurrent is detected (ICOMP1 = 0), R_CTSU_Diagnosis returns FSP_SUCCESS.

3.4 Load Resistance Diagnosis

Figure 3-5 shows a circuit diagram for load resistor diagnosis. CTSU2 incorporates a load resistance circuit that enables measurement operations internally, without requiring additional capacitance on external elements connected to the TS pin in CCO correction.

This diagnosis verifies the load resistance circuit. For each current measurement range, the current adjusted by the CTSU load resistance circuit is applied to the CCO, and the load resistance circuit is diagnosed for faults based on whether multiple measured values fall within the specified range.

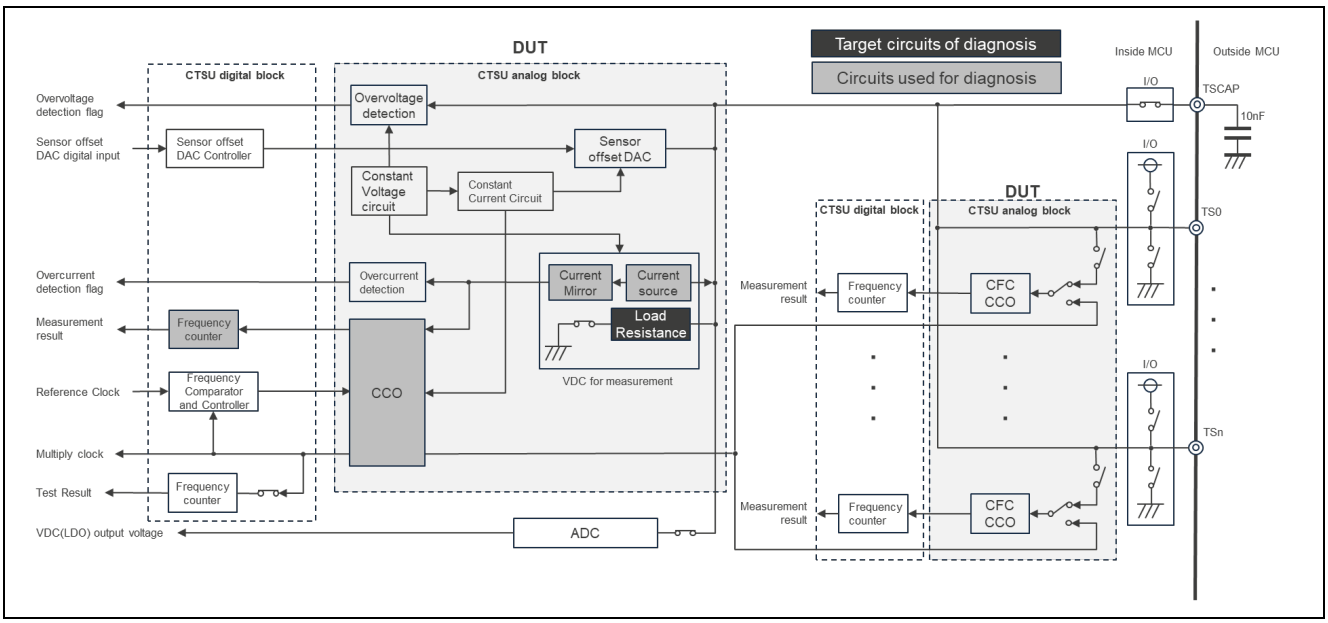

Figure 3-5 Circuit Diagram for Load Resistance Diagnosis

3.4.1 Measurement

When the TSCAP voltage is applied to the load resistance, the resulting current is input to the CCO. The CCO-corrected measurement value is then acquired four times, and the average of measurement values are calculated.

Table 3-17 to Table 3-19 show the register setting values for used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-17 Register Settings for Load Resistance Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCALIB CTSUBGR1	TSOC	1	Calibration mode
CTSUSO CTSUSO0	SO[9:0]	00 00000000b	No offset current
CTSUSO	SNUM[7:0	0x07	Measurement time 128us
CTSUSO CTSUSO1	SDPA[7:0	0x00	Sensor drive pulse frequency: 1/2 of SUCLK
CTSUCRA CTSUCRAH CTSUCRA2	LOAD[1:0]	01b→11b	Resistive load mode
CTSUCRA CTSUCRAx (x: H, L, 2, 1)	ATUNE1 ATUNE2	0 1	Current measurement range: 20uA
	ATUNE1 ATUNE2	1 0	Current measurement range: 40uA
	ATUNE1 ATUNE2	0 0	Current measurement range: 80uA
	ATUNE1 ATUNE2	1 1	Current measurement range: 160uA

Table 3-18 Register Settings for Load Resistance Diagnosis for RAL78 Family (Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUDBGR1	-	0x0000	Initialization of calibration register
CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK
CTSUCRAH	LOAD[1:0]	01b→11b	Resistive load mode
CTSUCRAL	ATUNE1	0	Current measurement range: 20uA
CTSUCRAH	ATUNE2	1	
CTSUCRAL	ATUNE1	1	Current measurement range: 40uA
CTSUCRAH	ATUNE2	0	
CTSUCRAL	ATUNE1	0	Current measurement range: 80uA
CTSUCRAH	ATUNE2	0	
CTSUCRAL	ATUNE1	0	Current measurement range: 160uA
CTSUCRAH	ATUNE2	1	

Table 3-19 Register Settings for Load Resistance Diagnosis for RX Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUOPT	CCOCFEN	0	Hardware correction OFF (only when hardware frequency correction is effective)
CTSUSO	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK
CTSUCRA	LOAD[1:0]	01b→11b	Resistive load mode
	ATUNE1 ATUNE2	0 1	Current measurement range: 20uA
	ATUNE1 ATUNE2	1 0	Current measurement range: 40uA
	ATUNE1 ATUNE2	0 0	Current measurement range: 80uA
	ATUNE1 ATUNE2	1 1	Current measurement range: 160uA

3.4.2 Condition

The CTSU power supply operates in either Normal (NM) mode or Low Voltage (LV) mode depending on the user settings (see Table 3-5).

3.4.3 Determination

Check whether the average measurement value falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ LOAD_RESISTANCE . If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.5 Sensor Offset Diagnosis

Figure 3-6 shows a circuit diagram for sensor offset diagnosis. The CTSU2 sensor offset function is a function that supplies a current corresponding to the parasitic capacitance of the electrode using the offset current adjusted by sensor offset DAC. As the offset current increases, the current flowing through the current mirror in the measurement VDC circuit decreases accordingly.

In this diagnosis, changes in the measurement value in response to the offset current are evaluated, and the sensor offset circuit is diagnosed for faults by verifying whether the offset current is correctly reflected in the current mirror.

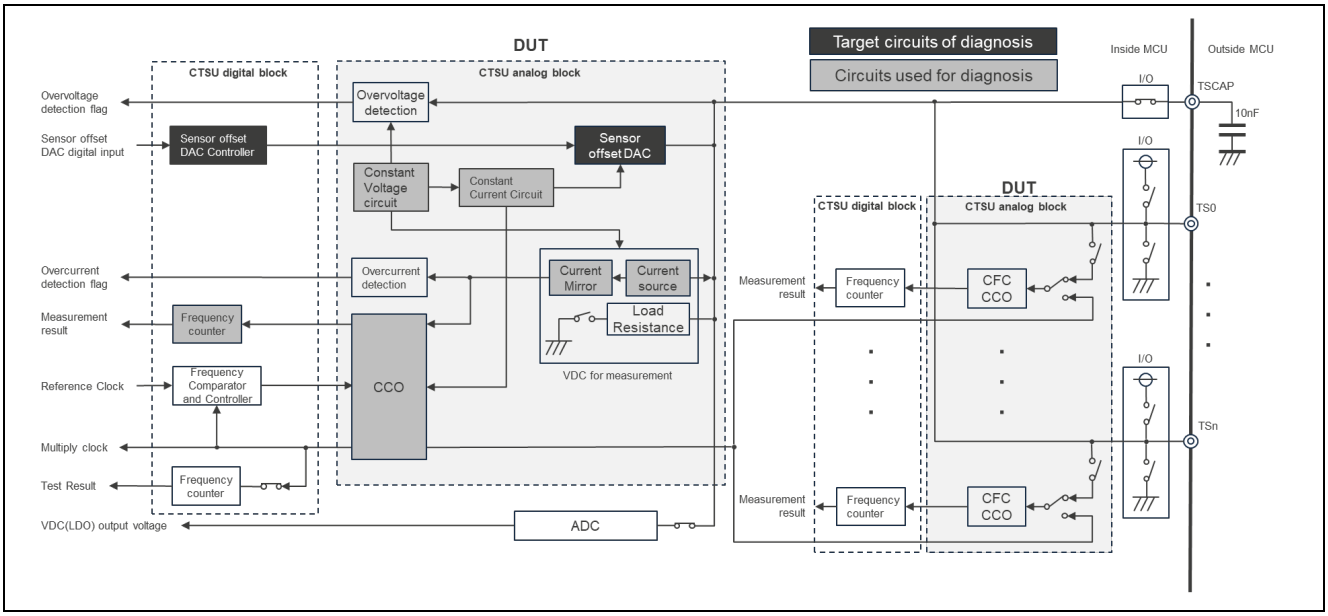

Figure 3-6 Circuit Diagram for Sensor Offset Diagnosis

3.5.1 Measurement

The difference between the measurement values for minimum changes in the offset current as below.

Under all combinations of settings where only a single bit of the offset current is enabled, measurements are performed four times for each condition, and the average of CCO-corrected measurement values is obtained. Then, the difference from the result of section 3.4 (no offset current) is calculated.

With the offset current set to the maximum, measurements are performed four times, and the average of CCO-corrected measurement values is obtained. Then, under all combinations of settings where only a single bit of the offset current is disabled, measurements are performed four times for each condition, and the average of CCO-corrected measurement values is obtained. The difference between them is calculated.

Table 3-20 to Table 3-22 show the register setting values for used for the diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-20 Register Settings for Sensor Offset Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCALIB CTSUBGR1	TSOC	1	Calibration mode
CTSUCALIB CTSUBGR1	DACMSEL	1	Current source fixed
	DACCARRY	1	ON/OFF control enabled for each current source
CTSUCRA CTSUCRAH CTSUCRA2	LOAD[1:0]	01b→11b	Resistive load mode
CTSUCRAx (x: H, L, 2, 1)	ATUNE1 ATUNE2	0 1	Current measurement range: 20uA

Table 3-21 Register Settings for Sensor Offset Diagnosis for RL78 Family (Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUDBGR1	-	0x0000	Initialization of calibration register
CTSUBGR1	DACMSEL	1	Current source fixed
	DACCARRY	1	ON/OFF control enabled for each current source
CTSUCRAH	LOAD[1:0]	01b→11b	Resistive load mode
CTSUCRAL	ATUNE1	0	Current measurement range: 20uA
CTSUCRAH	ATUNE2	1	

Table 3-22 Register Settings for Sensor Offset Diagnosis for RX Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode
	DACMSEL	1	Current source fixed
	DACCARRY	1	ON/OFF control enabled for each current source
CTSUCRA	LOAD[1:0]	01b→11b	Resistive load mode
	ATUNE1 ATUNE2	0 1	Current measurement range: 20uA

3.5.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings (see Table 3-5).

3.5.3 Determination

Check whether the difference acquired in each test falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ CURRENT_SOURCE. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.6 CCO Frequency Diagnosis

Figure 3-7 shows a circuit diagram for CCO frequency diagnosis. In CTSU2, measurement values are generated based on the current flowing through the electrode, and CCO is used to generate a frequency signal corresponding to the input current. This signal is counted by a counter, and the resulting count value is obtained as the CTSU measurement value.

This diagnosis evaluates the counter response to an arbitrary current from the test circuit and verifies whether the oscillation and measurement path from the CCO to the frequency counter operates as specified. Thus, abnormalities in the frequency characteristics of the CCO is detected.

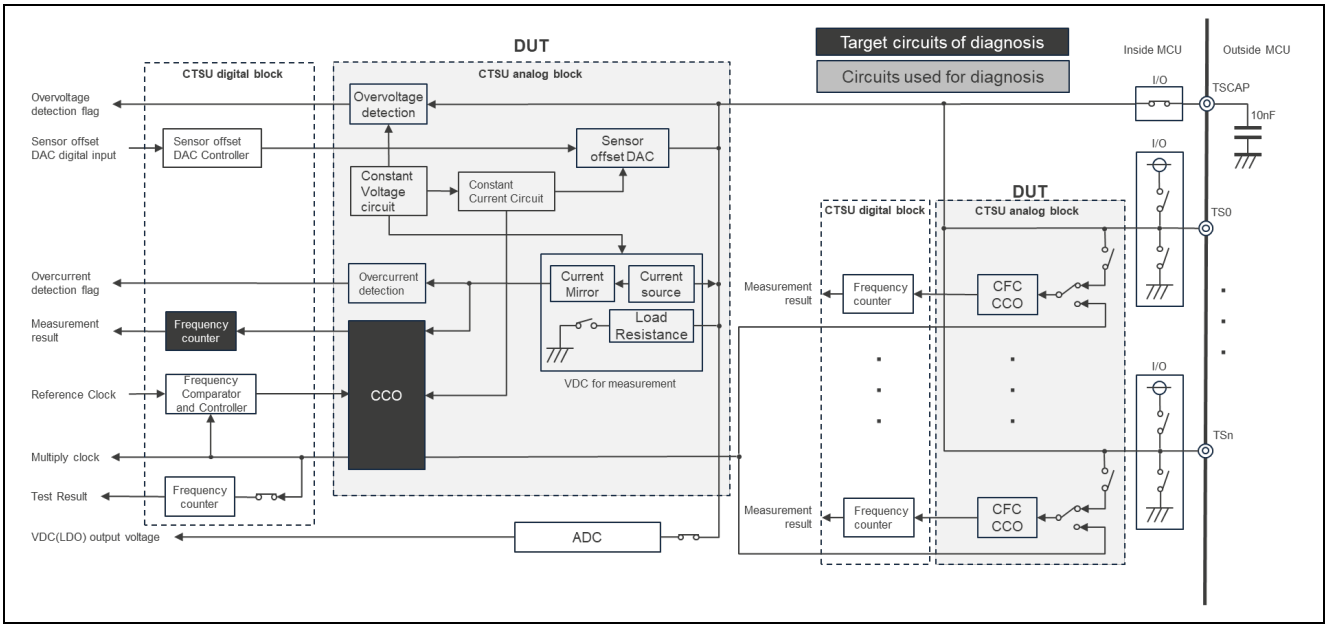

Figure 3-7 Circuit Diagram for CCO Frequency Diagnosis

3.6.1 Measurement

For each test, a different current level is applied to the frequency counter, with the current increasing stepwise from Test 1 onward. In each test, measurements are performed four times, and the average value is calculated. The difference between the average values obtained from consecutive tests is then calculated.

Table 3-23 through Table 3-25 show the register setting values used for CCO frequency diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-23 Register Settings for CCO Frequency Diagnosis (RA Family)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCALIB CTSUBGR0	TSOC	1	Calibration mode
CTSUCALIB CTSUBGR1	CCOCALIB	1	Oscillator calibration mode
CTSUCRA CTSUCRAH CTSUCR2	LOAD[1:0]	01b	Load resistance OFF
CTSUCRB	SSCNT[1:0]	00b	Clock adjustment for SUADJD0 disabled
CTSUSO CTSUSO0	SO[9:0]	00 00000000b	No offset current
CTSUSO	SNUM[7:0]	0x07	Measurement time 128us
CTSUSO CTSUSO1	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK

Table 3-24 Register Settings for CCO Frequency Diagnosis (RL78 Family)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUDBGR1	-	0x0000	Initialization of calibration register
	CCOCALIB	1	Oscillator calibration mode
CTSUCRAH	LOAD[1:0]	01b	Load resistance OFF
CTSUCRBH	SSCNT[1:0]	00b	Clock adjustment for SUADJD0 disabled
CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK

Table 3-25 Register Settings for CCO Frequency Diagnosis (RX Family)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUCALIB	CCOCALIB	1	Oscillator calibration mode
CTSUCRA	LOAD[1:0]	01b	Load resistance OFF
CTSUCRB	SSCNT[1:0]	00b	Clock adjustment for SUADJD0 disabled
CTSUSO	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency: 1/2 of SUCLK

3.6.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings(see Table 3-5).

3.6.3 Determination

Check whether the difference obtained in each test falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ SENSCLK_GAIN. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.7 SUCLK Frequency Diagnosis

Figure 3-8 shows a circuit diagram for SUCLK frequency diagnosis. CTSU2 is connected to SUCLK with an FLL (frequency-locked loop) the source clock for sensor drive pulses.

In this diagnosis, while the current supplied to the frequency counter for SUCLK is varied, it is verified whether the resulting oscillation frequency falls within the specified range. Thus, abnormalities in the frequency characteristics of the SUCLK circuit is detected.

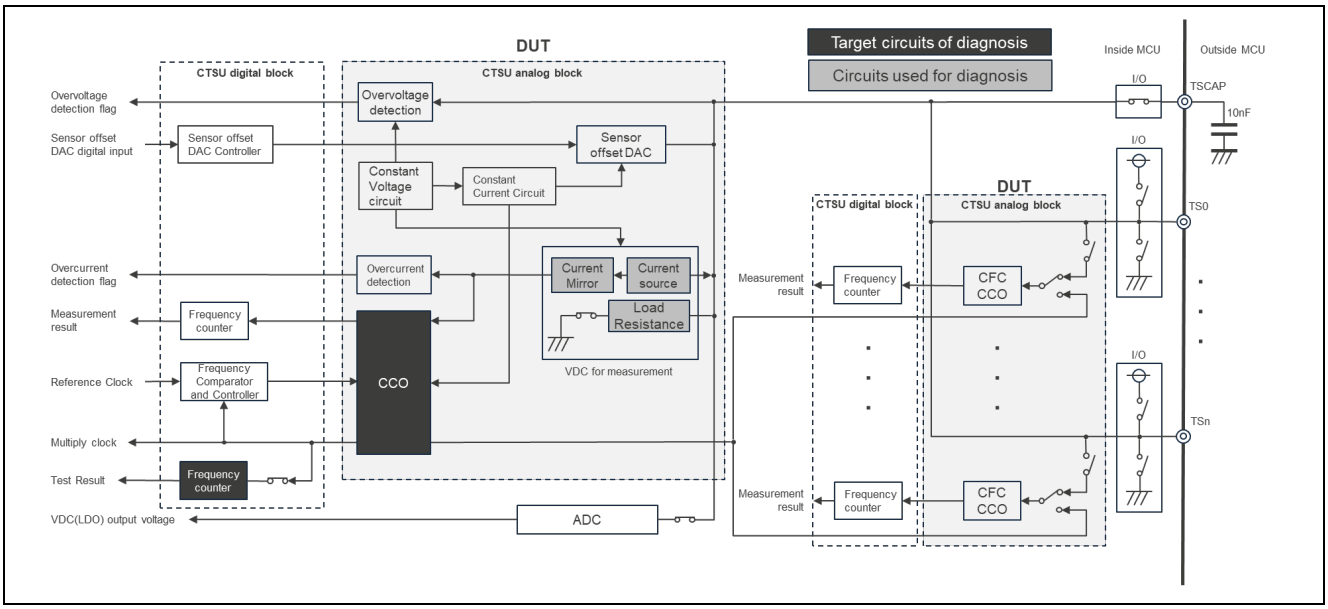

Figure 3-8 Circuit Diagram for SUCLK Frequency Diagnosis

3.7.1 Measurement

For each test, a different current level is applied to the frequency counter, with the current increasing stepwise from Test 1 onward. In each test, measurements are performed four times, and the average value is calculated. The difference between the average values obtained from consecutive tests is then calculated.

Table 3-26 and Table 3-27 show the register setting values for used for SUCLK frequency diagnosis. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-26 Register Settings for SUCLK Frequency Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
CTSUCALIB CTSUBGR1	SUMSEL	0 1	CCODAC current source switching CCODAC current source fixed
CTSUCRA CTSUCRAH CTSUCR2	LOAD[1:0]	01b	Load resistance OFF
CTSUCRB CTSUCRBH CTSUDCLKC	SSCNT[1:0]	00b	Clock adjustment for SUADJD0 disabled
CTSUSO CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

Table 3-27 SUCLK Register Settings for SUCLK Frequency Diagnosis for RL78 Family (Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUDBGR1	-	0x0000	Initialization of calibration register
	CCOCALIB	0	Oscillator calibration mode
	SUMSEL	0 1	CCODAC current source switching CCODAC current source fixed
CTSUCRAH	LOAD[1:0]	01b	Load resistance OFF
CTSUCRBH	SSCNT[1:0]	00b	Clock adjustment for SUADJD0 disabled
CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

Table 3-28 SUCLK Register Settings for SUCLK Frequency Diagnosis for RX Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode
	CCOCALIB	1	Oscillator calibration mode
CTSUCALIB	SUMSEL	0 1	CCODAC current source switching CCODAC current source fixed
CTSUCRA	LOAD[1:0]	01b	Load resistance OFF
CTSUCRB	SSCNT[1:0]	00b	Clock adjustment for SUADJD0 disabled
CTSUSO	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

3.7.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings (see Table 3-5).

3.7.3 Determination

Check whether the average counter value acquired in each test falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_ SUCLK_GAIN. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.8 SUCLK Clock Recovery Diagnosis

Figure 3-9 shows a circuit diagram for SUCLK recovery diagnosis. CTSU2 incorporates a clock recovery function that compensates for deviations between the configured frequency and the actual output frequency using FLL during SUCLK generation.

In this diagnosis, the measurement process is performed with SUCLK set to a specified frequency, and the SUCLK clock recovery function is diagnosed for faults based on whether the resulting SUCLK counter value falls within the specified range.

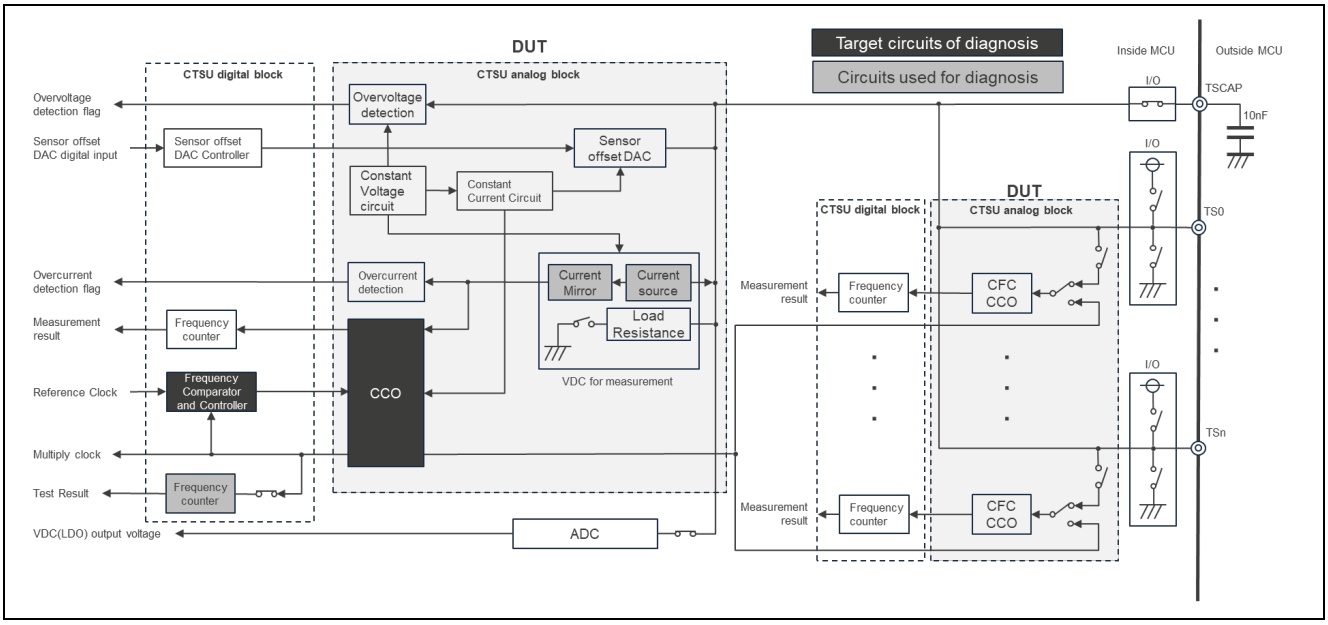

Figure 3-9 Circuit Diagram for SUCLK Clock Recovery Diagnosis

3.8.1 Measurement

The maximum output frequency of SUCLK varies depending on the MCU product.

The tests are performed four times at three or four different frequency settings depending on the SUCLK upper limit. The SUCLK counter values are measured in each test, and the average is obtained.

Table 3-29 through Table 3-31 shows the register setting values used for the diagnosis.

Table 3-29 Register Settings for SUCLK Clock Recovery Diagnosis for RA Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode
	CCOCALIB	1	SENSCLK Oscillator calibration mode
	CCOCLK	1	SUCLK selected for CCO modulation circuit clock
CTSUCRA	LOAD[1:0]	01b	Load resistance OFF
CTSUCRB CTSUCRBH CTSUDCLKC	SSCNT[1:0]	01b	SUCLK frequency adjustment
CTSUCRB CTSUCRBL CTSUSST	SST[7:0]	0x3F	Measurement stabilization wait-time setting
CTSUSO CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

Table 3-30 Register Settings for SUCLK Clock Recovery Diagnosis for RL78 Family (Common)

Register	Bit	Value	Setting
CTSUDBGR0	-	0x0000	Initialization of calibration register
	TSOC	1	Calibration mode
CTSUDBGR1	-	0x0000	Initialization of calibration register
	CCOCALIB	1	Oscillator calibration mode
	CCOCLK	1	SUCLK selected for CCO modulation circuit clock
CTSUCRAH	LOAD[1:0]	01b	Load resistance OFF
CTSUCRBH	SSCNT[1:0]	01b	SUCLK frequency adjustment
CTSUCRBL	SST[7:0]	0x3F	Measurement stabilization wait-time setting
CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

Table 3-31 Register Settings for SUCLK Clock Recovery Diagnosis for RX Family (Common)

Register	Bit	Value	Setting
CTSUCALIB	-	0x00000000	Initialization of calibration register
	TSOC	1	Calibration mode
	CCOCALIB	1	Oscillator calibration mode
	CCOCLK	1	SUCLK selected for CCO modulation circuit clock
CTSUCRA	LOAD[1:0]	01b	Load resistance OFF
CTSUCRB	SSCNT[1:0]	01b	SUCLK frequency adjustment
	SST[7:0]	0x3F	Measurement stabilization wait-time setting
CTSUSO	SO[9:0]	00 00000000b	No offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

In this diagnosis, the test frequency is set based on the SUCLK upper limit of the MCU. Since the MCU maximum frequency varies depending on the CTSU power supply operation mode, the test conditions are configured accordingly. Table 3-32 shows the settings for each test, and Table 3-33 and Table 3-34 show the combination for the tests based on the CTSU power supply operation mode. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-32 SUCLK Frequency Settings during SUCLK Clock Recovery Diagnostic Operation

Test	Register	Bit	Value	Setting
1	CTSUSUCLKA Note 1 CTSUSUCLK0	SUMULTI0	31	SUCLK: 16MHz
2	CTSUSUCLKA CTSUSUCLK0	SUMULTI0	47	SUCLK: 24MHz
3	CTSUSUCLKA CTSUSUCLK0	SUMULTI0	63/59	SUCLK: 32MHz/30MHz Note 2
4	CTSUSUCLKA CTSUSUCLK0	SUMULTI0	79/75	SUCLK: 40MHz/38MHz Note 3

Note 1: Due to CTSU IP constraints, writing to CTSUSUCLKx (x: A, 0) is prohibited while SDPSEL is set to 1. After setting SDPSEL to "0", set CTSUCLKA, and then set SDPSEL back to "1".
2: For MCU products with a maximum SUCLK of 30 MHz, the test is performed at 30 MHz instead.
3: For MCU products with a maximum SUCLK of 38 MHz, the test is performed at 38 MHz instead.

Table 3-33 Combination for SUCLK Clock Recovery Diagnostic Tests (CTSU Power Supply Operation Mode: NM)

MCU	Maximum Frequency (MHz)	Tests to be conducted
RA2L1, RA4L1, RA2E1, RX140,	40	Test 1, Test 2, Test 3, Test 4
RL78/F25, RL78/F22	38	Test 1, Test 2, Test 3, Test 4 Note 1
RX261, RX260	32	Test 1, Test 2, Test 3
RA0L1, RL78/G22, RL78/G23, RL78/L23	30	Test 1, Test 2, Test 3 Note 2

Note 1: Since a maximum SUCLK of the MCU is 38 MHz, Test 4 is conducted at 38 MHz frequency instead.
2: Since a maximum SUCLK of the MCU is 30 MHz, Test 3 is conducted at 30 MHz frequency instead.

Table 3-34 Combination for SUCLK Clock Recovery Diagnostic Tests (CTSU Power Supply Operation Mode: LV)

MCU	Maximum Frequency (MHz)	Tests to be conducted
RA2L1, RA4L1, RA2E1, RX140,	32	Test 1, Test 2, Test 3
RL78/F25, RL78/F22	N/A	-
RX261, RX260	32	Test 1, Test 2, Test 3
RA0L1, RL78/G22, RL78/G23, RL78/L23	30	Test 1, Test 2, Test 3 Note

Note : Since a maximum SUCLK of the MCU is 30 MHz, Test 3 is conducted at 30 MHz frequency instead.

3.8.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings(see Table 3-5).

3.8.3 Determination

Check whether the average counter value acquired in each test falls within the specified range. If it falls outside the range, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_CLOCK_RECOVERY. If it is within the range, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.9 CFC Oscillator Diagnosis

Figure 3-10 shows a circuit diagram for CFC oscillator diagnosis. CTSU2 provides a function that enables parallel simultaneous measurement using the CFC-CCO (current controlled oscillator) by the mutual-capacitance method.

This diagnosis verifies whether the CFC-CCO operates as specified by examining the response of the measurement values to variations in the current supplied to the CFC-CCO.

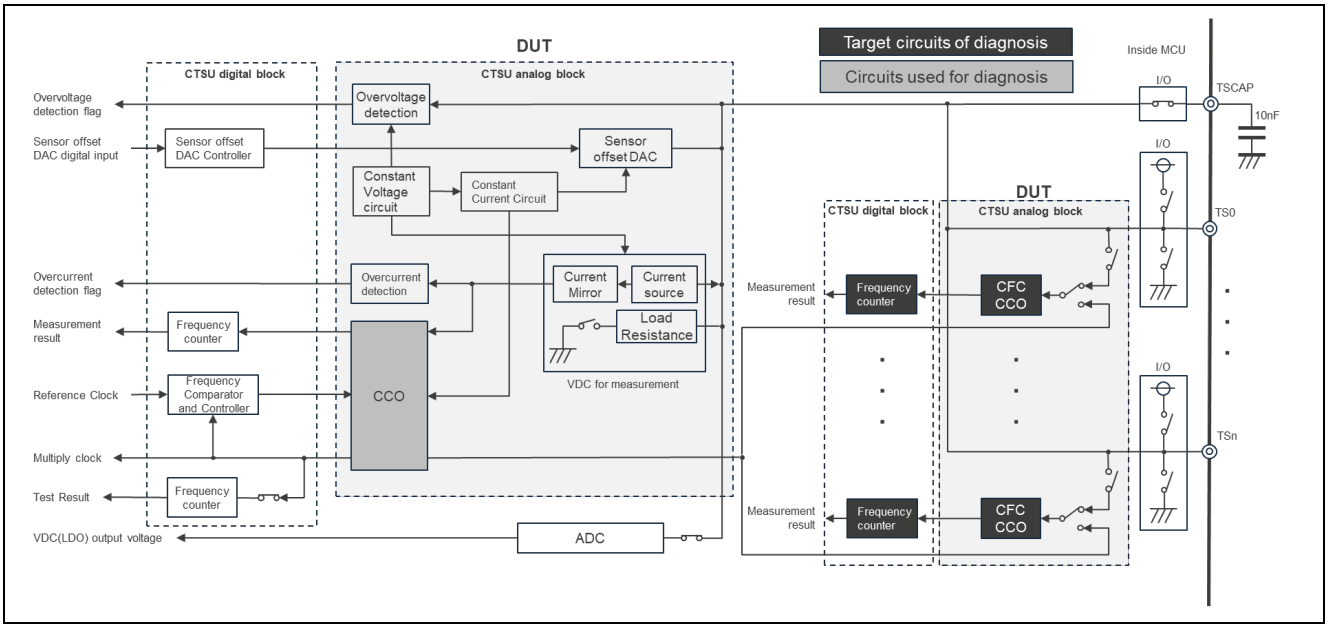

Figure 3-10 Circuit Diagram for CFC Oscillator Diagnosis

3.9.1 Measurement

In this diagnosis, measurements are performed four times for each of five conditions with different input currents, and the average value is obtained.

Table 3-35 shows the register settings for CFC oscillator diagnosis.

Table 3-35 Register Settings for CFC Oscillator Diagnosis (Common)

Register	Bit	Value	Setting
CTSUCALIB CTSUDBGR1 CTSUDBGR0	-	0x00000000	Initialization of calibration register
	CCOCALIB	1	Oscillator calibration mode
	CFCMODE	1	Calibration mode selected for CFC oscillator calibration mode
	CFCRDMD	1	CFC counter reading enabled
CTSUCRA CTSUCRAH CTSUCR2	MD2	1	Switched capacitor current and DC current
CTSUCRA CTSUCRAL CTSUCR0	CFCON	1	CFC power-on control: ON
	TXVSEL	1	VCC pin selected as a power supply for the transmit pin
CTSUCRB CTSUCRBH CTSUDCLKC	SSCNT[1:0]	0x00	SUCLK adjustment bit
CTSUCHACx (x: A, AH, AL, B, BL, 4, 0, 1, 2, 3)	CHACxxx Note	1	Measurement of the selected TS pin
CTSUCHTRCx (x: A, AH, AL, B, BL, 4, 0, 1, 2, 3)	CHTRC Note	0	CTSU channel transmission/reception control setting: reception
CTSUSO CTSUSO0 CTSUSO1	SO[9:0]	00 00000000b	Offset current
	SNUM[7:0]	0x07	Measurement time 128us
	SDPA[7:0]	0x00	Sensor drive pulse frequency : 1/2 of SUCLK

Note: Refer to the User's Manual (Hardware) for the MCU in use.

Table 3-36 shows the register setting during CFC oscillator diagnosis operation. For details on how to configure the registers, refer to the User's Manual (Hardware) for the MCU in use.

Table 3-36 Register Setting during CFC Oscillator Diagnostic Operation

Register	Bit	Value	Setting
CTSUSUCLK0 CTSUSUCLKA	SUADJ0	((N+1) * 32) – 1 N indicates the test counts N = 1,2,3,4,5	CFC scan time control and the SUCLK frequency setting

3.9.2 Condition

The CTSU power supply operates in either NM mode or LV mode depending on the user settings(see Table 3-5).

3.9.3 Determination

Compare the measurement average values obtained from each test to determine whether the result of the Nth test (N = 2, 3, 4, and 5) is greater than that of the (N-1) test. If this condition is not met, R_CTSU_Diagnosis returns FSP_ERR_CTSU_DIAG_CFC_GAIN. If it is met, R_CTSU_Diagnosis returns FSP_SUCCESS.

3.10 Diagnostic API

The diagnostic API retrieves diagnostic results. If R_CTSU_Diagnosis returns FSP_SUCCESS, the result is normal. Otherwise, the error value defined for each diagnostic is returned, and should be treated as a diagnostic error. Even if an abnormality is detected in diagnosis, diagnosis can be executed again without user operation.

3.11 Relation to Other Functions

If R_CTSU_Stop is called, the diagnostic test is suspended, and the current diagnostic state is retained. When measurement is restarted, the diagnostic test resumes from the point at which it was suspended.

If R_CTSU_Close is called, the diagnostic test is terminated, and the diagnostic state is initialized. When diagnosis is restarted, one-time tests are also executed again.

4. API Specifications

For the details on API specifications, refer to the following Application Notes that describe Touch modules.

RL78 Family CTSU Module Software Integration System Rev.2.30

RX Family QE CTSU module Firmware Integration Technology Rev.3.30

RA Flexible Software Package Documentation: CTSU(r_ctsu)

For details on the API related to the functional safety, refer to “2. API Information” and “3. API Functions” for RL78 and RX families.

5. Sample Application Flowchart

For details on the flowcharts, refer to the following Application Notes that describe Touch modules.

RL78 Family CTSU Module Software Integration System Rev.2.30

RX Family QE CTSU module Firmware Integration Technology Rev.3.30

For details on the sample program related to the diagnostic function, refer to Section “1.4.5 Diagnosis Mode” for RL 78 family and RX family microcontrollers. When using RA family microcontrollers, refer to the same material as RX family microcontrollers.

6. Project Creation using QE for Capacitive Touch

This chapter describes how to create a project using QE for Capacitive Touch. For more detailed explanation, refer to the following Application Notes.

RA Family Using QE and FSP to Develop Capacitive Touch Applications

RX Family Using QE and FIT to Develop Capacitive Touch Applications

RL78 Family Using QE and SIS to Develop Capacitive Touch Applications

6.1 RA Family

1. Create a new project.

2. As shown in Figure 6-1, add the Touch middleware on the [Stacks] tab of the RA Smart Configurator.

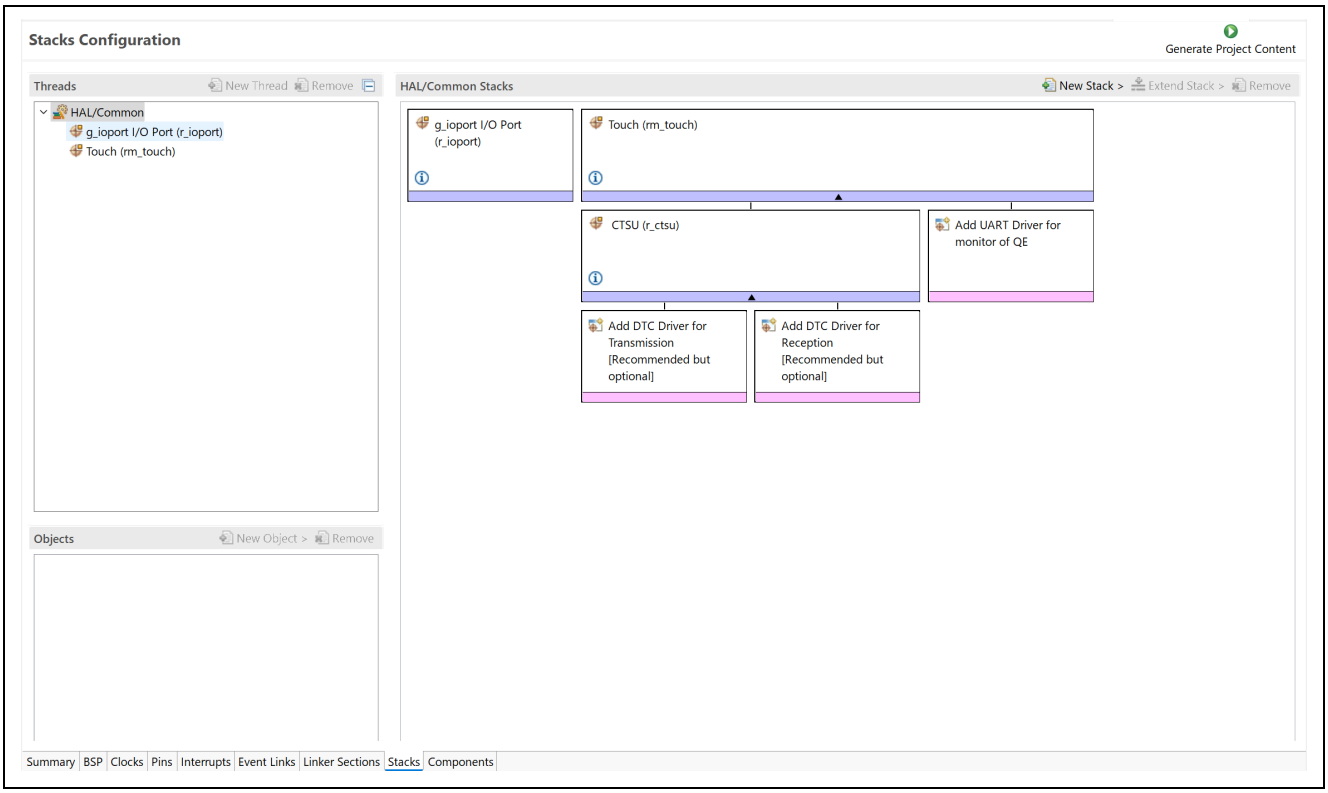

Figure 6-1 Add the Touch Middleware

3. If you are using an MCU with CTSU2, ADC drivers must be added. For the procedure to configure the ADC driver, refer to Step 4 through 11. If you are using an MCU with CTSU1, proceed to Step 12.

4. As shown in Figure 6-2, add two ADC drivers

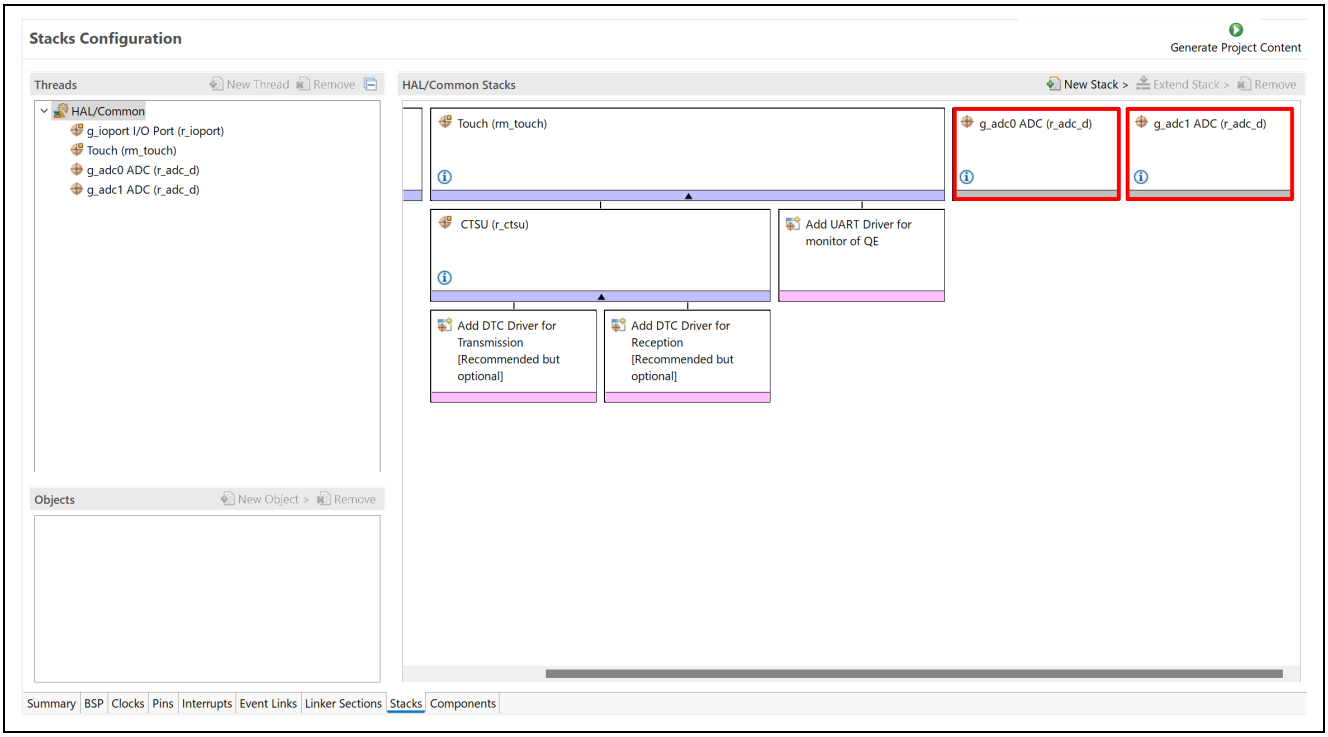

Figure 6-2 Add ADC drivers

5. Starting from the next section, the procedures to set the ADC drivers are described for each microcontroller. Refer to the steps shown in Table 6-1 according to the MCU in use.

Table 6-1 ADC Driver Settings and Steps to Be Referred for RA Family Products

Microcontroller	CTSU Power Operating Mode	Steps to be referred
RA0L1	NM mode	6, 7
	LV mode	8, 9
RA2E1, RA2L1, RA4L1	NM mode	10, 11
	LV mode	

6. If you are using an RA0L1 in NM mode, select “g_adc0 ADC” and click [Properties] at the lower left. As shown in Figure 6-3, change the following settings.

    1. Set [Interrupt Support] to “Disabled”
    2. Change the name to ”g_adc_ctsu” in [General] > [Name].
    3. Select “CTSU TSCAP voltage” in [Input] > [A/D Input channel]
    4. Select “Software” in [Interrupt] > [Start trigger source]

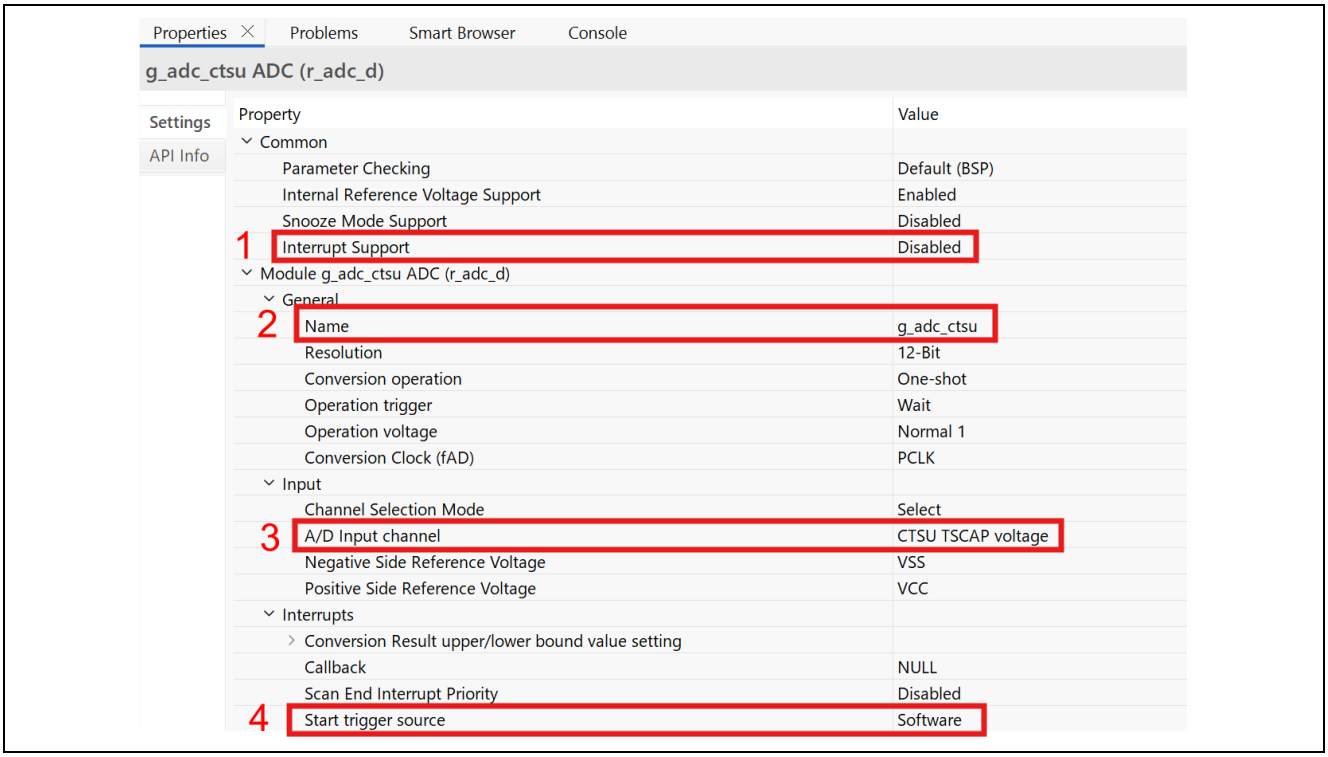

Figure 6-3 Configure "g_adc_ctsu" (RA0L1/NM mode)

7. Select “g_adc1 ADC” and click [Properties] and change the following settings as shown in Figure 6-4.

1. Set [Internal Reference Voltage Support] to “Enabled” in [Common]
2. Change the name to “g_adc_ctsu_ivref” in [General] > [Name]
3. Select “No-wait” in [General] > [Operation trigger]
4. Select “Normal 2” in [General] > [Operation voltage]
5. Select “Internal reference voltage” in [Input] > [A/D Input channel]
6. Select “Software” in [Interrupts] > [Start trigger source]

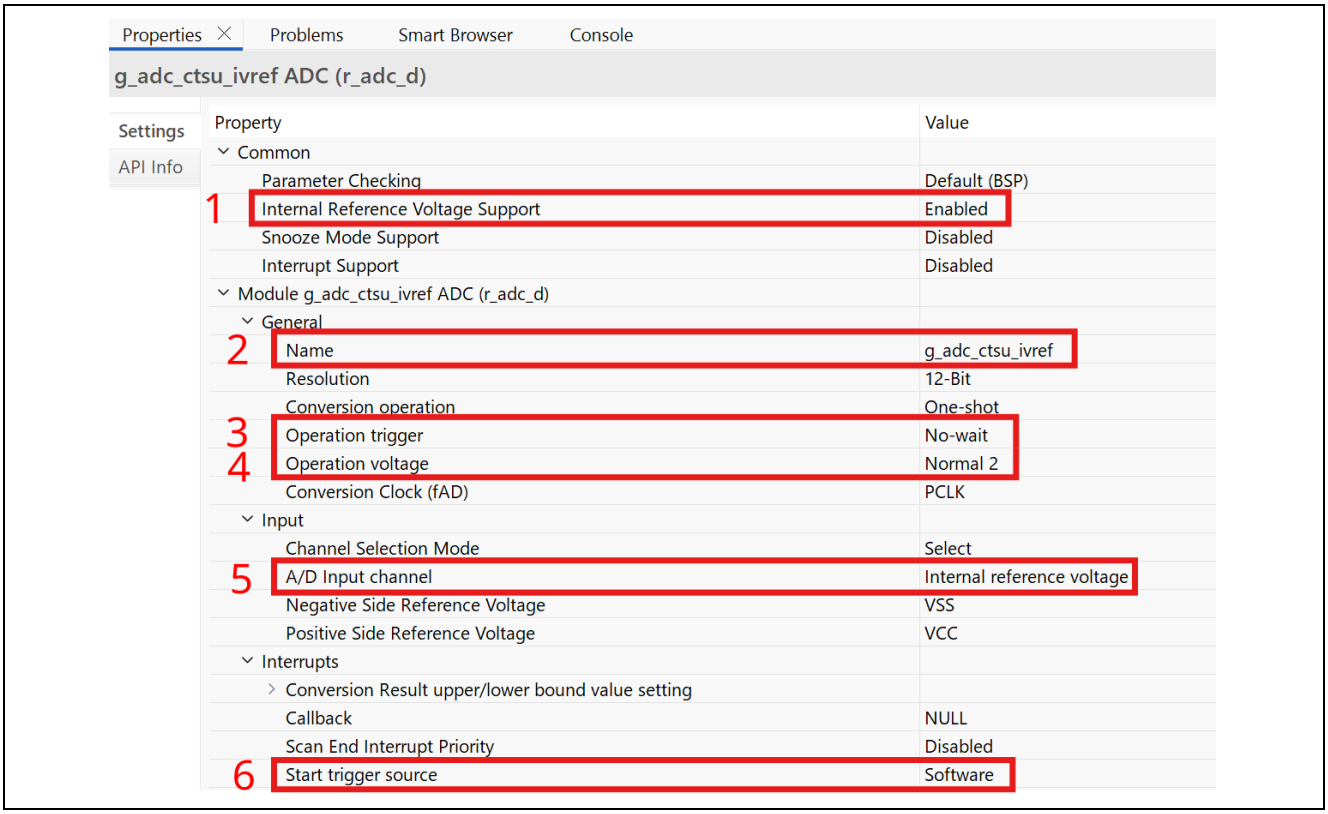

Figure 6-4 Configure “g_adc_ctsu_ivref” (RA0L1/NM mode)

8. If you are using an RA0L1 in LV mode, select “g_adc0 ADC” and click [Properties] at the lower left. Change the following settings as shown in Figure 6-5

    1. Set [Interrupt Support] to “Disabled”
    2. Change the name to ”g_adc_ctsu” in [General] > [Name]
    3. Select “Low voltage 1” in [General] > [Operation voltage]
    4. Select “[PCLK/2” in [General] > [Conversion Clock (fAD)]]
    5. Select “CTSU TSCAP voltage” in [Input] > [A/D Input channel]
    6. Select “Software” in [Interrupt] > [Start trigger source]

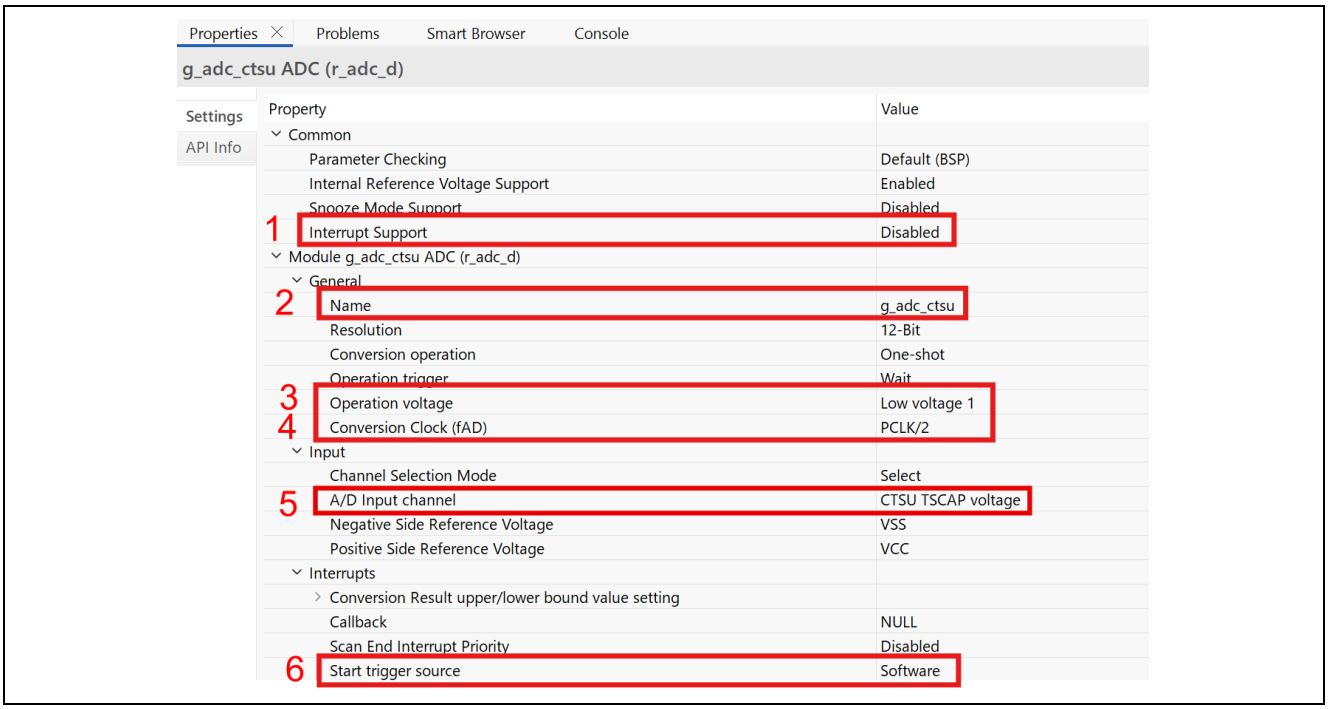

Figure 6-5 Configure “g_adc_ctsu_ivref” (RA0L1/LV mode)

9. Select “g_adc1 ADC” and click [Properties] and change the following settings as shown in Figure 6-6.

1. Set [Internal Reference Voltage Support] to “Enabled” in [Common]
2. Change the name to “g_adc_ctsu_ivref” in [General] > [Name]
3. Select “No-wait” in [General] > [Operation trigger]
4. Select ”Low Voltage 2” in [General] > [Operation voltage]
5. Select ”PCLK/2” in [General] > [Conversion Clock (fAD)]
6. Select “Internal reference voltage” in [Input] > [A/D Input Channel]
7. Select “Software” in [Interrupt] > [Start trigger source]

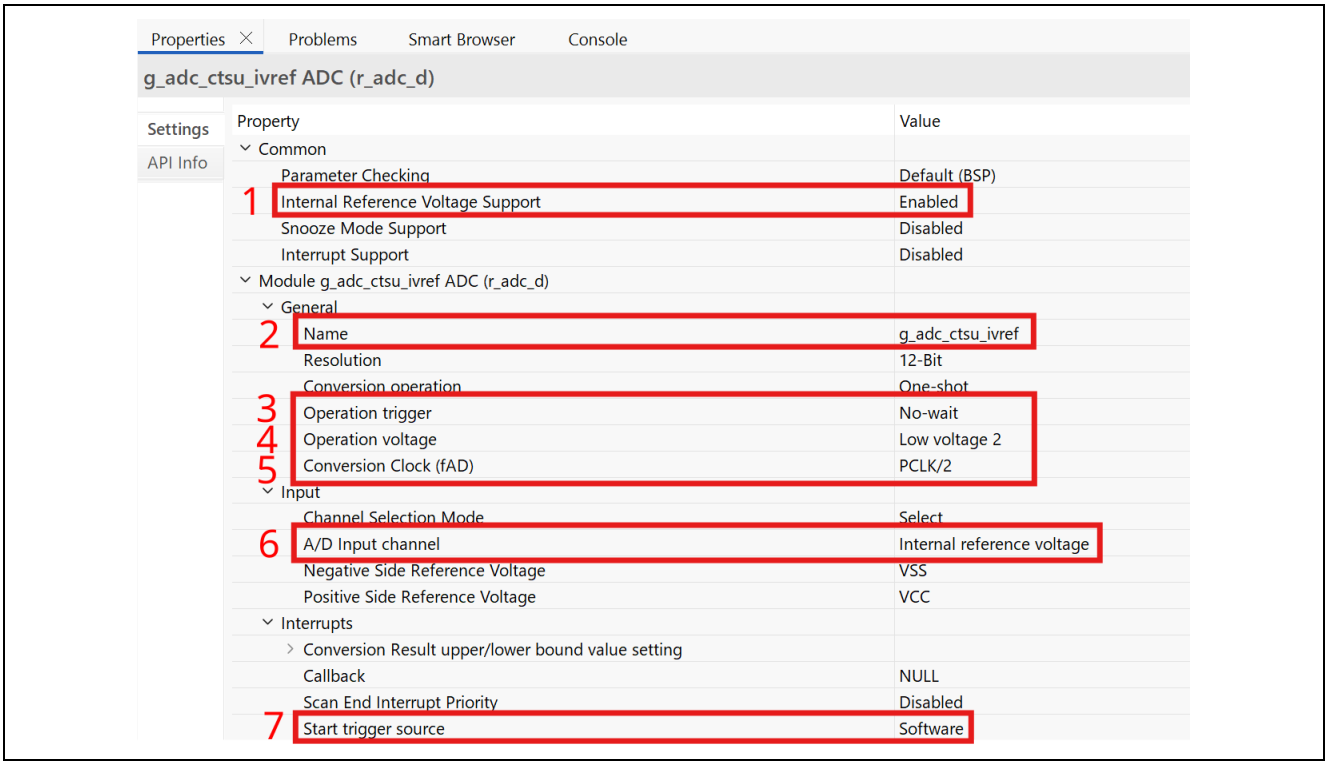

Figure 6-6 Configure "g_adc_ivref" (RA0L1/LV mode)

10. If you are using an RA2L1 or RA4L1, select “g_adc0 ADC” and click [Properties] at the lower left. As shown Figure 6-7 and Figure 6-8, change the following settings.

    1. Change the name to ”g_adc_ctsu” in [General] > [Name]
    2. Select “Channel 16” in [Input] > [Channel Scan Mask]
    3. Select “Channel 16” in [Input] > [Additon/Averaging Mask]
    4. Select [Average four samples] in [Input] > [Add/Average Count]

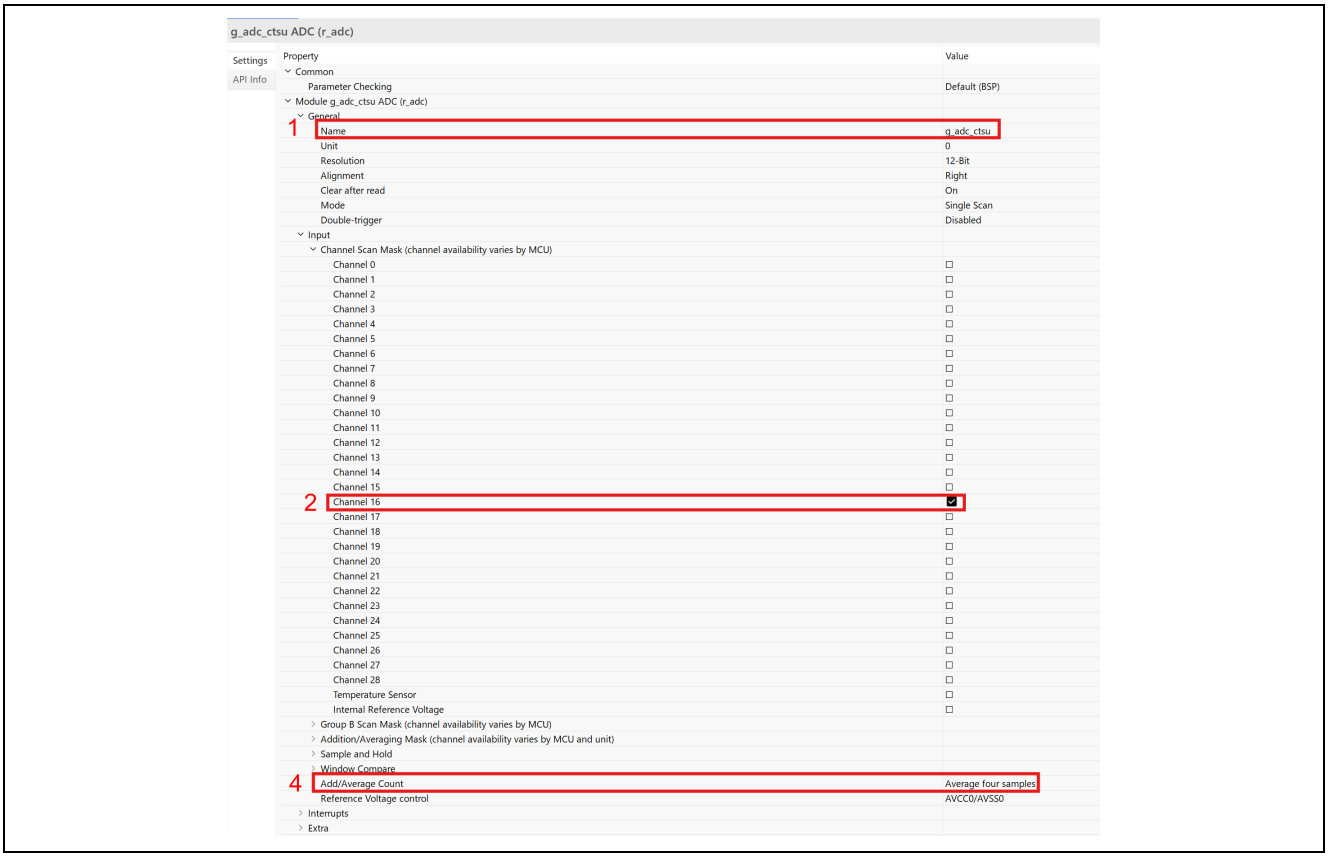

Figure 6-7 Configure "g_adc_ctsu" (RA2E1, RA2L1, RA4L1)

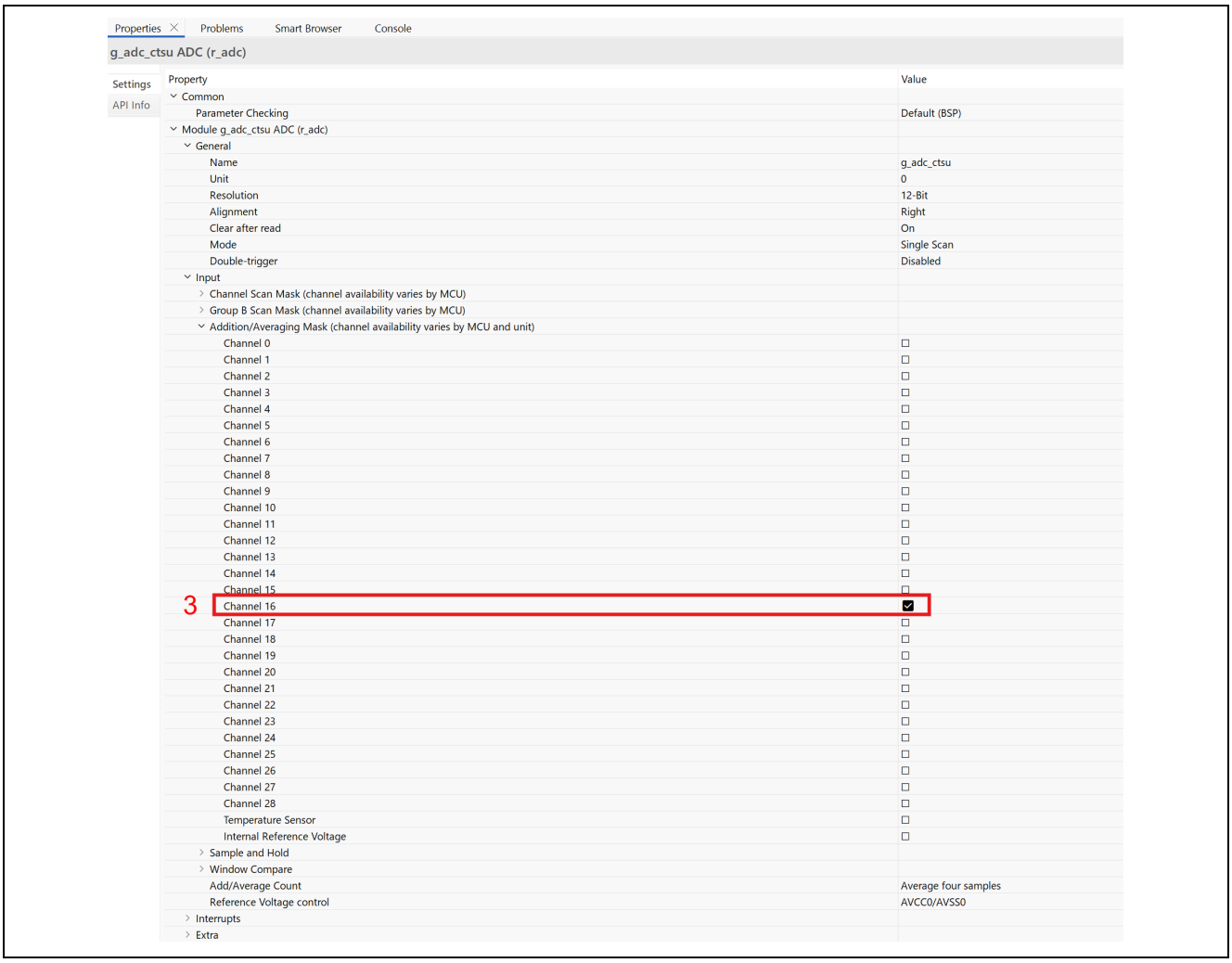

Figure 6-8 Configure "g_adc_ctsu" Addition/Averaging Mask (RA2E1, RA2L1, RA4L1)

11. Select “g_adc1 ADC” and click [Properties] at the lower left. As shown in Figure 6-9 and Figure 6-10, change the following settings.

    1. Change the name to ”g_adc_ivref” in [General] > [Name]
    2. Select “Internal Reference Voltage” in [Input] > [Channel Scan Mask]
    3. Select “Internal Reference Voltage” in [Input] -> [Additon/Averaging Mask]
    4. Select [Average four samples] in [Input] > [Add/Average Count]

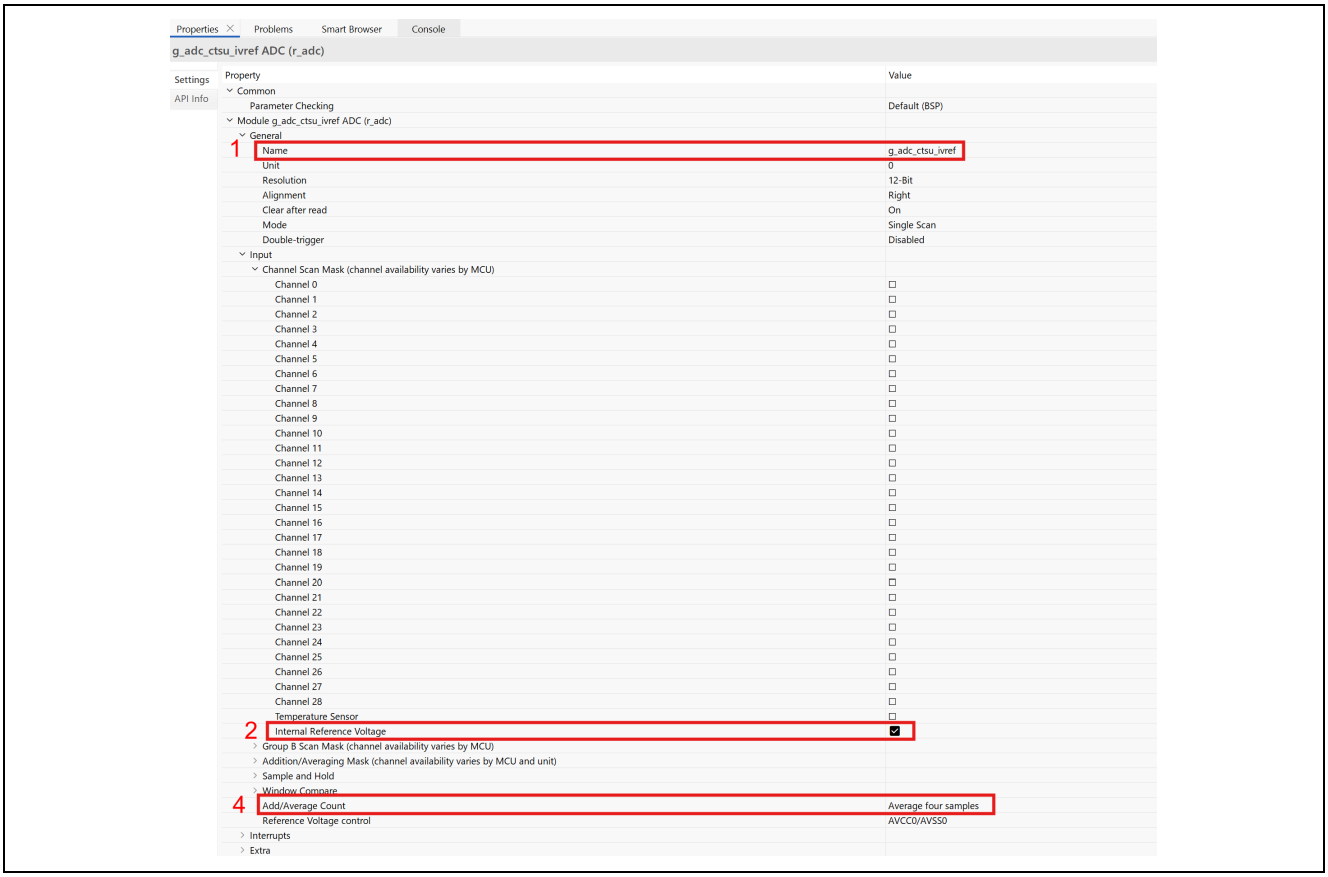

Figure 6-9 Configure "g_ctsr_ivref" (RA2E1, RA2L1, RA4L1)

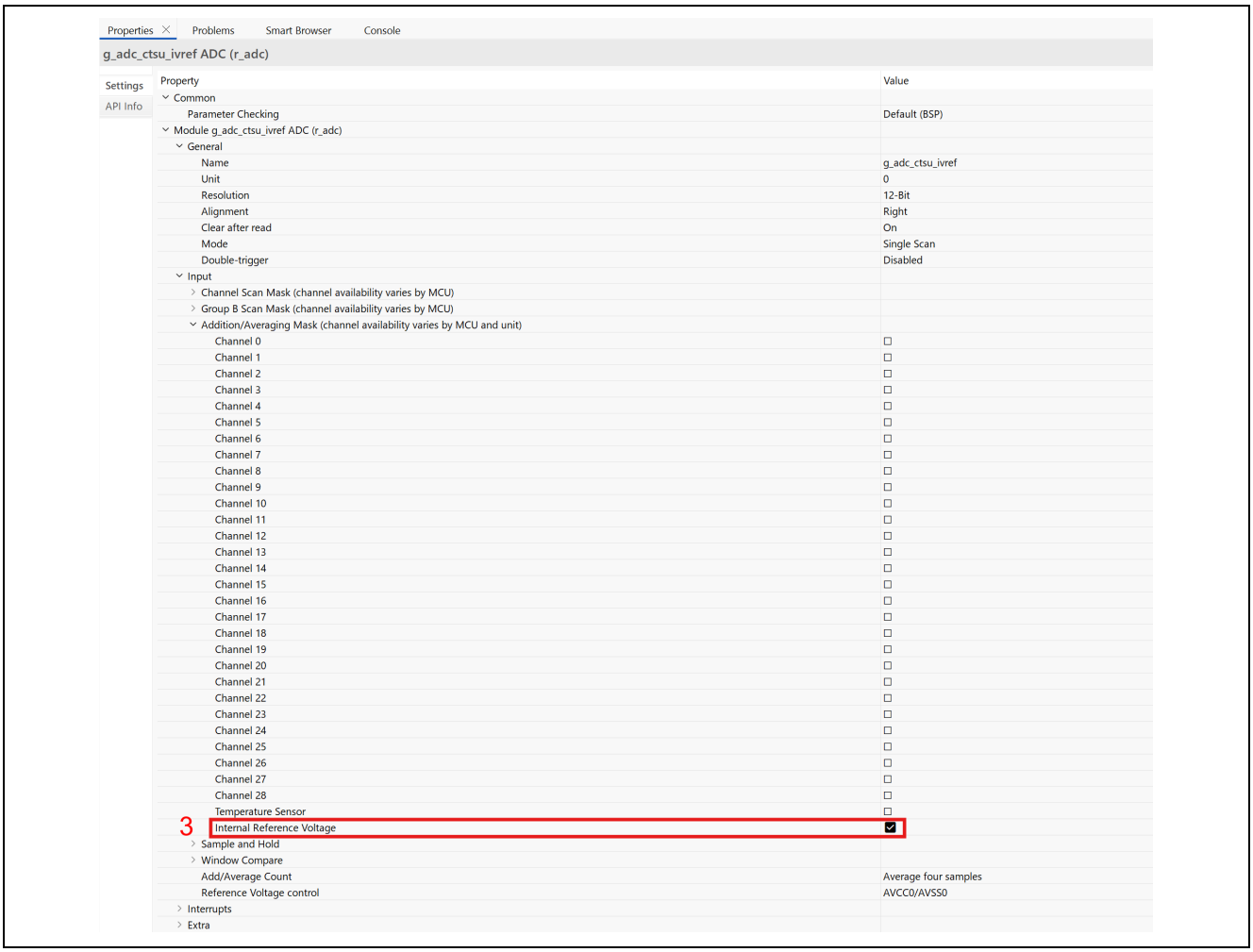

Figure 6-10 Configure "g_adc_ctsu_ivref" Addition/Averaging Mask (RA2E1, RA2L1, RA4L1)

12. In the RA Smart Configurator, select the TS pin to be used for CTSU measurement. (For CTSU1, additionally, the TS pin for Sensor Offset Diagnosis must be selected.)

13. Click [Generate Project Content] at the upper right of the RA Smart Configurator, generate code.

14. Open [Renesas Views] > [Renesas QE] > [Cap Touch Workflow (QE)]. As shown in Figure 6-12, click [Prepare a Configuration] and select an existing configuration or create a new configuration

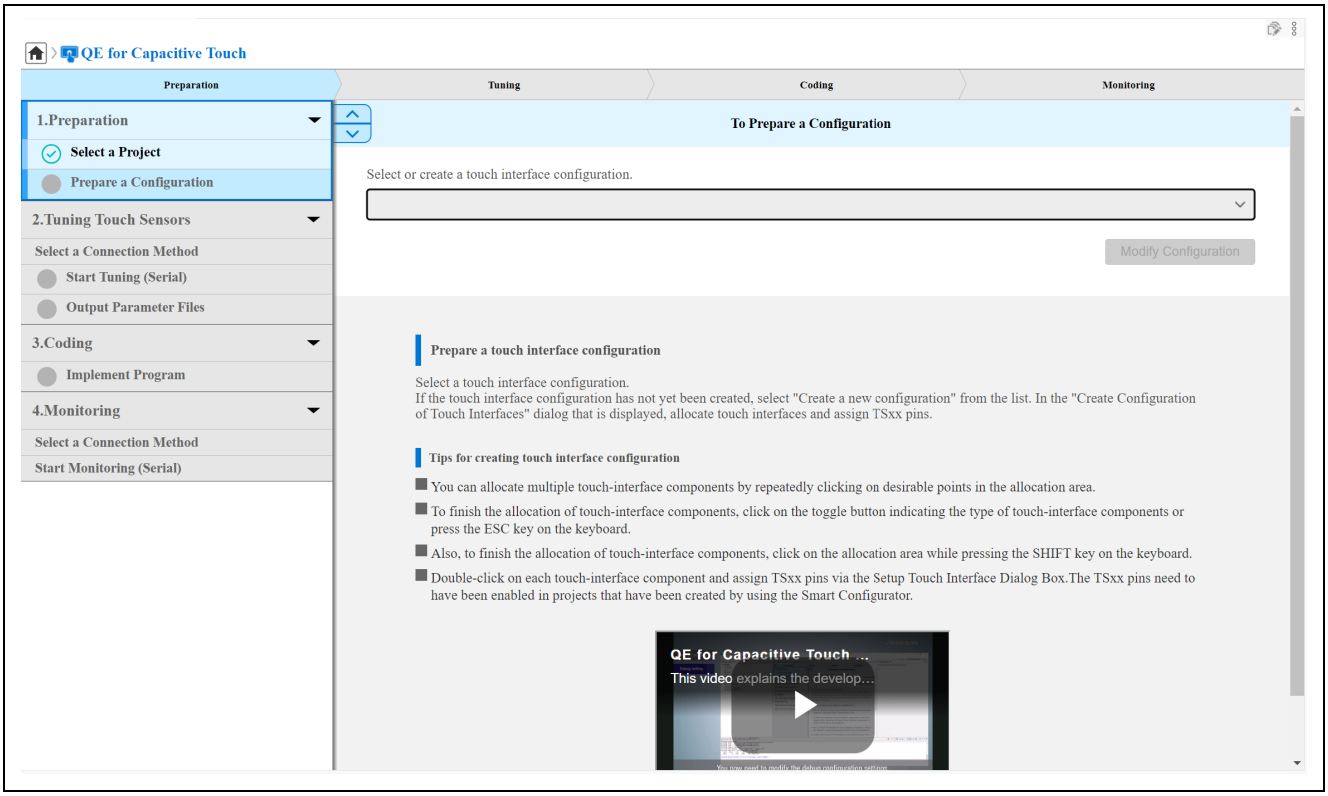

Figure 6-11 [Prepare a Configuration] in Cap Touch Workflow (QE)

15. Configure the electrode to be used for CTSU measurement. For CTSU1, place a Diagnosis pin and assign it to the TS pin used for Sensor Offset Diagnosis as shown in Figure 6-12.

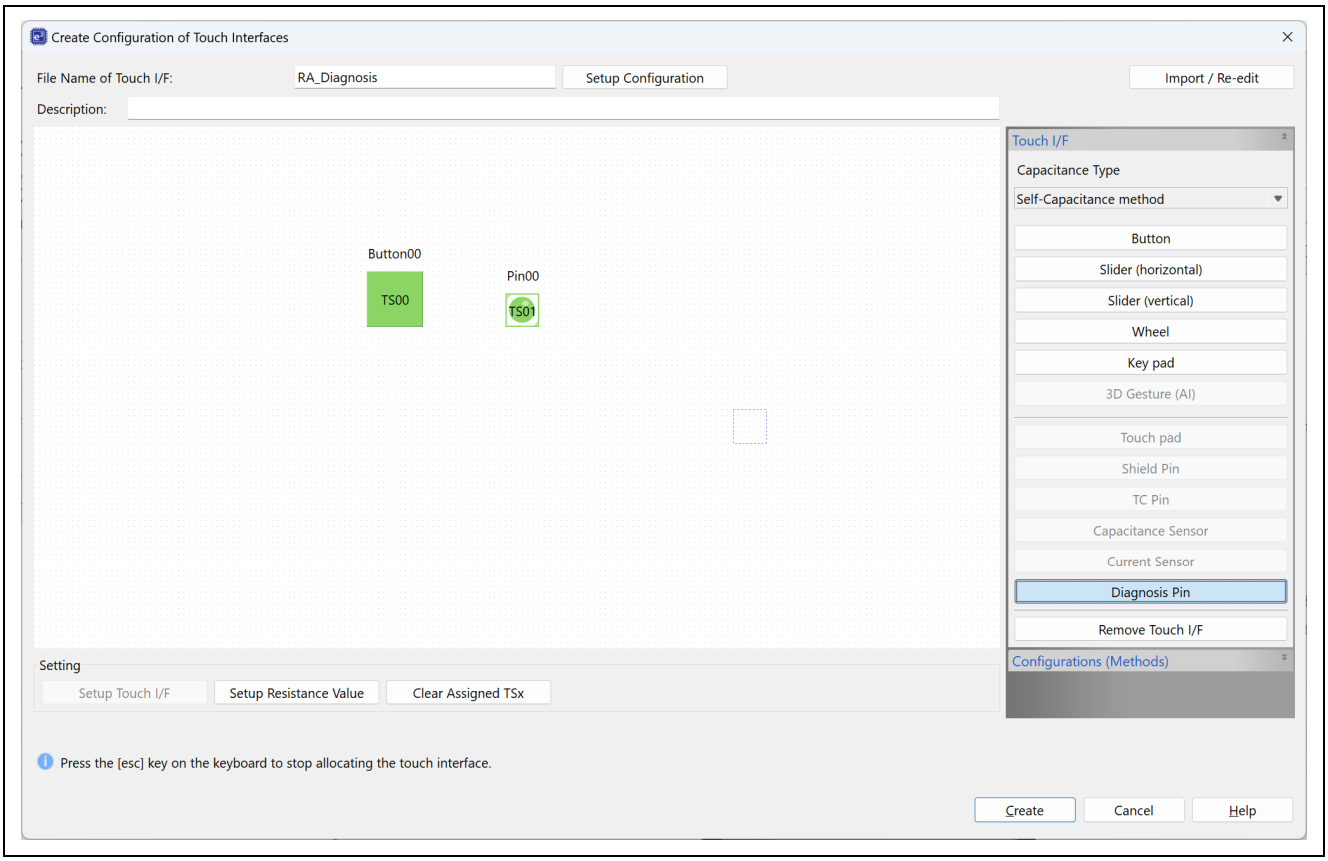

Figure 6-12 Configure TS Pin for Diagnosis in Touch Interface Configuration

16. As shown in Figure 6-13, click [Start Tuning]. Complete the tuning operation according to the QE instructions.

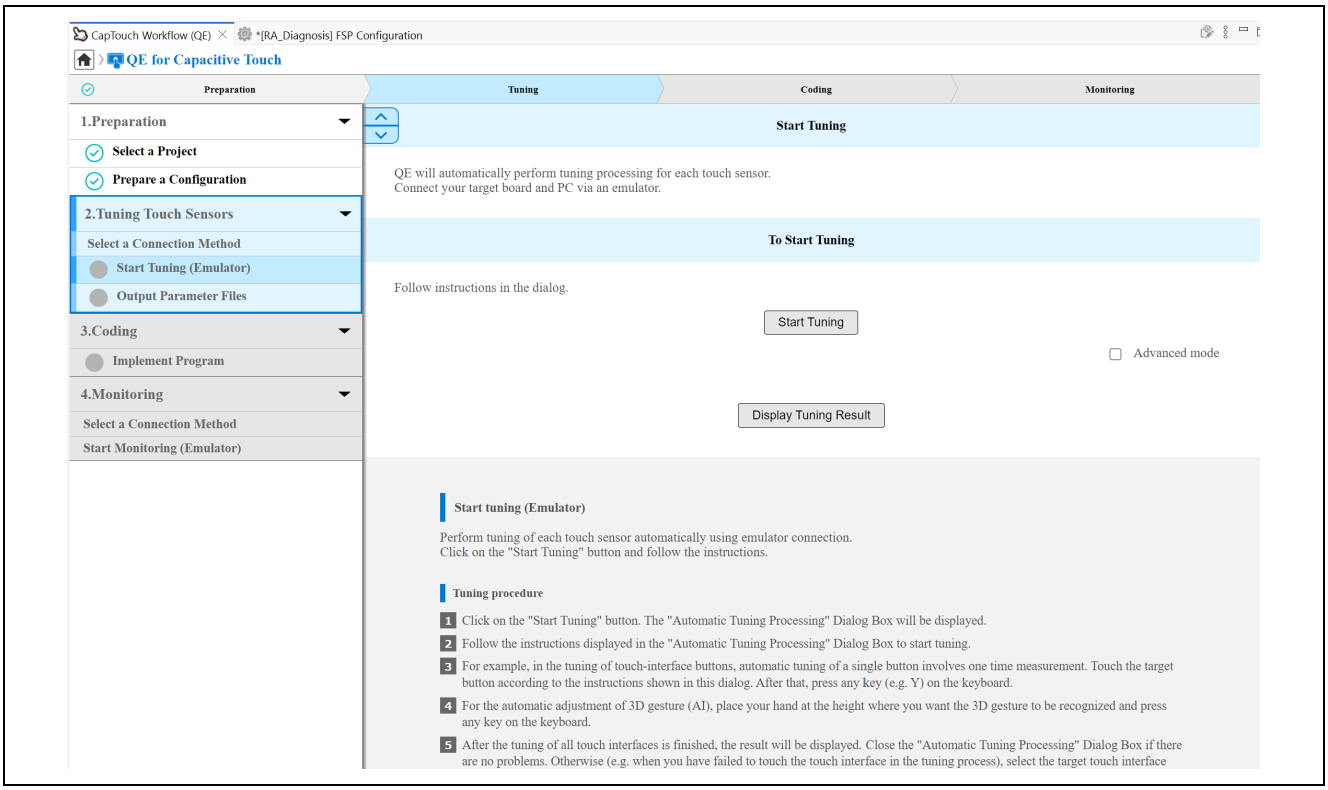

Figure 6-13 Start Tuning

17. As shown in Figure 6-14, check [Use diagnostic code] and click [Output Parameter Files].

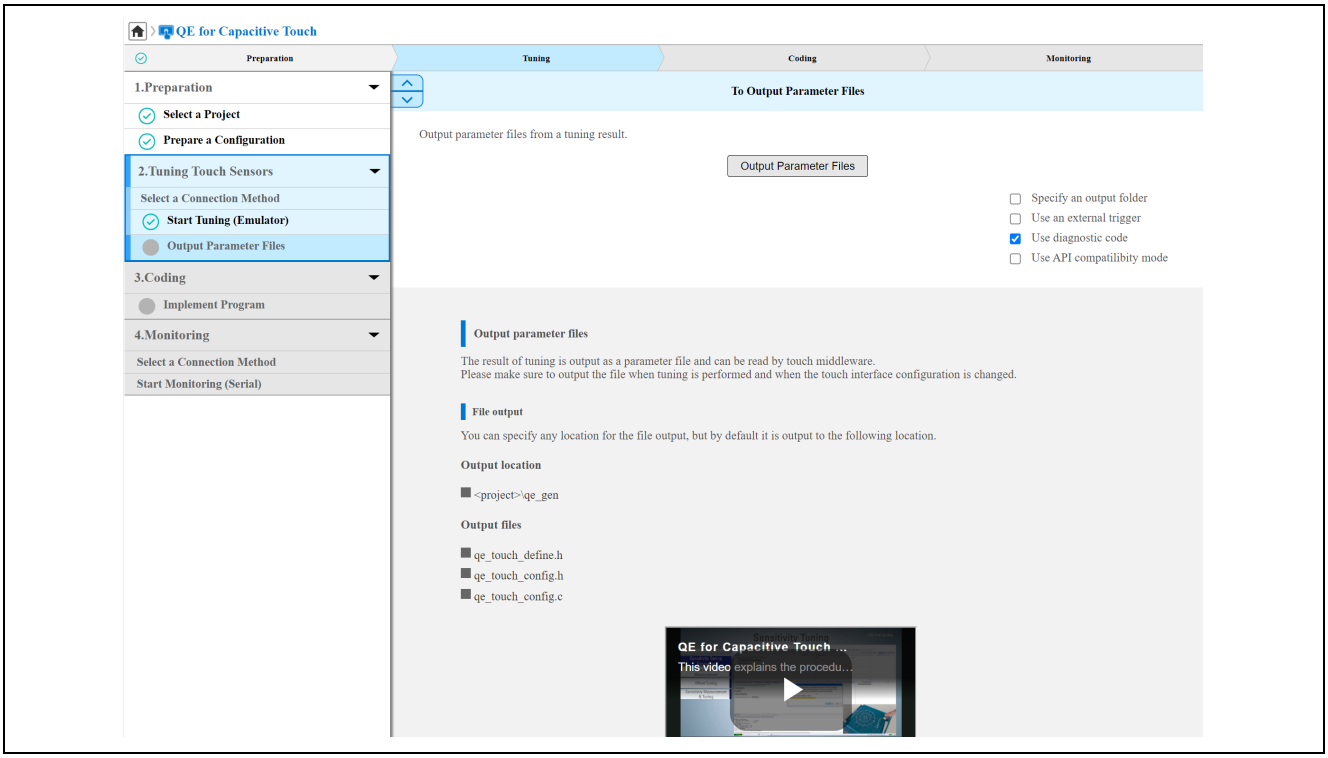

Figure 6-14 Output Diagnostic Code

18. Click [Implement Program] -> [Show Samples] to open the [Show Sample Code] window. Click [Output to a File] to implement the sample code.

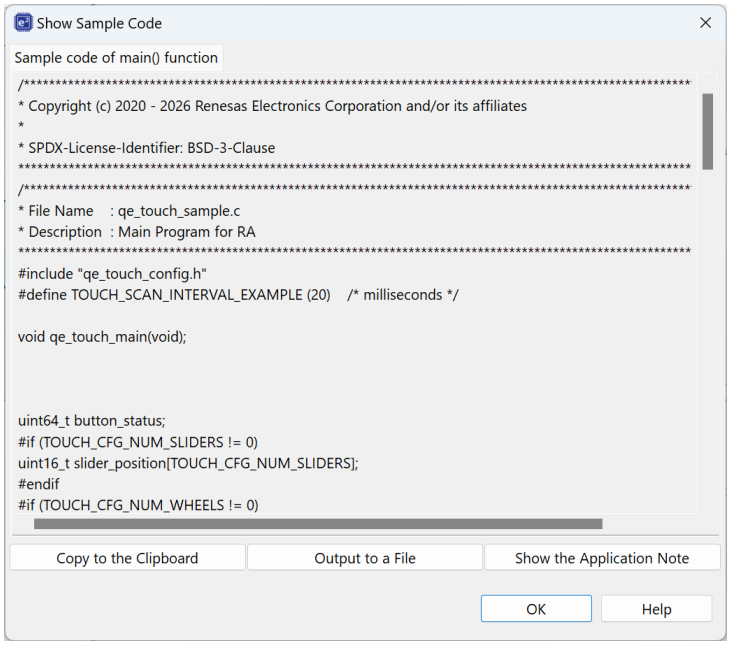

Figure 6-15 Implement Sample Code

6.2 RL78 Family

1. Create a new project.

2. As shown in Figure 6-16, add the Touch middleware and the CTSU driver on the Smart Configurator.

3. In the RA Smart Configurator, select the TS pin to be used for CTSU measurement.

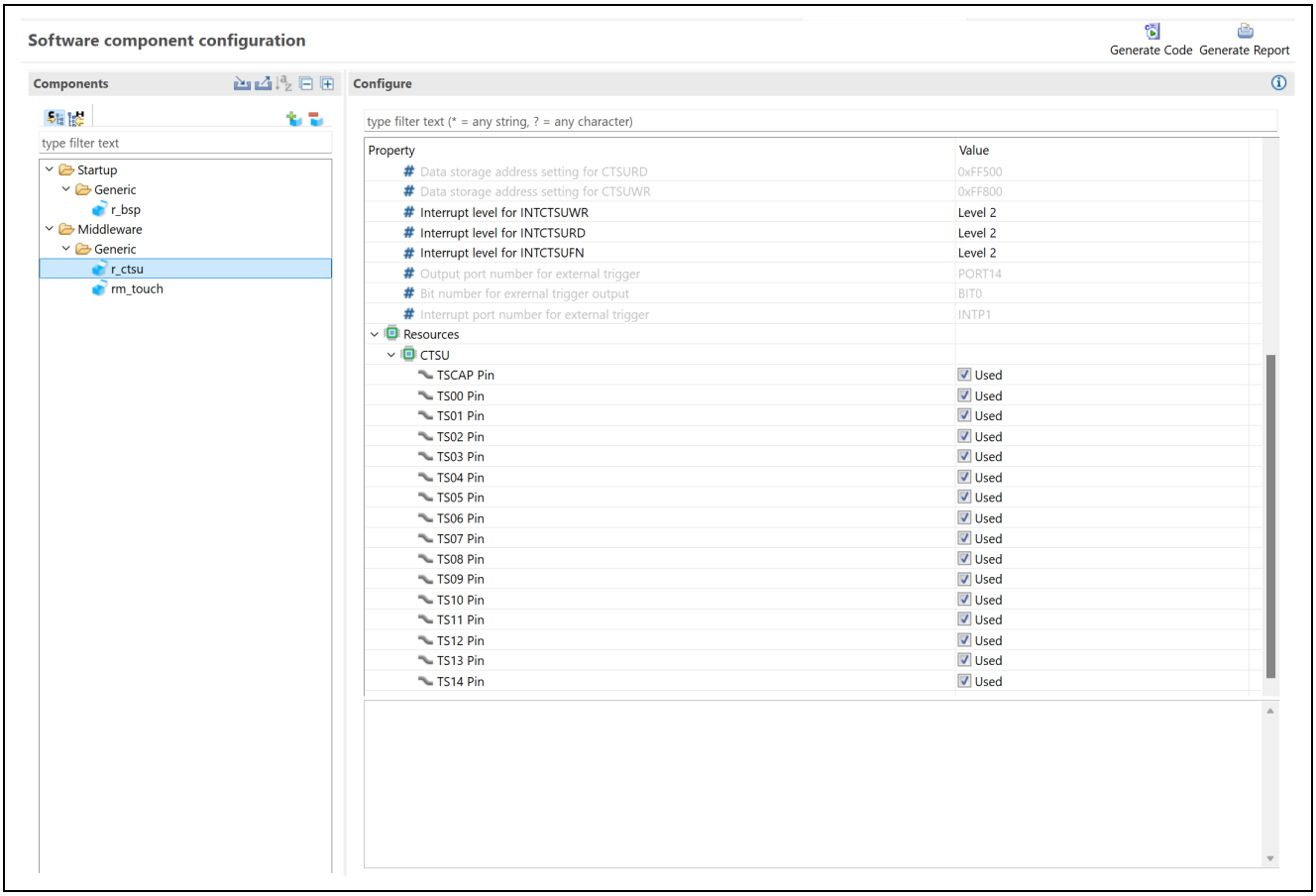

Figure 6-16 Smart Configurator (RL78)

4. If you are using an MCU with CTSU2, the ADC drivers must be added. For the procedure to configure the ADC driver, refer to Step 5 to 8. If you are using an MCU with CTSU1, proceed to Step 9

5. The following steps describe how to configure the ADC driver for each MCU. Refer to the appropriate steps according to the MCU in use.

Table 6-2 ADC Driver Settings and Steps to Be Referred for RL78 Family Products

Microcontroller	CTSU Power Operating Mode	Steps to be referred
RL78/G22	NM mode	Step 6
	LV mode	
RL78/G23, RL78/L23	NM mode	Step 7
	LV mode	
RL78/F22, RL78/F25	NM mode	Step 8

6. If you are using an RL78/G16, add the AD converter “Config_ADC”. Change the following settings as shown in Figure 6-17
   1. Select “One-shot select mode” in [Operation mode setting].
   2. Select “Internal reference voltage output” in [A/D channel selection].
   3. Uncheck “Use AD interrupt (INTAD) ” in [Interrupt setting].

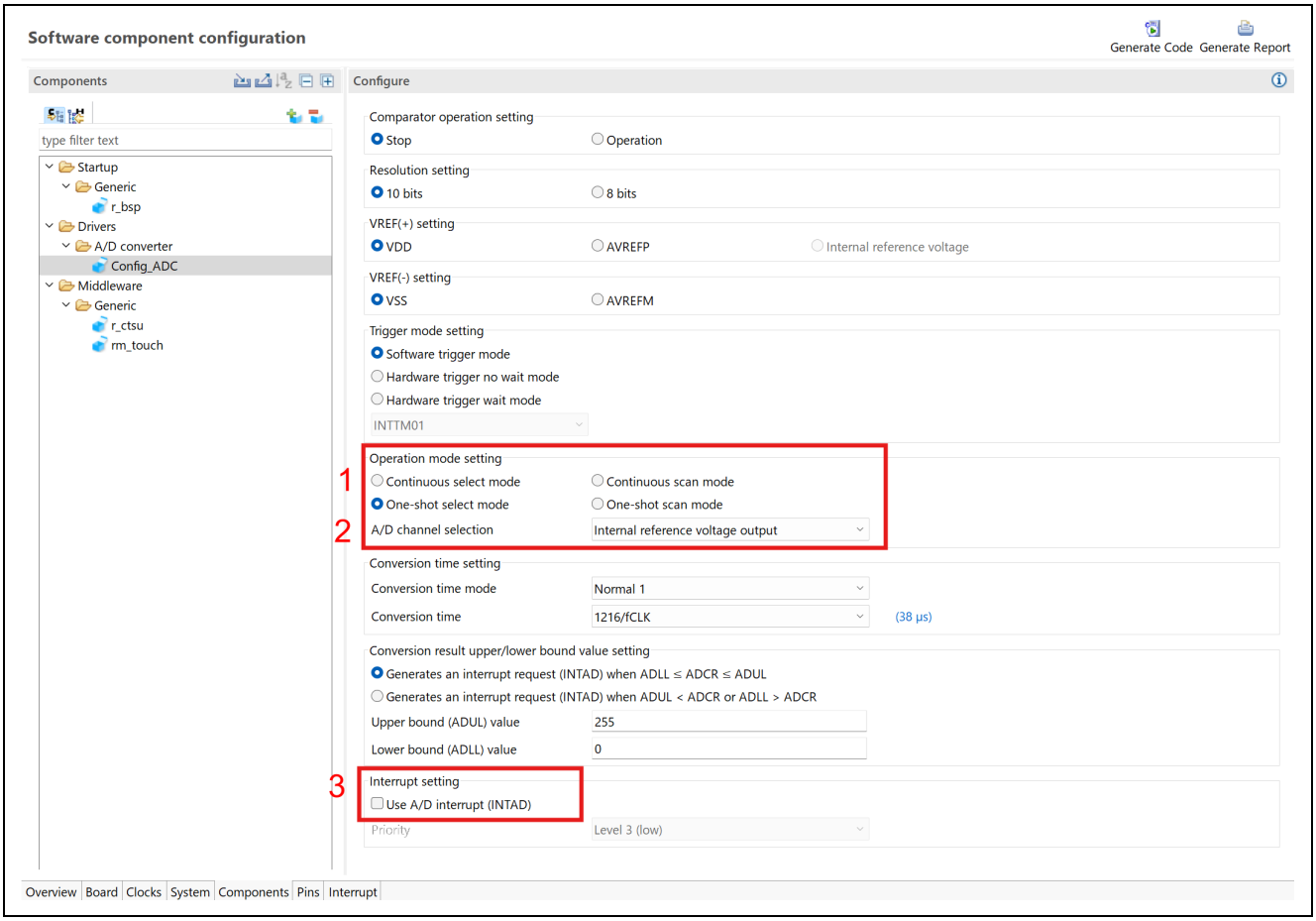

Figure 6-17 Configure ADC driver (RL78/G22)

7. If you are using an RL78/G23 or RL78/L23, add the AD converter “Config_ADC” and change the following setting as shown in Figure 6-18.
   1. Select “12 bits” in [Resolution setting]
   2. Select “One-shot select mode” in [Operation mode setting]
   3. Select “Internal reference voltage output” in [Operation mode setting]
   4. Select “Normal 2” (NM mode) or “Low voltage 2” (LV mode) in [Conversion time setting] > [Conversion time mode]
   5. Uncheck “Use A/D interrupt (INTAD)” in [Interrupt setting]

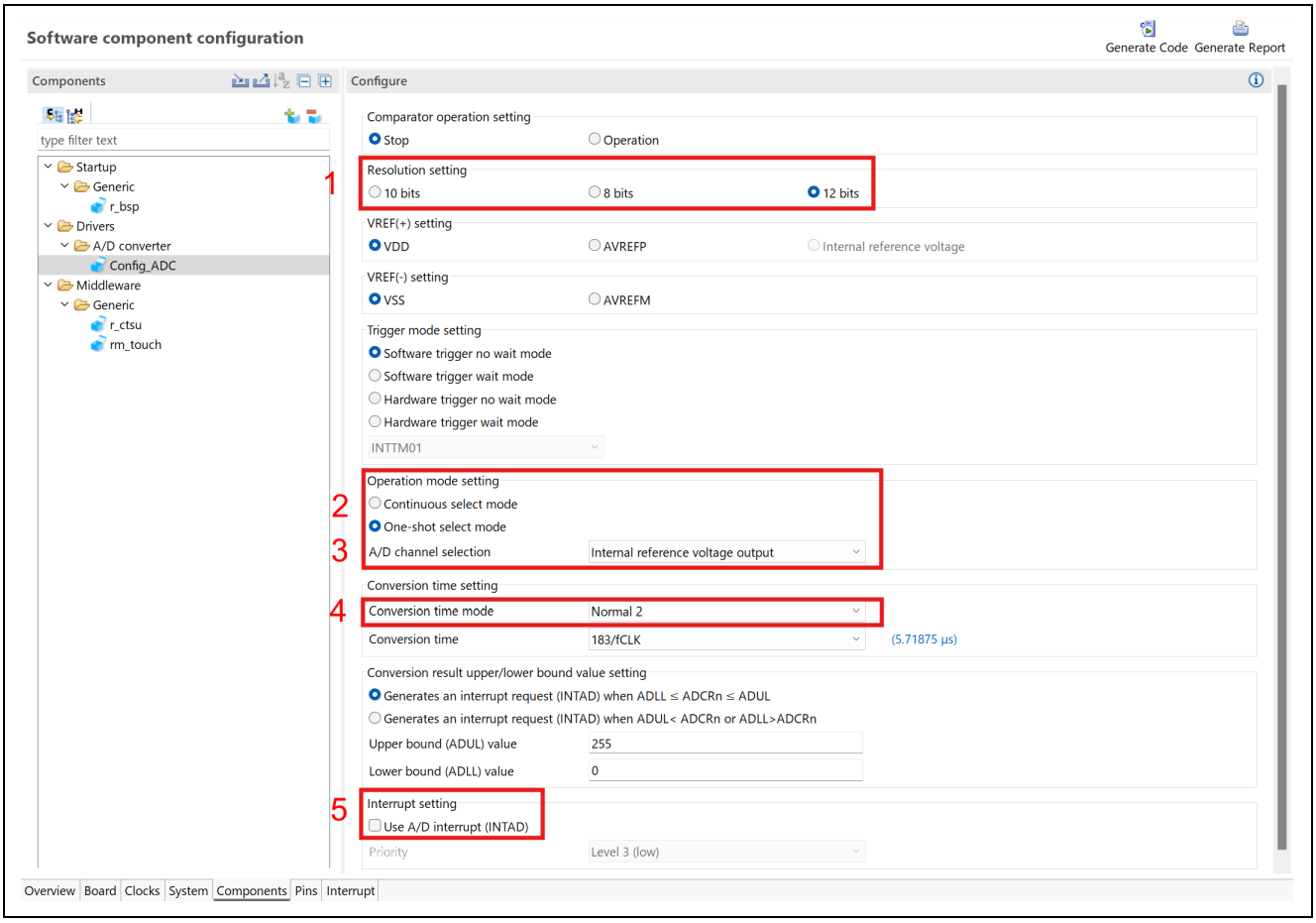

Figure 6-18 Configure ADC driver (RL78/G23, RL78/L23)

8. If you are using an RL78/F22 or RL78/F25, add the 12-bit AD single-scan “Config_ S12AD0”. Change the following settings as shown in Figure 6-19 and Figure 6-20.
   1. Select “Internal reference voltage” in [Analog input channel setting].
   2. Uncheck “Enabled AD conversion end interrupt (INTAD)” in [Interrupt setting].
   3. Select “Average mode” in [Data register setting] > [Addition/average mode]
   4. Select “4-time (addition 3 times)” in [Data register setting] > [Addition count]

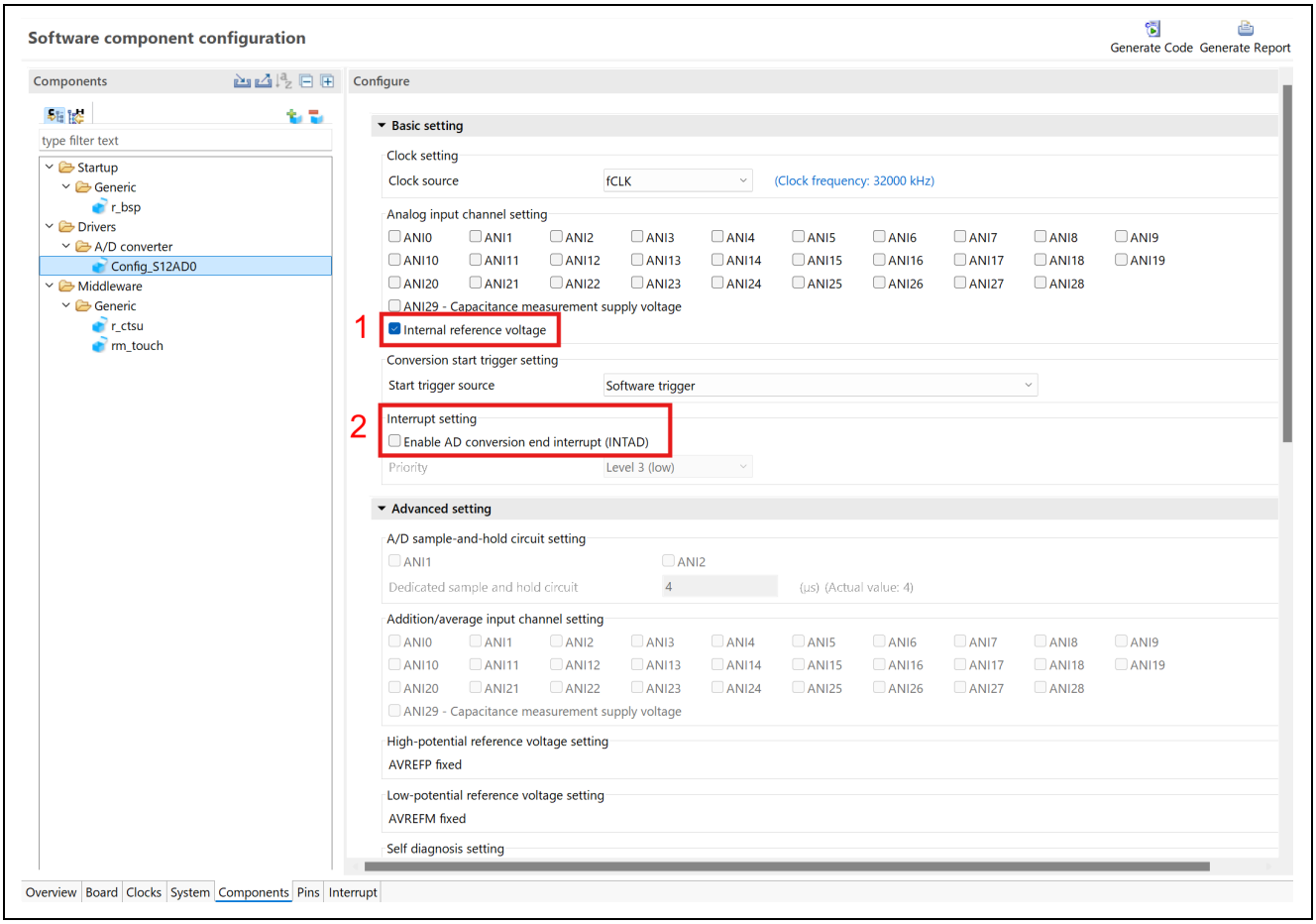

Figure 6-19 Configure ADC Driver Reference (RL78/F22, RL78F25)

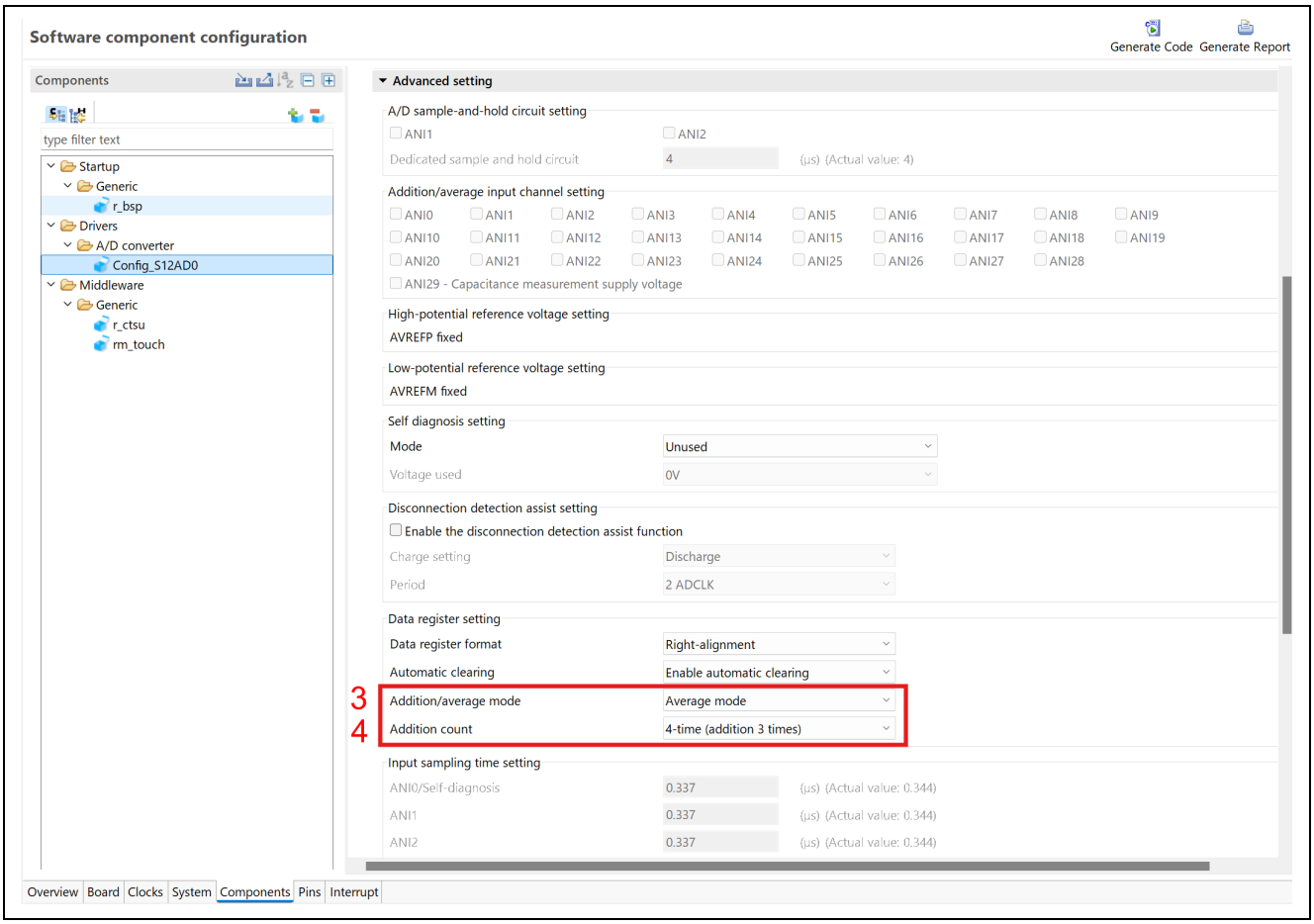

Figure 6-20 Configure ADC Driver (RL78/F22, RL78F25)

9. Click [Generate Code] at the upper right of the Smart Configurator to generate code.

10. Open [Renesas Views] > [Renesas QE] > [Cap Touch Workflow (QE)]. As shown in Figure 6-21, click [Prepare a Configuration] and select an existing configuration or create a new configuration.

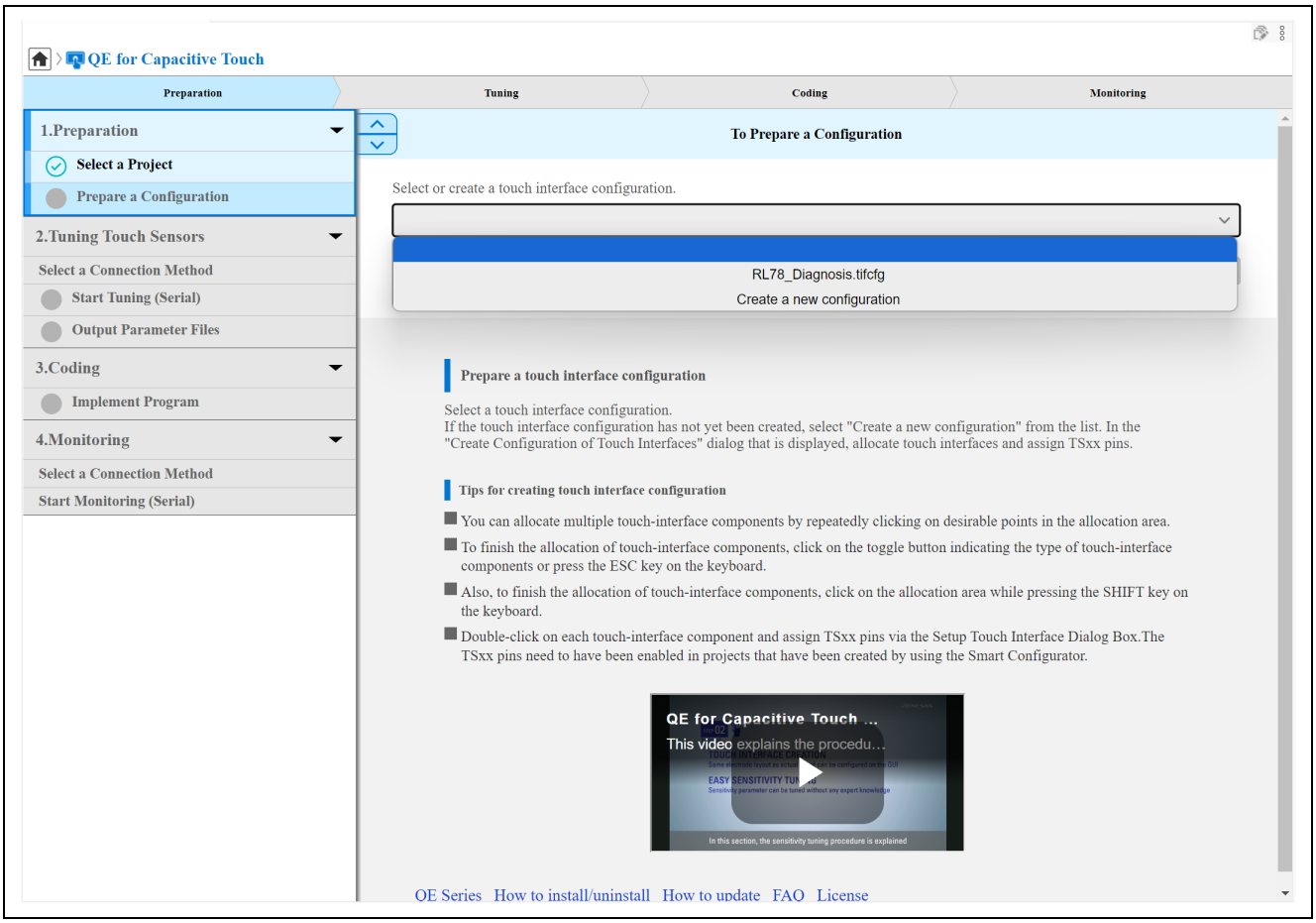

Figure 6-21 [Prepare a Configuration] in Cap Touch Workflow (QE) (RL78)

11. Configure the electrode to be used for CTSU measurement.as shown in Figure 6-22. Configuration of the diagnostic pin is not required in this step.

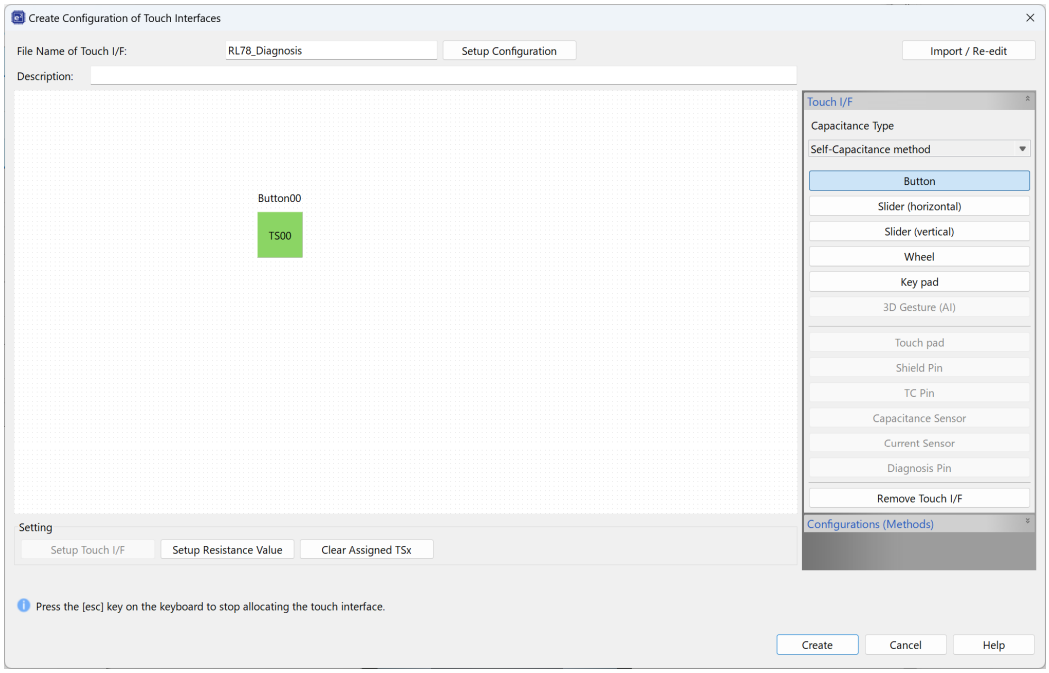

Figure 6-22 Configure TS Pin in Touch Interface Setting (RL78)

12. Using the QE for Capacitive Touch, implement the sample code following the same steps described in Section 6.1 RA Family, Steps 16 through 18.

6.3 RX Family

1. Create a new project.

2. As shown in Figure 6-23, add the Touch middleware and the CTSU driver on the Smart Configurator.

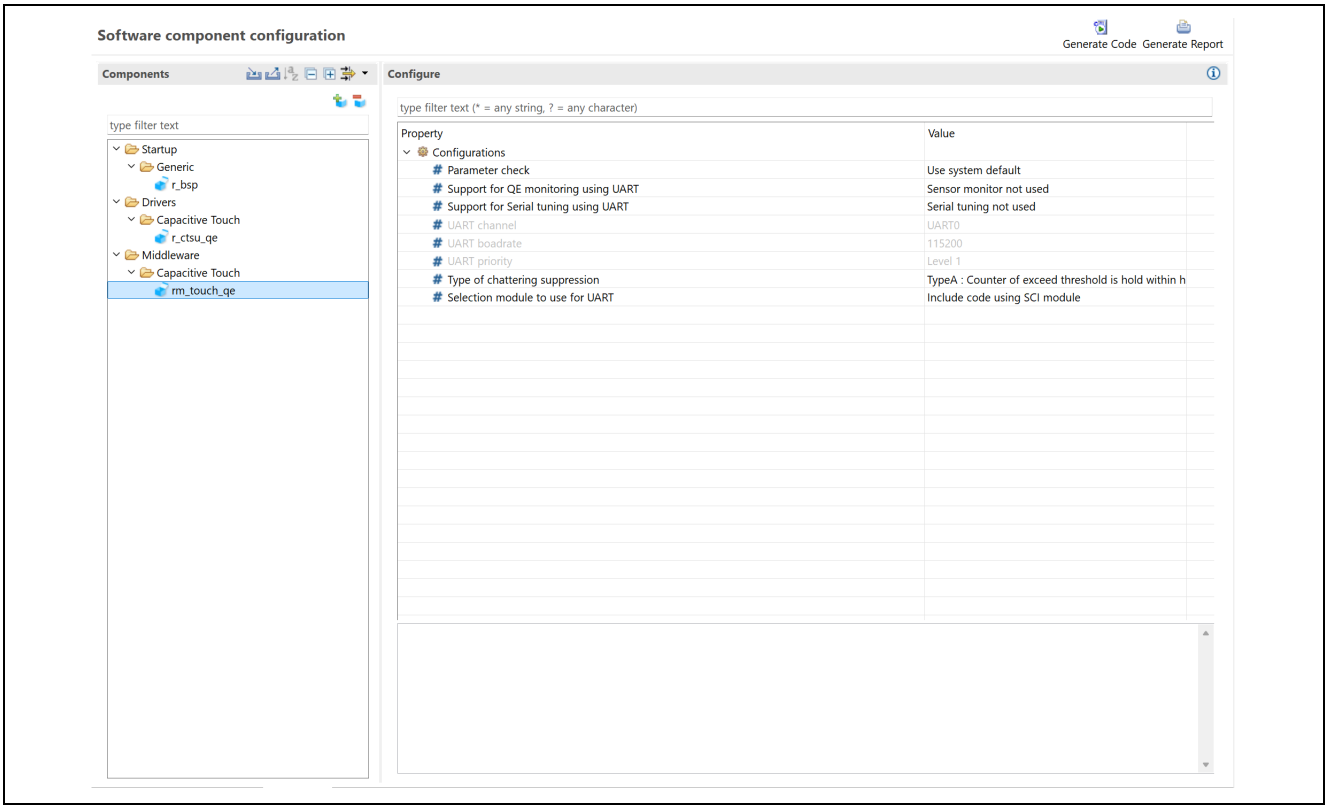

Figure 6-23 Smart Configurator (RX)

3. If you are using an MCU with CTSU2, the ADC drivers must be added. For the procedure to configure the ADC driver, refer to Step 4 to 11. If you are using an MCU with CTSU1, proceed to Step 5.

4. Add the ADC driver as shown in Figure 6-24. The ADC pins (ANxxx) do not need to be selected in this step.

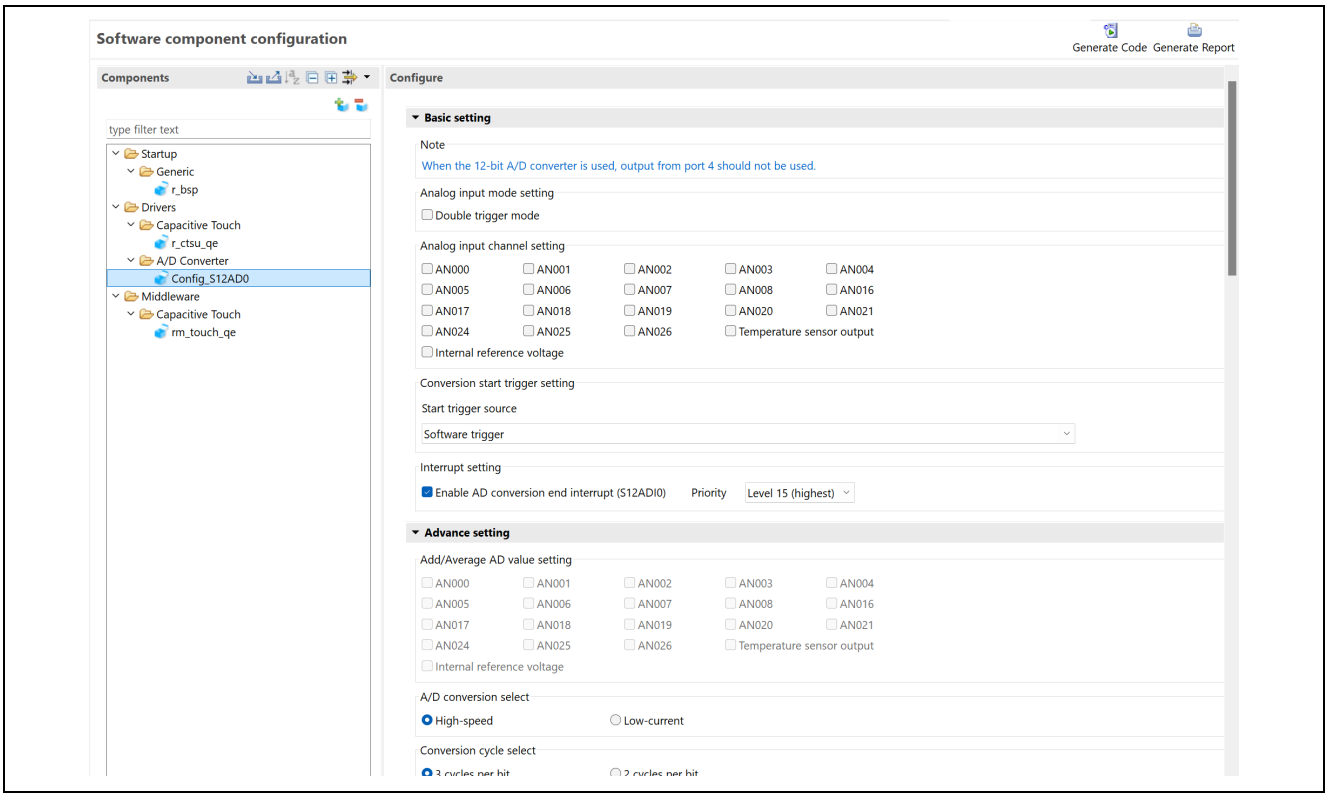

Figure 6-24 Add ADC Drover (RX)

5. Click [Generate Code] at the upper right of the Smart Configurator to generate code.

6. Using the QE for Capacitive Touch, implement the sample code following the same steps described in Section 6.1 RA Family, Steps 12 through 18.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.10.25	-	First edition issued
1.10	2023.3.31	-	Added target devices
1.20	2023.10.16	-	Added target devices
		5	Added diagnostic for CTSUb
		8	Revised for using corrected current values
		10	Revised for using corrected CTSU measurement values
		12	Added diagnostic for CTSUb
2.00	2026.5.27	-	Japanese edition issued
		-	Added target devices
		4	Updated description in Chapter 1
		5-23	Updated description and figures in Chapter 2
		24-56	Updated description on diagnostic function in Chapter 3
		57	Deleted previous description in Chapter 4 and added instructions to follow CTSU module APNs for each family
		57	Deleted previous description in Chapter 5 and added instructions to follow CTSU module APNs for each family
		57-80	Updated description in Chapter 6 to match QE for Capacitive Touch v4.3.0

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

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8. Differences between products

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