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H8SX Family

Buffered Compared-Match Operation of the TPU for Pulse Output

Introduction

Buffered operation of the output-compare function of the 16-bit TPU (Timer Pulse Unit) is used to drive toggling that produces output pulses with varying widths at the high and low levels.

Target Device

H8SX/1638 and 1653 Groups

Preface

Other than the target devices indicated above, the program covered in this application note can be run on H8SX devices that have the same I/O registers as those employed by the program. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the actual target device

Contents

1. Specifications

Figure 1 shows how the buffered operation of the TPU's output-compare function is used to drive output toggling that produces output pulses with varying widths at the high and low levels.

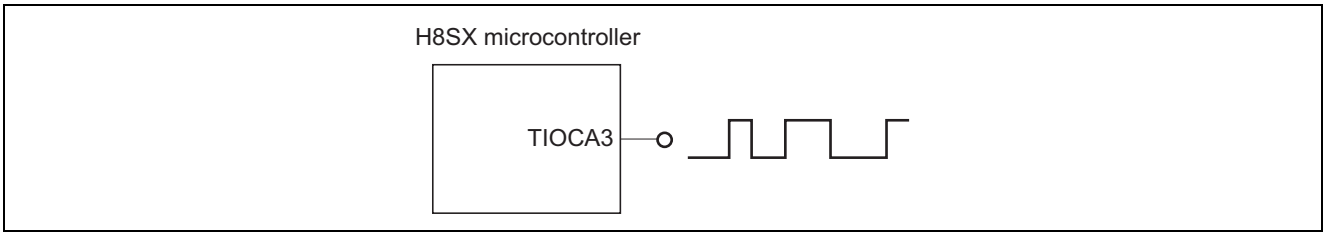


Figure 1 Pulse Output by Buffered Operation of the TPU's Compare Match

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Setting	
Operating frequency	Input clock	12 MHz
	System clock (Iϕ)	24 MHz (input clock frequency × 2)
	Peripheral module clock (Pϕ)	24 MHz (input clock frequency × 2)
	External bus clock (Bϕ)	24 MHz (input clock frequency × 2)
MD_CLK pin (H8SX/1653F)	MD_CLK = 0 Allowable input clock range: 8 to 18 MHz	
Operating mode	Mode 7 (single chip mode) Mode pin settings: MD2 = 1, MD1 = 1, MD0 = 1	

3. Principles of Operation

Figure 2 shows operation for pulse output by employing buffered compare-match operation of the TPU. TGRA is configured as an output-compare register and TGRA_3 and TGRC_3 are set up for buffered operation. On compare match A, TCNT_3 is cleared and the output on pin TIOCA3 is toggled.

As buffered operation has been set up, when a compare match A occurs, the output on pin TIOCA3 is toggled and the value in the buffer register (TGRC_3) is transferred to TGRA_3. This process is repeated on every compare-match A.

Table 2 describes details of the timing of operations (1) to (5) in figure 2. Consult figure 2 in conjunction with table 2.

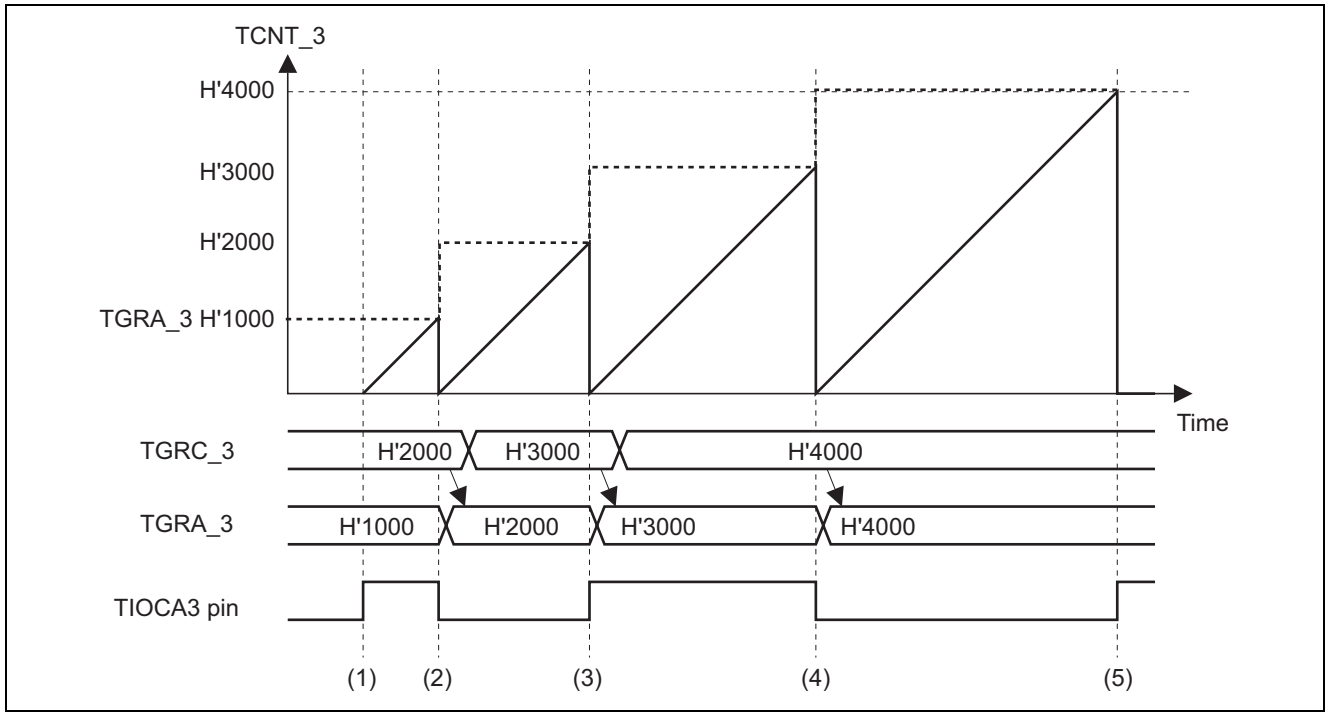


Figure 2 Timing of Pulse Output Operation

Table 2 Description of Processing

	Hardware processing	Software processing
(1)	Power-on reset	Initial setting (a) Set the TIOCA3 pin to output 1 initially. For other settings, see section 4, Description of Software.
(2)	Occurrence of compare match on TGRA_3 (a) Set TGFA in TSR_3 to 1. (b) Toggle output (to 0) on compare match with TGRA_3. (c) Transfer the value in TGRC_3 to TGRA_3.	TGI3A interrupts (a) Set data for transfer in TGRC_3. (b) Clear TGFA in TSR_3 to 0.
(3)	Occurrence of compare match on TGRA_3 (a) Set TGFA in TSR_3 to 1. (b) Toggle output (to 1) on compare match with TGRA_3. (c) Transfer the value in TGRC_3 to TGRA_3.	TGI3A interrupts (a) Set data for transfer in TGRC_3. (b) Clear TGFA in TSR_3 to 0.
(4)	Occurrence of compare match on TGRA_3 (a) Set TGFA in TSR_3 to 1. (b) Toggle output (to 0) on compare match with TGRA_3. (c) Transfer the value in TGRC_3 to TGRA_3.	TGI3A interrupts (a) Clear TGFA in TSR_3 to 0.
(5)	Occurrence of compare match on TGRA_3 (a) Set TGFA in TSR_3 to 1. (b) Toggle output (to 1) on compare match with TGRA_3. (c) Transfer the value in TGRC_3 to TGRA_3.	TGI3A interrupts (a) Disable the TIOCA3 pin output. (b) Disable the TGI3A interrupt. (c) Clear TGFA in TSR_3 to 0.

[Legend]
TIORH_3: Timer I/O control register H_3
TCNT_3: Timer counter_3
TGRA_3: Timer general register A_3
TGRC_3: Buffer register
TSR_3: Timer status register_3

4. Description of Software

4.1 Operating Environment

Table 3 Operating Environment

Item	Description
Development tool	High-performance Embedded Workshop Ver.4.03.00
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.02.00 (manufactured by Renesas Technology)
	Option settings: -cpu=h8sxa:24: md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver.9.03.00 (manufactured by Renesas Technology)
Linkage editor options	None

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	C	Area for constants
H'FF2000	B	Non-initialized data area (RAM area)

Table 5 Vector Table for Interrupt Exception Processing

Exception Processing Source		Vector No.	Address in Vector Table	Destination Interrupt-Processing Function
Reset		0	H'000000	init
TPU_3	TGI3A	101	H'000194	tgi3a_int

4.2 List of Functions

The functions in this sample task are shown in table 6. The hierarchy of calls in the user program is shown in figure 3.

Table 6 List of Functions

Function Name	Description
init	Initialization routine Releases the modules from module stop mode, configures the clocks, and calls the main function.
main	Main routine Configures TPU_3 for buffered operation of the output compare function, to drive toggling of the output on the TIOCA3 pin.
tgi3a_int	TGI3A interrupt exception processing Sets values in TGRC_3 (buffer register) and clears TGFA in TSR_3.

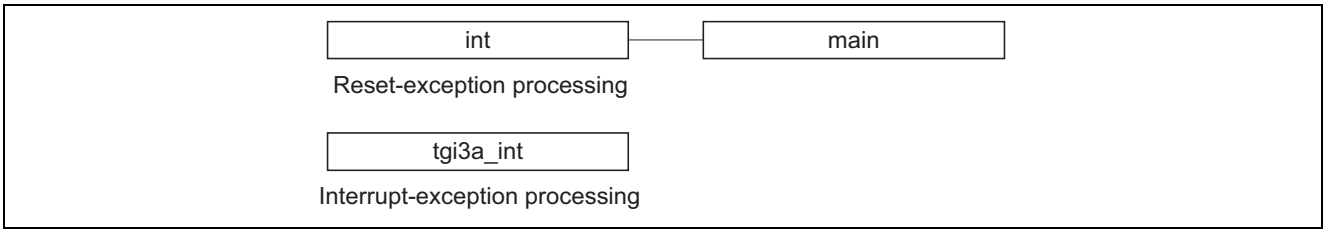


Figure 3 Hierarchy of Calls in the User Program

4.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in
unsigned char	cnt	Counter (1 byte)	main, tgi3a_int

4.4 Constant

Table 8 Constant

Type	Variable Name	Setting	Description	Used in
unsigned char	output[4]	H'1000, H'2000, H'3000, H'4000	Settings for TGRA_3	main, tgi3a_int

4.5 Description of Functions

4.5.1 init Function

1. Functional overview
   Initialization routine: this function releases the modules from module-stop mode, configures the clocks, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of employed internal registers of the H8SX/1638F
   The internal registers used in this sample task are described below. The settings shown in the tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	—*	R	Mode Select 3 to 0
10	MDS2	—*	R	These bits indicate the operating mode selected by the mode
9	MDS1	—*	R	pins (MD2 to MD0) (see table 9). When MDCR is read, the
8	MDS0	—*	R	signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset.

Note: * Determined by the settings on pins MD3 to MD0.

Table 9 Settings of Bits MDS3 to MDS0

MCU	Pins			MDCR			
Operating Mode	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
1	0	0	1	1	1	0	1
2	0	1	0	1	1	0	0
3	0	1	1	0	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to
8	ICK0	1	R/W	the CPU, DMAC, and DTC. 001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External-Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module-stop mode. Setting a bit to 1 makes the corresponding module enter the module-stop mode, while clearing the bit to 0 releases the module from module-stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current drawn by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode. 1: Enables all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timers (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timers (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPB15	1	R/W	Programmable pulse generator (PPG_0: PO15 to PO0)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communications interface_3 (SCI_3)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 2_1 (IIC2_1)
6	MSTPB6	1	R/W	I^2C bus interface 2_0 (IIC1_0)
5	MSTPB5	1	R/W	User break controller (USC)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timers (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timers (TMR_6 and TMR_7)
10	MSTPC10	1	R/W	Cyclic redundancy checker
9	MSTPC9	1	R/W	A/D converter (unit 1)
8	MSTPC8	1	R/W	Programmable pulse generator (PPG_1: PO31 to PO16)
7	MSTPC7	0	R/W	On-chip RAM_6 (H'FEE000 to H'FEFFFF)
6	MSTPC6	0	R/W	Always set the MSTPC7 and MSTPC6 bits to the same value.
5	MSTPC5	0	R/W	On-chip RAM_5, 4 (H'FF0000 to H'FF3FFF)
4	MSTPC4	0	R/W	Always set the MSTPC5 and MSTPC4 bits to the same value.
3	MSTPC3	0	R/W	On-chip RAM_3, 2 (H'FF4000 to H'FF7FFF)
2	MSTPC2	0	R/W	Always set the MSTPC3 and MSTPC2 bits to the same value.
1	MSTPC1	0	R/W	On-chip RAM_1, 0 (H'FF8000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always set the MSTPC1 and MSTPC0 bits to the same value.

5. Description of employed internal registers of the H8SX/1653F
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
11	MDS3	—*	R	Mode Select 3 to 0
10	MDS2	—*	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 10). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
9	MDS1	—*	R	
8	MDS0	—*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 10 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to the CPU, DMAC, and DTC.
8	ICK0	1	R/W	001: Input clcok × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clcok × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clcok × 2

- MSTPCRA, MSTPCRB, and MSTPCRC control module-stop mode. Setting a bit to 1 makes the corresponding module enter the module-stop mode, while clearing the bit to 0 releases the module from module-stop mode.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current drawn by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: Disables all-module-clock-stop mode. 1: Enables all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timers (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timers (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

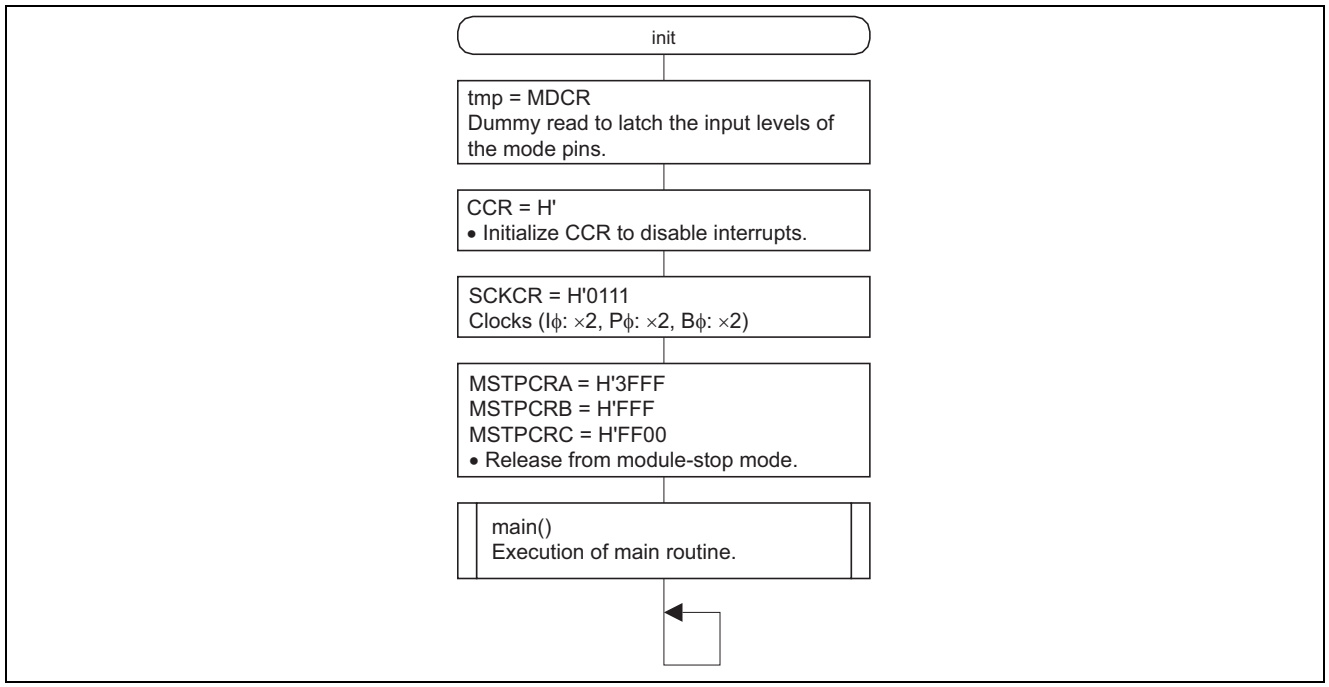
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timers (TMR_4 and TMR_5)
12	MSTPC12	1	R/W	8-bit timers (TMR_6 and TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy checker
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input levels of the mode pins.
CCR = H'
• Initialize CCR to disable interrupts.
SCKCR = H'0111
Clocks (Iϕ: ×2, Pϕ: ×2, Bϕ: ×2)
MSTPCRA = H'3FFF
MSTPCRB = H'FFF
MSTPCRC = H'FF00
• Release from module-stop mode.
main()
Execution of main routine.

4.5.2 main Function

1. Functional overview
   For the output-compare function of the TPU, the main routine selects buffered operation and toggling of the TIOCA3 pin output.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Timer control register_3 (TCR_3) Number of bits: 8 Address: H'FFFEC1

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	0	R/W	These bits select the TCNT_3 counter-clearing source.
5	CCLR0	1	R/W	001: TCNT_3 is cleared to 0 by TGRA_3-compare match/input capture.
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. 00: Counting of falling edges
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	Selects the TCNT_3 counter clock.
0	TPSC0	0	R/W	000: Counting of internal clock (Pϕ/1) cycles

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	0	R/W	These bits select operation or stoppage for TCNT.
3	CST3	1	R/W	0: Counting by TCNT_n is stopped.
2	CST2	0	R/W	1: Counting by TCNT_n proceeds.
1	CST1	0	R/W	
0	CST0	0	R/W	

- Timer mode register_3 (TMDR_3) Number of bits: 8 Address: H'FFFFF1

Bit	Bit Name	Setting	R/W	Description
4	BFA	1	R/W	Buffer Operation A 0: TGRA operates normally. 1: TGRA and TGRC are used together in buffered operation.
3	MD3	0	R/W	Mode 3 to 0
2	MD2	0	R/W	These bits set the timer's operating mode.
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer I/O control register H_3 (TIORH_3) Number of bits: 8 Address: H'FFFFF2

Bit	Bit Name	Setting	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	1	R/W	These bits specify the function of TGRA_3.
1	IOA1	1	R/W	0111: TGRA_3 functions as an output compare register.
0	IOA0	1	R/W	The initial output on TIOCA3 is 1, and the level is toggled on each compare match.

- Timer interrupt enable register_3 (TIER_3) Number of bits: 8 Address: H'FFFFF4

Bit	Bit Name	Setting	R/W	Description
0	TGIEA	1	R/W	TGR Interrupt Enable A This bit enables or disables generation of interrupt requests (TGIA) by setting of the TGFA bit. 0: Generation of interrupt requests (TGIA) by the TGFA bit is disabled. 1: Generation of interrupt requests (TGIA) by the TGFA bit is enabled.

- Timer status regsiter_0 (TSR_0) Number of bits: 8 Address: H'FFFFF5

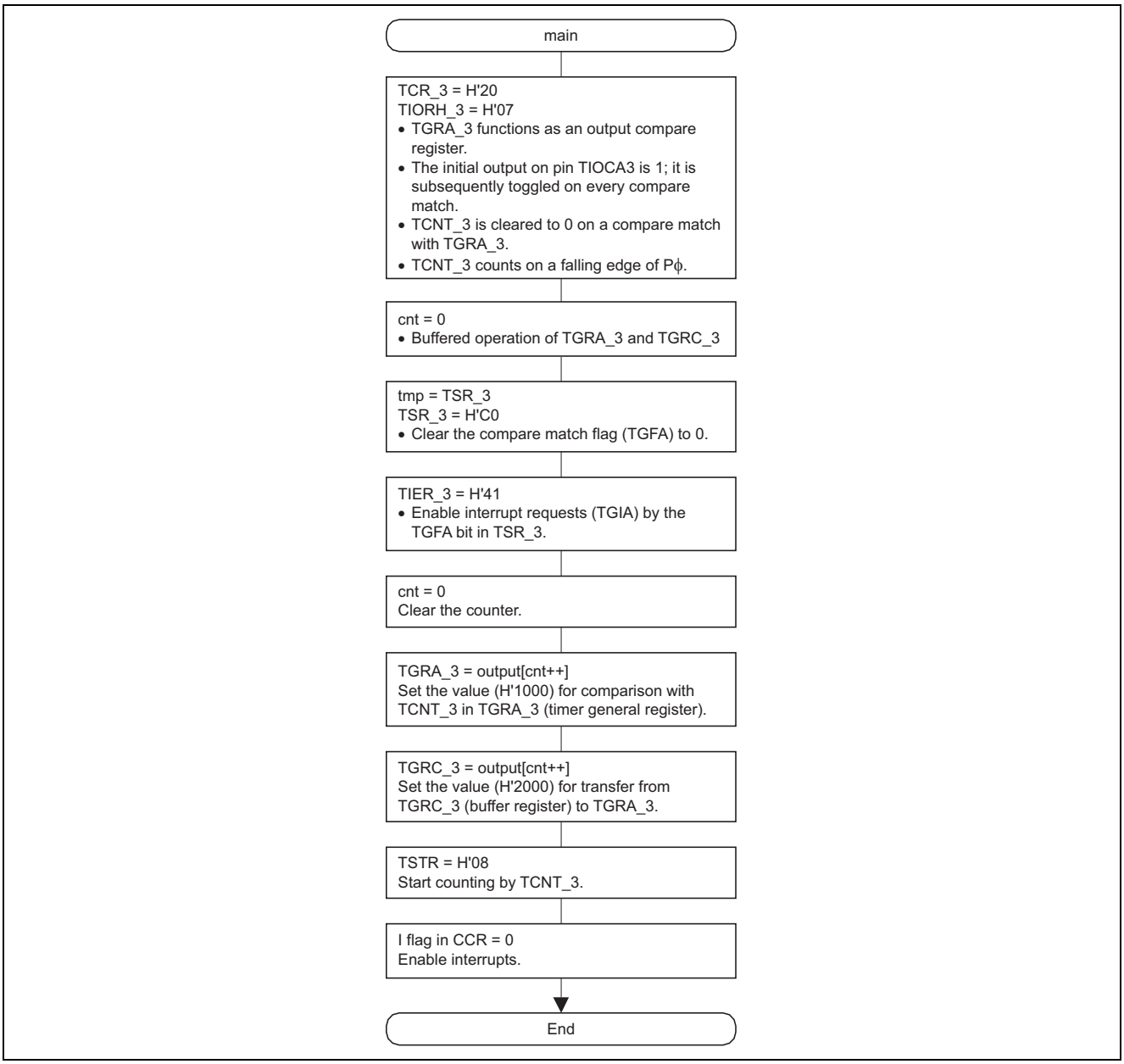
Bit	Bit Name	Setting	R/W	Description
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_3 is functioning as an output-compare register, the following conditions apply. [Setting condition] TCNT_3=TGRA_3 [Clearing condition] Writing 0 to TGFA after having read TGFA as 1

Note: * Only 0 can be written here, to clear the flag.

- Timer general register A_3 (TGRA_3) Number of bits: 16 Address: H'FFFFF8
  Function: TGRA_3 is used as an output-compare register in this application.
  Setting: output[cnt++] (=H'1000)

- Timer general register C_3 (TGRC_3) Number of bits: 16 Address: H'FFFFFC
  Function: TGRC_3 is used as a buffer register for TGRA_3 in this application.
  Setting: output[cnt++] (=H'2000)

5. Flowchart


main
TCR_3 = H'20
TIORH_3 = H'07
• TGRA_3 functions as an output compare register.
• The initial output on pin TIOCA3 is 1; it is subsequently toggled on every compare match.
• TCNT_3 is cleared to 0 on a compare match with TGRA_3.
• TCNT_3 counts on a falling edge of Pϕ.
cnt = 0
• Buffered operation of TGRA_3 and TGRC_3
tmp = TSR_3
TSR_3 = H'C0
• Clear the compare match flag (TGFA) to 0.
TIER_3 = H'41
• Enable interrupt requests (TGIA) by the TGFA bit in TSR_3.
cnt = 0
Clear the counter.
TGRA_3 = output[cnt++]
Set the value (H'1000) for comparison with TCNT_3 in TGRA_3 (timer general register).
TGRC_3 = output[cnt++]
Set the value (H'2000) for transfer from TGRC_3 (buffer register) to TGRA_3.
TSTR = H'08
Start counting by TCNT_3.
I flag in CCR = 0
Enable interrupts.
End

4.5.3 tgi3a_int Function

1. Functional overview
   Interrupt processing for TGI3A. tgi3a_int sets values in TGRC_3 (the buffer register) and clears TGFA in TSR_3.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Timer I/O control register H_3 (TIORH_3) Number of bits: 8 Address: H'FFFFF2

Bit	Bit Name	Setting	R/W	Description
3	IOA3	0	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	These bits specify the function of TGRA_0.
1	IOA1	0	R/W	0000: TGRA_3 functions as an output-compare register.
0	IOA0	0	R/W	Output on pin TIOCA3 is disabled.

- Timer interrupt enable register_3 (TIER_3) Number of bits: 8 Address: H'FFFFF4

Bit	Bit Name	Setting	R/W	Description
0	TGIEA	0	R/W	TGR Interrupt Enable A This bit enables or disables generation of interrupt requests (TGIA) by setting of the TGFA bit. 0: Generation of interrupt requests (TGIA) by the TGFA bit is disabled. 1: Generation of interrupt requests (TGIA) by the TGFA bit is enabled.

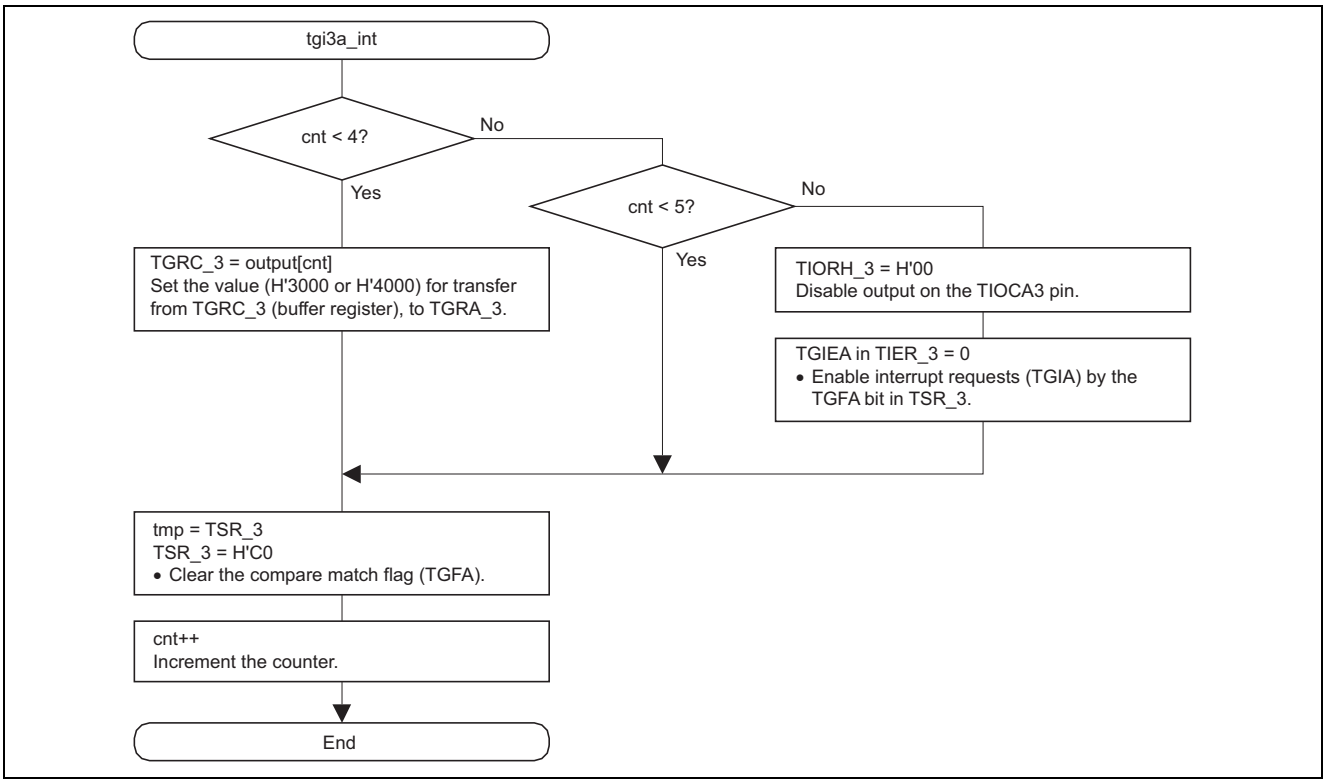
- Timer status register_3 (TSR_3) Number of bits: 8 Address: H'FFFFF5

Bit	Bit Name	Setting	R/W	Description
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_3 is functioning as an output-compare register, the following conditions apply. [Setting condition] TCNT_3=TGRA_3 [Clearing condition] Writing 0 to TGFA after having read TGFA as 1

Note: * Only 0 can be written here, to clear the flag.

- Timer general register C_3 (TGRC_3) Number of bits: 16 Address: H'FFFFFC
  Function: TGRC_3 is used as a buffer register for TGRA_3 in this application.
  Setting: output[cnt] (=H'3000 or H'4000)

5. Flowchart


tgi3a_int
cnt < 4?
No
Yes
cnt < 5?
No
Yes
TGRC_3 = output[cnt]
Set the value (H'3000 or H'4000) for transfer from TGRC_3 (buffer register), to TGRA_3.
TIORH_3 = H'00
Disable output on the TIOCA3 pin.
TGIEA in TIER_3 = 0
• Enable interrupt requests (TGIA) by the TGFA bit in TSR_3.
tmp = TSR_3
TSR_3 = H'C0
• Clear the compare match flag (TGFA).
cnt++
Increment the counter.
End

5. Documents for Reference

- Hardware Manual
  H8SX/1638 Group Hardware Manual
  H8SX/1653 Group Hardware Manual
  The most up-to-date versions of these documents are available on the Renesas Technology Website.

- Technical News/Technical Update
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