Bench-Testing Important DC-Parameters of Operational Amplifiers

Today many engineers rely on Spice models when assessing the performance of operational amplifiers (op-amps). If you suspect a Spice model to be inaccurate or lacking certain parameters, you can build your own op-amp test system and still determine the key device parameters.

This application note discusses a universal test circuit that allows you to measure the key DC parameters of an op-amp on your lab workbench.

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1. DC Parameters

The test circuit in Figure 1 enables you to measure the key DC parameters of an op-amp Device Under Test (DUT) with the help of an auxiliary amplifier (AUX) in a servo-loop configuration.

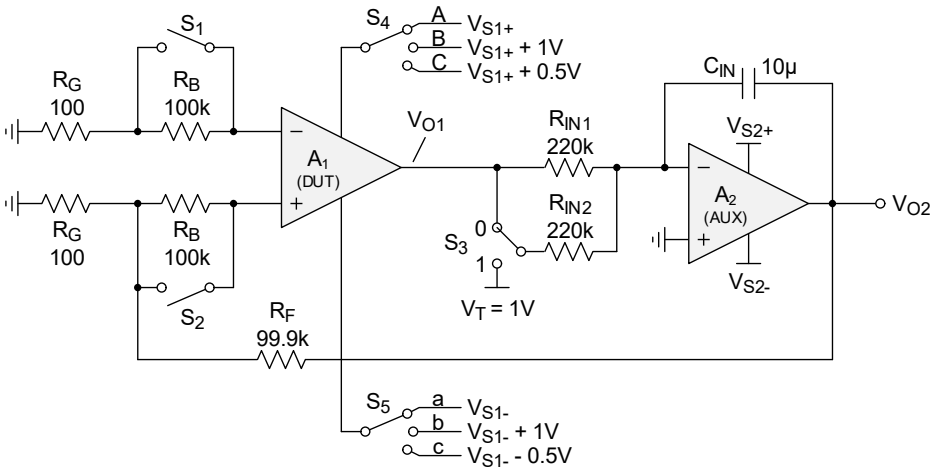

Figure 1. Test Circuit for Measuring Key DC Parameters of Op-Amps

The various DC parameters measurable with this circuit and their corresponding switch positions are listed in Table 1.

Table 1. Switch Positions for Measuring the Key DC Parameters of an Op-Amp

Parameter Measurements		Switch Positions[1]				
		S_1	S_2	S_3	S_4	S_5
DC (Output = TP1)	V_{OS}	1	1	0	A	a
	I_{B-}	0	1	0	A	a
	I_{B+}	1	0	0	A	a
	A_{OL}	1	1	1	A	a
	CMRR	1	1	0	B	b
	PSRR	1	1	0	C	c

1. For S_1, S_2, S_3: 1 = closed, 0 = open

The circuit uses dual supplies but works well for both single-supply and dual-supply op-amps. It basically amplifies the input error voltages of the DUT and makes them available at the output of the AUX amplifier.

For the DUT, apply the nominal supply voltage in dual supply fashion, even for a single-supply op-amp. For example, in the case of a 3.3V single supply op-amp, make V_{S1} = ±1.65V.

For the AUX amplifier, select an op-amp with large dual supply rails of ±12V to ±20V to obtain a wide dynamic output voltage range at V_{O2}. The AUX amplifier does not need to be a precision amplifier but can be a general-purpose op-amp because the impact of its input errors on the measurement accuracy are negligible. This is explained in section Input Errors of the AUX Op-Amp are Negligible.

1.1 Servo-Loop Operating Principle

The operation of the servo or negative feedback loop is shown in Figure 2. Here, the DUT operates at open-loop gain. For better understanding, we can separate the DUT into an ideal op-amp with the external input DC error voltage, V_E. At t = 0, V_E is amplified by the high DC open-loop gain of the DUT; therefore, driving the output voltage (V_{O1}) to one of the supply rails, in this case the positive rail (V_{S1+}). This abrupt rise of V_{O1} is converted into gradually declining, negative output voltage, V_{O2}, by the integrator. V_{O2} is attenuated by the R_F-R_G voltage divider and fed back to the positive input of the DUT as feedback voltage (V_{FB}): $V_{FB} = V_{FB} \times \beta$. As the feedback factor is the reciprocal of the circuit gain, $\beta = 1/G$, we can also write: $V_{FB} = V_{O2}/G$.

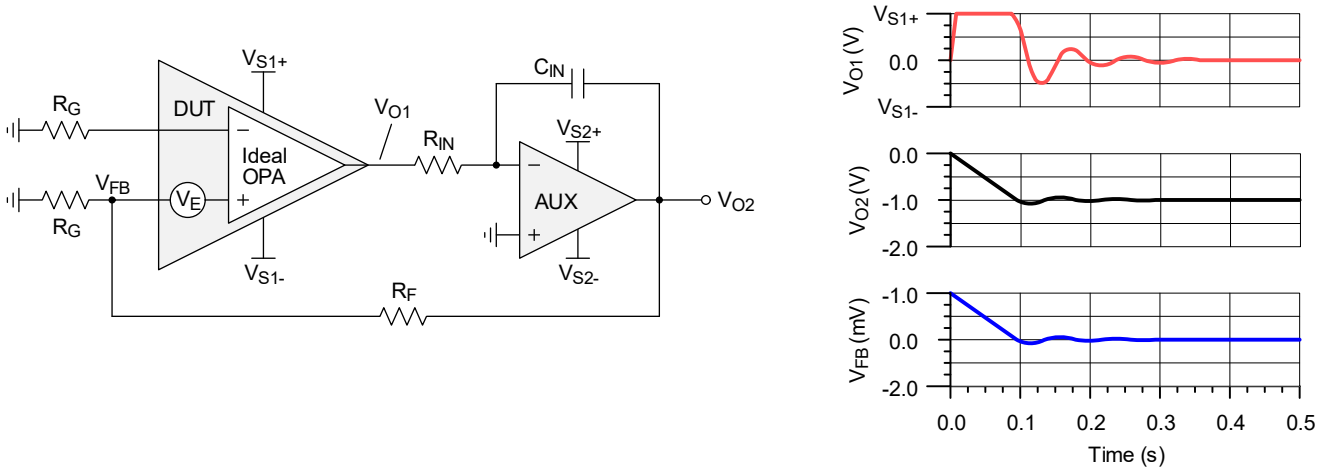

Figure 2. Servo-Loop Operation

With V_{FB} having the opposite polarity of V_E, the sum, $V_E + V_{FB}$, results in a smaller negative V_{O1}. This causes the integrator to integrate towards a smaller positive V_{O2}.

This regulating process continues until V_{O1} equals the positive input of the AUX amplifier, which is 0V. At that point, the current into the integrator is zero, the integration stops, and V_O remains constant. If V_{O1} = 0V, the total input error must be also zero volt: $V_{FB} + V_E$ = 0V, which requires that $V_E = -V_{FB}$.

To express the input error through the output voltage, we can substitute V_{FB} with $V_{FB} = V_{O2}/G$ and receive $V_E = -V_{O2}/G$. This means that the input error voltage is the measured inverted output voltage, divided by the circuit gain.

1.2 Input Errors of the AUX Op-Amp are Negligible

Figure 3 depicts the simplified test circuit in the steady state, when V_{O2} has stabilized and remains constant. In this state, C_{IN} is fully charged and high-impedance and no current flows through R_{IN}. Therefore, both components can be omitted, indicating that A_2 operates at open-loop gain. The input errors of each op-amp are consolidated in the error voltages, V_{E1} and V_{E2}.

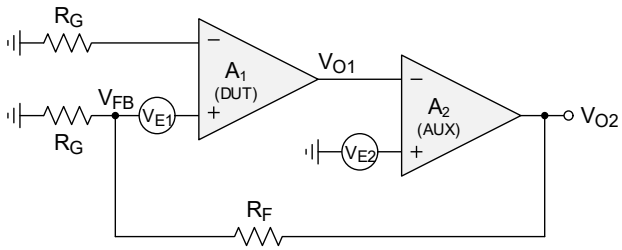

Figure 3. Test Circuit with Input Error Voltages, V_{E1} and V_{E2}

To determine the impact of V_{E2} on the circuit output voltage, we establish the equation for V_{O2} with:

(EQ. 1) $$V_{O2} = A_2(V_{E2} - V_{O1})$$

The output voltage of A_1 is derived in the same way:

(EQ. 2) $$V_{O1} = A_1(V_{E1} + V_{FB} - 0) = A_1(V_{E1} + V_{FB})$$

As mentioned earlier, the feedback voltage equals the output voltage divided by the circuit gain:

(EQ. 3) $$V_{FB} = V_{O2}/G \quad \text{with} \quad G = 1 + R_F/R_G$$

Then, inserting Equation 2 and Equation 3 into Equation 1 and solving for V_{O2} gives:

(EQ. 4) $$V_{O2} = -G \times (V_{E1} - V_{E2}/A_1)$$

Equation 4 shows that the input errors of A_2 are suppressed by the high DC open-loop gain of A_1, which reduces the error contribution of A_2 to zero: $V_{E2}/A_1 \approx 0$. Therefore, the output voltage solely represents the input error of A_1 amplified by the circuit gain:

(EQ. 5) $$V_{O2} = -V_{E1} \times G$$

1.3 Input Offset Voltage, V_{OS}, Measurement

Figure 4 shows the equivalent test circuit for measuring V_{OS} of A_1. Here, the switches S_1 and S_2 are closed, shunting the input bias resistors R_B. The input bias currents still flow through the gain resistors, R_G, but their voltages across these resistors are much smaller than V_{OS} and therefore, can be ignored.

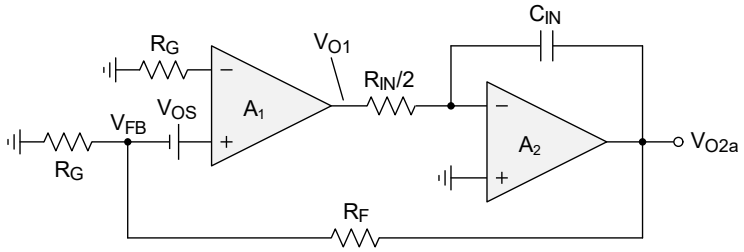

Figure 4. Equivalent DC Test Circuit for measuring V_{OS}

Because the steady state of V_{O2} is reached when V_{O1} is zero, we can write the equation for V_{O1} as:

(EQ. 6) $$V_{O1} = 0 = A_1(V_{OS} + V_{FB} - 0)$$

With $V_{FB} = V_{O2}/G$, solving for V_{OS} yields $V_{OS} = -V_{O2}/G$.

Because V_{O2} is going to change for each parametric measurement, we distinguish between the various V_{O2} values through indices. In the case of the V_{OS} measurement, we denote the output voltage as V_{O2a}:

(EQ. 7) $$V_{OS} = 0 = \frac{V_{O2a}}{G}$$

1.4 Negative Input Bias Current, I_{B-}, Measurement

To measure I_{B-}, switch S_1 is opened and S_2 remains closed. This inserts a large bias resistor, $R_B >> R_G$, into the inverting input path, causing V_{O2} to change from V_{O2a} to V_{O2b}.

The equation for V_{O1} now includes the large voltage drop across R_B due to I_{B-}:

(EQ. 8) $$V_{O1} = 0 = V_{OS} + V_{FB} - I_{B-} \times R_B = V_{OS} + \frac{V_{O2b}}{G} - I_{B-} \times R_B$$

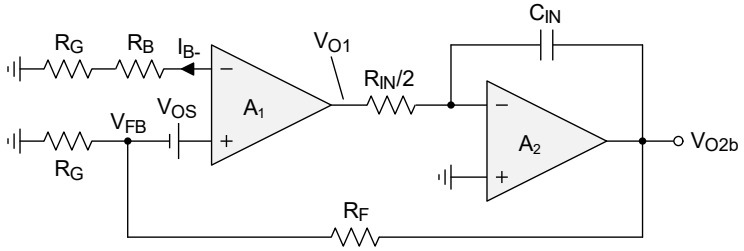

Figure 5. Inserting R_B into the inverting Input Path to measure I_{B-}

Then, solving for I_{B-} yields: $I_{B-} = \frac{1}{R_B}\left(V_{OS} + \frac{V_{O2b}}{G}\right)$, and substituting V_{OS} with the term in Equation 7 gives:

(EQ. 9) $$I_{B-} = \frac{1}{R_B}\left(\frac{V_{O2b} - V_{O2a}}{G}\right)$$

1.5 Positive Input Bias Current, I_{B+}, Measurement

To measure I_{B+}, switch S_2 is opened and S_1 is closed. This inserts a large bias resistor, R_B, into the non-inverting input path, causing V_{O2} to change from V_{O2a} to V_{O2c}.

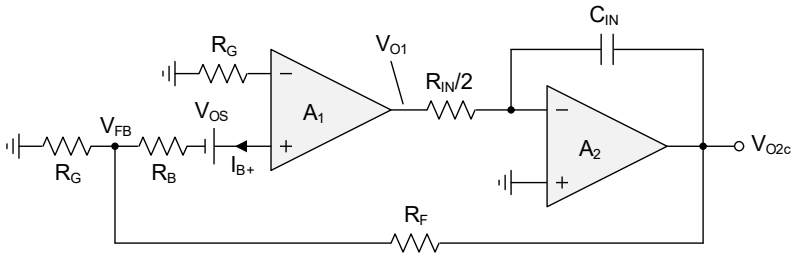

Figure 6. Inserting R_B into the Non-Inverting Input Path to Measure I_{B+}

The equation for V_{O1} now includes the large voltage drop across R_B due to I_{B+}:

(EQ. 10) $$V_{O1} = 0 = V_{OS} + V_{FB} = V_{OS} + I_{B+} \times R_B + \frac{V_{O2c}}{G}$$

Then, solving for I_{B+} yields: $I_{B+} = -\frac{1}{R_B}\left(V_{OS} + \frac{V_{O2c}}{G}\right)$, and substituting V_{OS} with the term in Equation 7 gives:

(EQ. 11) $$I_{B+} = \frac{1}{R_B}\left(\frac{V_{O2a} - V_{O2c}}{G}\right)$$

Note: For op-amps with high bias currents, the output of A_2 can saturate. In this case, reduce the value of R_B (typically by a factor of 10) until the output of A_2 stays within the supply rails.

1.6 DC Open-Loop Gain, $A_{OL(DC)}$, Measurement

To measure the DC open-loop gain, switches S_1 and S_1 are closed, and S_3 connects R_{IN2} to the test voltage, V_T (Figure 7). Now, V_{O2} reaches the steady state when $V_{O1} = -V_T$ and no charge current flows.

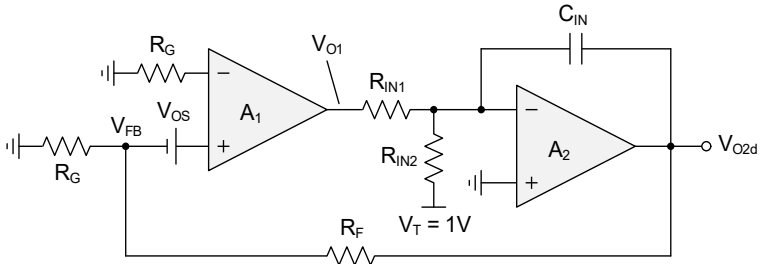

Figure 7. Applying a Test Voltage, V_T, to Measure A_1 at DC

Except for V_T, the circuit is identical to the one, measuring V_{OS}. Therefore, we can apply Equation 6 with the modification that $V_{O1} = -V_T$ and V_{O2} changes from V_{O2a} to V_{O2d}.

(EQ. 12) $$V_{O1} = -V_T = A(V_{OS} + V_{FB}) = A_1\left(V_{OS} + \frac{V_{O2d}}{G}\right)$$

Then solving for A_1 gives: $A_1 = \frac{-V_T}{V_{OS} + \frac{V_{O2d}}{G}}$ and substituting V_{OS} with the term in Equation 7 yields:

(EQ. 13) $$A_1 = \frac{V_T \times G}{V_{O2a} - V_{O2d}}$$

Note: Making V_T = 1V, reduces Equation 13 to:

(EQ. 14) $$A_1 = \frac{G}{V_{O2a} - V_{O2d}}$$

1.7 DC Common-Mode Rejection Ratio, $CMRR_{(DC)}$, Measurement

The common-mode rejection ratio (CMRR) of an op-amp is the ratio of the applied change in common-mode voltage to the change in offset voltage (due to a change in common-mode voltage):

(EQ. 15) $$CMRR = \frac{A_{DM}}{A_{CM}} = \frac{\Delta V_O / \Delta V_{OS}}{\Delta V_O / \Delta V_{CM}} = \frac{\Delta V_{CM}}{\Delta V_{OS}}$$

In the circuit of Figure 8, the common-mode voltage is not applied to the input terminals of A_1, where low-level effects could disrupt the measurement, but to the power-supply voltages instead. Here, both supply rails are altered in the same (common) direction by ΔV_{CM} = +1V, relative to the input.

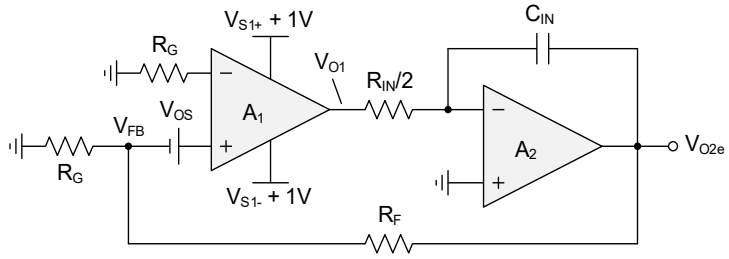

Figure 8. Changing A_1 Supply Voltages in a Common Direction to Measure CMRR at DC

The input offset voltage at V_{S1+} and V_{S1-} is given in Equation 7 with $V_{OS} = -V_{O2a}/G$. A change in input offset because of a common-mode change of V_{S1} can therefore be expressed through $V_{OS(CM)} = -V_{O2e}/G$. This makes ΔV_{OS}:

(EQ. 16) $$\Delta V_{OS} = V_{OS} - V_{OS(CM)} = \frac{V_{O2e} - V_{O2a}}{G}$$

Then, inserting Equation 15 into Equation 14 gives the common-mode rejection ratio:

(EQ. 17) $$CMRR_{(DC)} = \frac{G \times \Delta V_{CM}}{V_{O2e} - V_{O2a}}$$

Note: Making ΔV_{CM} = +1V, reduces Equation 17 to:

(EQ. 18) $$CMRR_{(DC)} = \frac{G}{V_{O2e} - V_{O2a}}$$

1.8 DC Power Supply Rejection Ratio, $PSRR_{(DC)}$, Measurement

The power supply rejection ratio (PSRR) of an op-amp is the ratio of a change in supply voltage to the change in offset voltage.

(EQ. 19) $$PSRR = \frac{\Delta V_S}{\Delta V_{OS}}$$

In the circuit of Figure 9, the positive rail is increased by 0.5V and the negative rail is decreased by -0.5V, therefore, resulting in a total supply change of ΔV_{S1} = +1V.

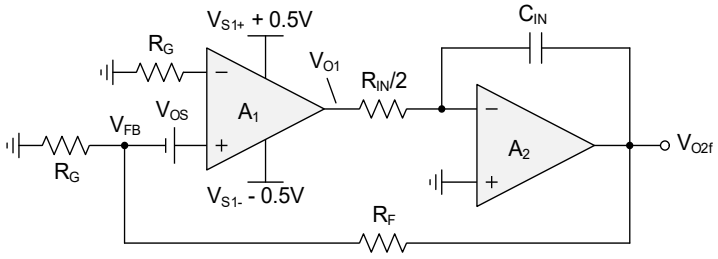

Figure 9. Changing A_1 total Supply Voltage to Measure PSRR at DC

Again, the input offset voltage at V_{S1+} and V_{S1-} is $V_{OS} = -V_{O2a}/G$, and the input offset voltage due to the change in total supply by ΔV_{S1} is $V_{OS(PS)} = -V_{O2f}/G$. This makes ΔV_{OS}:

(EQ. 20) $$\Delta V_{OS} = V_{OS} - V_{OS(PS)} = \frac{V_{O2f} - V_{O2a}}{G}$$

Then, inserting Equation 20 into Equation 19 gives the power supply rejection ratio:

(EQ. 21) $$PSRR_{(DC)} = \frac{G \times \Delta V_{S1}}{V_{O2f} - V_{O2a}}$$

Note: Making ΔV_S = +1V, reduces Equation 21 to:

(EQ. 22) $$PSRR_{(DC)} = \frac{G}{V_{O2f} - V_{O2a}}$$

1.9 Measurement Results for the Dual Op-Amp ISL28325

As a final check, the discussed DC parameters of the dual op-amp, ISL28325, were measured with the test circuit in Figure 10. Table 2 lists the measured results and the calculated parameters in comparison with the corresponding datasheet values.

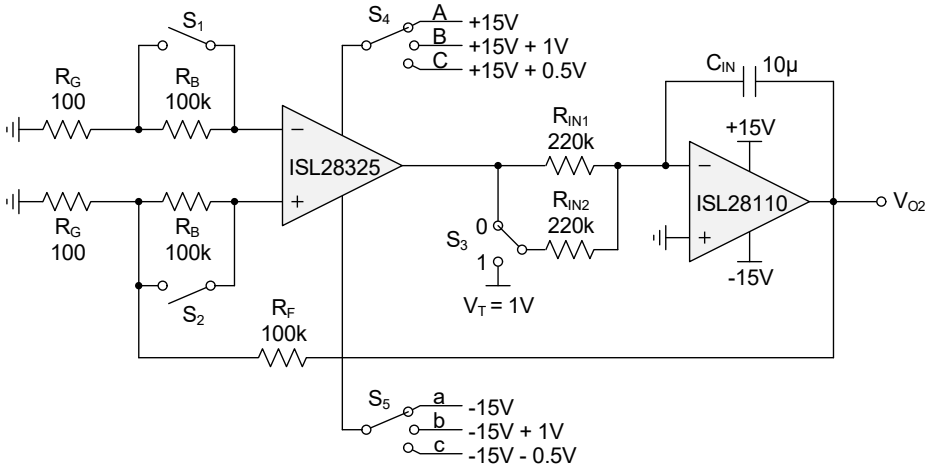

Figure 10. DC-Test Circuit for Dual Op-Amp ISL28325

Table 2. DC-Test Circuit for Dual Op-Amp ISL28325

Measured V_{O2}		Equations Applied	Calculated Parameter		Datasheet Value
V_{O2a}	-0.0188	$V_{OS} = -V_{O2a}/G$	V_{OS}	0.019mV	0.1mV (typical)
V_{O2b}	-0.0168	$I_{B-} = (V_{O2b} - V_{O2a})/R_B/G$	I_{B-}	0.020nA	0.2nA (typical)
V_{O2c}	-0.0183	$I_{B+} = (V_{O2a} - V_{O2c})/R_B/G$	I_{B+}	-0.005nA	0.2nA (typical)
V_{O2d}	-0.0179	$A_1 = G/(V_{O2a} - V_{O2d})$	$A_{OL(DC)}$	120.8dB	110dB (typical)
V_{O2e}	-0.0174	$CMRR_{(DC)} = G/(V_{O2e} - V_{O2a})$	$CMRR_{(DC)}$	117.0dB	80dB (minimum)
V_{O2f}	-0.0177	$PSRR_{(DC)} = G/(V_{O2f} - V_{O2a})$	$PSRR_{(DC)}$	118.5dB	80dB (minimum)

2. Revision History

Revision	Date	Description
1.01	Jan 27, 2026	Updated Table 2.
1.00	Nov 16, 2022	Initial release.

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