Application Note

Atmel SAMA5D3 Power Management with DA9061/2

AN-PM-067

Abstract

The Dialog DA9061 and DA9062 provide cost-effective power management for the Atmel® SMART SAMADx series of microprocessors. This application note describes the SAMA5D3 and DA9061 interface based on the Atmel SAMA5D3 Xplained Evaluation Kit.

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1 Terms and Definitions

DVC	Dynamic Voltage Control
MPU	Microprocessor Unit
OTP	One-Time Programmable (memory)
PFM	Pulse Frequency Modulation
PMIC	Power Management Integrated Circuit
SAM	SMART Atmel Microcontroller

2 References

[1] DA9062, Datasheet, Dialog Semiconductor

[2] DA9061, Datasheet, Dialog Semiconductor

[3] 'SAMA5D3 Series', Atmel-11121E-ATARM-SAMA5D3-Series-Datasheet_02-Feb-15, Atmel

[4] SAMA5D3 Xplained User Guide, Atmel-11269C-ATARM-SAMA5D3-Xplained-XPLD-User Guide_03-Oct-14, Atmel

3 Introduction

The Dialog DA9061 and DA9062 provide cost-effective power management of the Atmel SMART SAMA5D3 series of MPUs. Benefits of the Dialog PMIC solutions include:

- Provides the lowest power consumption in all system operation modes
- Improved regulator efficiencies
- Integrated internal and external safety features such as die temperature supervision, voltage supervision and watchdog
- High buck switching frequency enables low profile (mostly ≤1 mm), ultra-small external components
- Flexible power rail sequencing adaptable to any application

This document describes the interconnections required and the power supply sequence. The PMIC configuration was evaluated using an Atmel SAMA5D3 Xplained Evaluation Kit.

4 Atmel SAMA5D3 Power Requirements

For reliable operation, the SAMA5D3 processors require precise power management of the system supplies as listed in Table 1.

Table 1: Power requirements of the SAMA5D3 and Xplained Evaluation Kit

System Rail	Range /V	Nominal /V	Current /A
VDDCORE	1.10-1.32	1.2	0.35
VDDIODDR (DDR2)	1.70–1.90	1.8	0.05
VDDIODDR (LPDDR2)	1.14–1.32	1.2	0.03
VDDIOM	1.65–1.95	1.8	0.03
VDDIOM	3.00–3.60	3.3	0.03
VDDIOP	1.65–3.60	3.3	0.03
VDDANA	3.00–3.60	3.3	-
VDDFUSE	2.25–2.75	2.5	0.05

5 Interconnections Between DA9061/2 and SAMA5D3

The DA9061 has sufficient regulators for powering the SAMA5D3 Xplained Evaluation Kit. A recommended mapping is shown in Table 2. The evaluation kit is configured with several system rails driven from a single PMIC regulator. For example, VDDCORE, VDDPLLA, and VDDUTMIC are tied together. The DA9062 can be used instead of the DA9061 where a system requires additional power rails. Compared with the DA9061, the DA9062 has an extra buck converter, dual-phase buck capability, DDR VTT supply capability, real-time clock and coin cell charger.

The sequence shown in Table 2 retains the default used by the Xplained Evaluation Kit and meets the requirements of the MPU in that VDDCORE, VDDUTMIC and VDDPLLA must power up ≥1 ms after other rails. To meet the requirements of the SAMA5D3 datasheet, the DA9061/2 nRESET line is released ≥1 ms after all rails have reached their target voltage. The completed sequence is shown in Figure 2, with nRESET being released on the edge coincident with POWER_END. The GPIO0(WKUP)_RISE and _FALL generates an MPU wake-up pulse.

Table 2: Mapping of DA9061/2 to SAMA5D3 Xplained Evaluation Kit Supplies

System Rail	Nominal voltage /V	Power-up sequence	DA9062 regulator	DA9061 regulator
VDDCORE, VDDPLLA, VDDUTMIC	1.2	3	Buck 1	Buck 1
VDDIODDR (DDR2) (Note 1)	1.8	2	Buck 4	Buck 3
VDDIOM (Note 2)	3.3	1	Buck 3	Buck 2
VDDIOP0, VDDIOP1, VDDUTMII	3.3	1	Buck 3	Buck 2
VDDANA	3.3	not sequenced (software controlled)	LDO2	LDO2
VDDFUSE	2.5	not sequenced (software controlled)	LDO3	LDO3

Note 1 VDDIODDR = 1.2 V for LPDDR2

Note 2 VDDIOM can optionally be 1.8 V when driven from a separate DA9061/2 regulator.

The SAMA5D3 Xplained Evaluation Kit was used as a reference design for signal mapping between MPU and PMIC. Suggested interconnects are provided in Table 3 and illustrated in Figure 1.

Table 3: Xplained Evaluation Kit Signal Mapping to DA9061/2

Evaluation Kit System Line	DA9061/2 line
5V_MAIN	VSYS
NRST	nRESET (O/P - open drain)
PC31	nIRQ (O/P - open drain)
SHDN	nRESETREQ (level triggered)
WKUP (nPBSTAT)	GPIO0 (GPO; push-pull; sequenced low-high when powering-up to ACTIVE state)
SDA	SDA
SCL	SCL
nPBPIN	nONKEY (configured with short debounce to ensure the wakeup FET input works): Requires addition of pull-up to VSYS.
-	VDDIO (Note 3)

Note 3 VDDIO can be supplied from DA9061 Buck 2 at 3.3 V (DA9062 Buck 3).

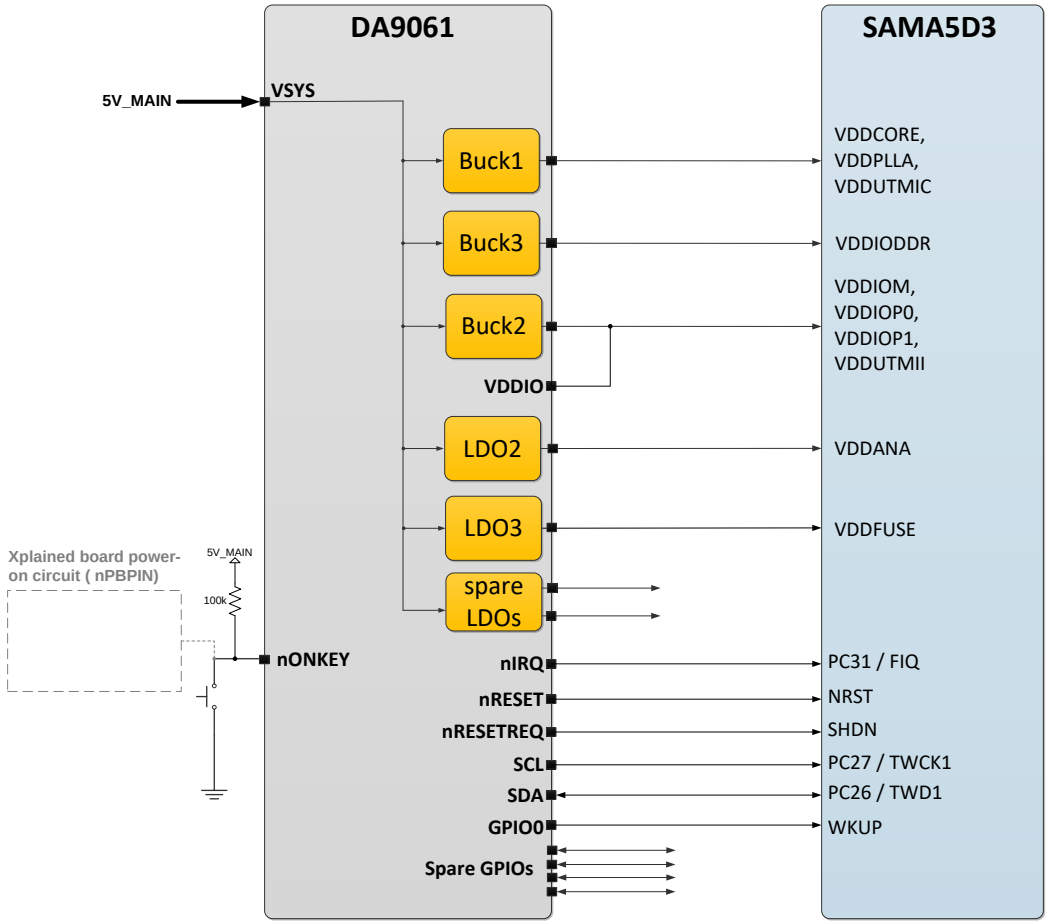

Figure 1: DA9061 and SAMA5D3 Interconnects

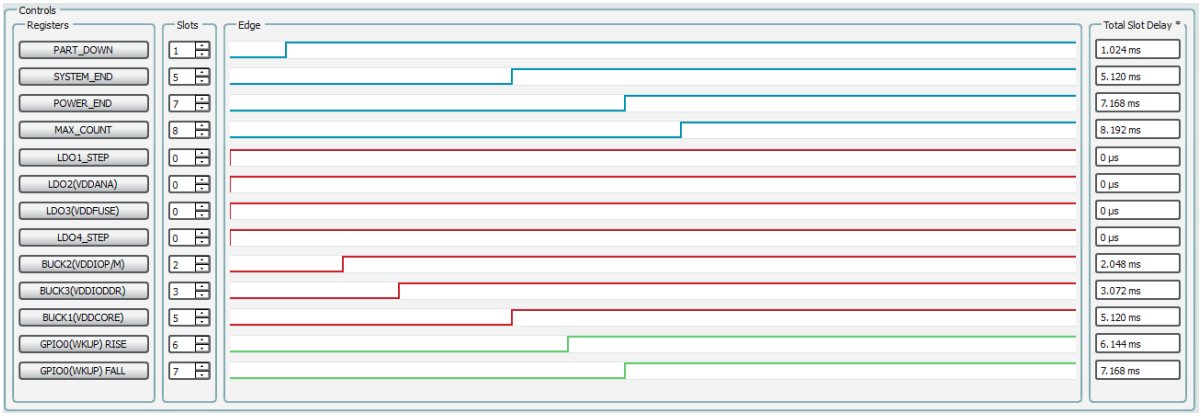

Figure 2: DA9061 Start-Up Power Sequence

6 Evaluation

A SAMA5D3 Xplained Evaluation Kit was successfully powered using a DA9061. The system was verified with its default boot configuration (with the processor mainly idle) and with a stress script to force the processor duty up to 100%. The tests were performed with the DA9061 bucks set in Auto mode. (In this test the bucks were running in PFM mode because of the low supply currents. The Dialog bucks are configured in Auto mode to ensure efficiency is optimised under all system load

conditions.) The total board current, I_{VBUS}, was measured at the USB input. This is the current supplying 5V_MAIN and is also the PMIC supply, VSYS.

Table 4: SAMA5D3 Xplained with DA9061 Evaluation Results

Parameter	Measured DA9061 current /mA	
	Standard Boot	Boot with MPU Stress Script
I_{VBUS}	150	177
I_{BUCK3}	31	60
I_{BUCK1}	57	109
I_{BUCK2}	124	124

6.1 Optimised Low Power Operation

The above evaluation results were achieved without optimising buck auto-thresholds, inductors, PCB layout and so forth. Dialog's PMIC architecture allows the optimised configuration to be programmed into the OTP so that the system automatically operates from startup with optimal efficiency. This avoids the need for software writes that are otherwise needed to place a PMIC into a power-saving mode.

Dialog PMICs also include dynamic voltage control (DVC) for the buck regulators. This feature allows setting of the regulator output voltage to a minimum value depending on the corresponding processor conditions (such as Active, Idle, Ultra Low-power and Backup). The DVC feature allows optimising of the power dissipation based on the actual processor speed and enables optimised low power operation. Such a scheme is implemented with minimal software overhead.

The DA9061/2 LDOs support switching between two pre-configured output voltages, VLDOx_A and VLDOx_B, either via software control or GPIO control. This allows lowering of the peripheral supply voltage when in suspend mode. Additionally, an LDO SLEEP mode can be linked to either the A or B settings. These features allow further reductions in system power dissipation.

7 Ordering Information

Devices with OTP configured for SAMA5D3 systems are orderable as standard variants:

DA9061-50

DA9062-50

Refer to the product datasheets for general ordering information. Please contact your Dialog Sales representative for further details on OTP variants.

8 Conclusions

The Dialog DA9061 and DA9062 support power management of the SAMA5D3 series of MPUs. Standard OTP variants are available from Dialog which have been verified in an Atmel SAMA5D3 Xplained Evaluation Kit.

Revision History

Revision	Date	Description
1.1	17-Feb-2022	File was rebranded with new logo, copyright and disclaimer
1.0	11-Feb-2016	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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