Gate Driver IC for IGBTs and SiC MOSFETs

Application Note for RAJ2930004AGM

Contents

Introduction

This application note summarizes features, functions and method to use it, regarding Renesas gate driver IC for IGBT and SiC MOSFET gate-drive in the high voltage applications such as traction inverters, DC-DC converters and On-board charger for EV/HEV in automotive.

Target Device

The scope of this application note is for RAJ2930004AGM.

1. Gate Driver IC features

The target device is a gate driver IC for IGBT and SiC MOSFET gate-drive in high voltage inverter applications. Integrated 3750Vrms micro-isolators provide data transfer with high voltage isolation between the primary circuit (MCU side) and the secondary circuit (IGBT or SiC MOSFET side). In addition, it boasts superior CMTI (Common Mode Transient Immunity) performance over 150 V/ns, providing reliable communication and increased noise immunity while meeting the high voltages and fast switching speeds required in inverter systems.

This device contains Gate drive circuit, Miller clamp circuit, and soft turn-off circuit as well as several types of protection circuits such as Overcurrent detection.

1.1 Features summary

The features of the target device is shown as follows.

	Part Number
Specifications	RAJ2930004AGM
Package	SOP16
Insulation voltage [Vrms], 1min	3750
CMTI [V/ns]	150
Gate drive output peak current [A]	10
VCC1 UVLO [V]	4.1
VCC2 UVLO [V]	10
Operating voltage [V]	12.5 - 33
Operating temperature [°C]	-40 - 125
Junction temperature [°C]	150
DESAT protection	✓
Current Sense protection	NA
Active miller clamp	✓
Soft turn-off function	✓
PWM interlock support (INA and INB)	✓

2. System application

2.1 Traction inverter system architecture

The traction inverter system is a system that converts DC power into AC power and is used in motors of xEV. In recent years, the demand for xEV has been increasing rapidly due to the tightening of CO2 reduction regulations and the increase in EV subsidies to stimulate the economy. There is also a need to improve the power efficiency of the traction inverter systems used in xEV in order to improve power costs and cruising range. Among them, instead of IGBT, SiC MOSFET use is getting more popular to reduce switching loss and improve the power efficiency of the traction inverter system.

Renesas Gate Driver IC (GDU) is used to drive inverters that convert DC power from battery into three-phase AC power to drive motors. The high voltage side consists of a motor, a high voltage battery that drives the motor and an IGBT or SiC MOSFET. And the low voltage side consists of an MCU, PMIC and a low voltage battery that provides power to the control circuit. In addition, the GDU is installed between the high and low voltage sides. The GDU not only drives the IGBTs, but also performs the functions of information communication and isolation between the high and low voltage sides.

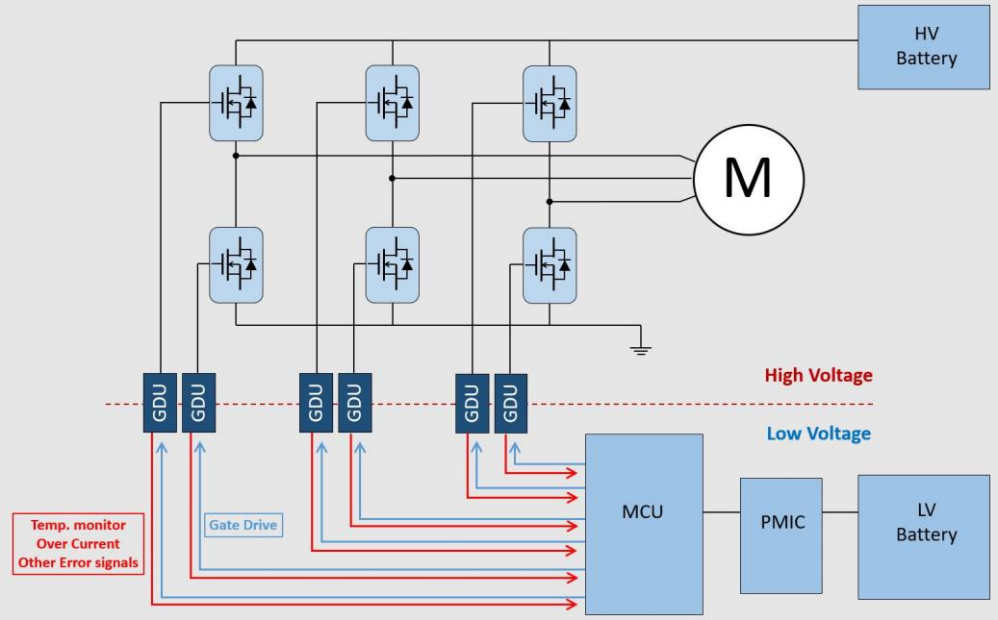


Figure 1. Traction inverter system

2.2 Application block diagram

Below diagram is Simplified application example diagram.
The external gate resistors (RGH, RGL) are connected to OUTH/OUTL. This is for controlling gate drive output peak current of GDU and power device switching speed. And this resistance is necessary to suppress the heating of GDU. The details of gate resister are shown in Chapter 3.2.
RAJ2930004AGM has DESAT protection. And external components (C_{blank}, R_{DESAT}, D_{DESAT}) are required for this function. The details of DESAT protection are shown in Chapter 3.3.
And this device has an on-chip active miller clamp and support VEE negative voltage input to prevent self turn-on of power device. The details of Active Miller Clamp and Negative Voltage consideration are shown in Chapter 3.4.
In addition, this device supports PWM interlock for shoot through protection. The details of PWM interlock are shown in Chapter 3.5.

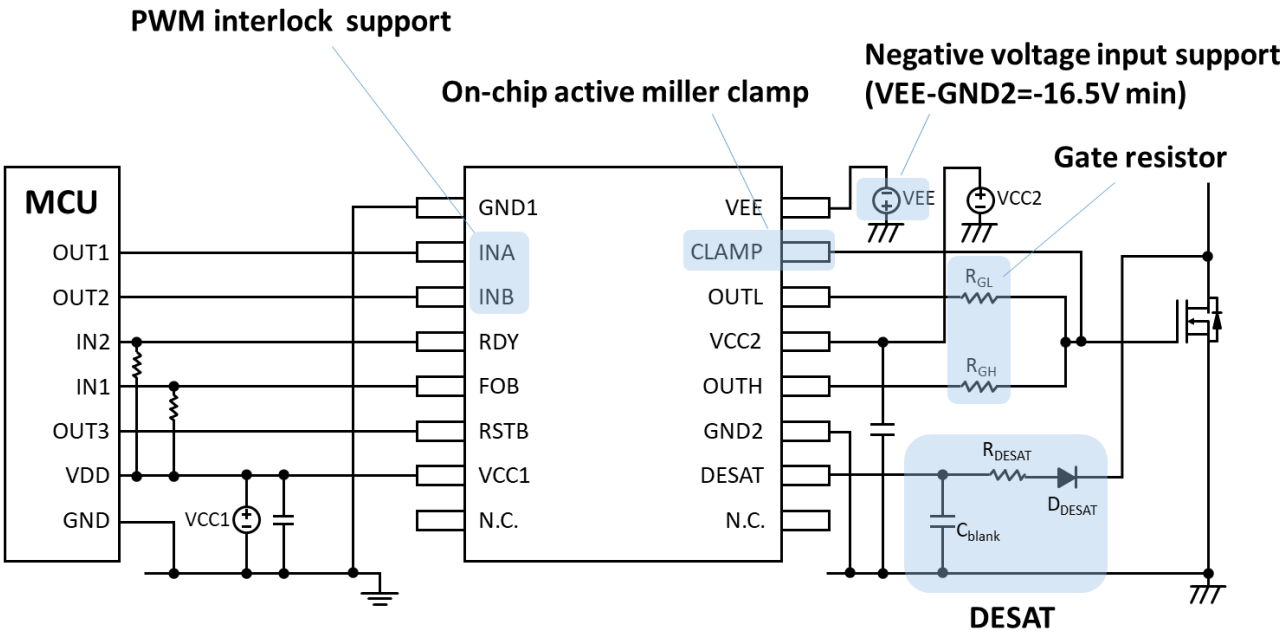


Figure 2. Application block diagram of RAJ2930004AGM

3. How to use / Hint

This chapter contains instructions and tips for using Renesas GDU.

3.1 PIN Configuration of Renesas GDU products

3.1.1 RAJ2930004AGM PIN Configuration

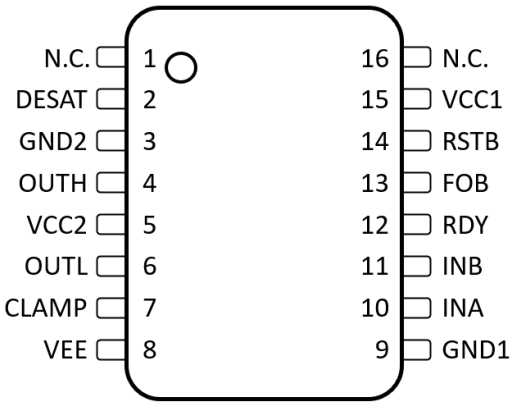


Figure 3. Pin assignment of RAJ2930004AGM

Table 1. Pin assignment and Functions of RAJ2930004AGM

No.	Pin Name	I/O	Functions
1	N.C.	-	Non-Connection
2	DESAT	I	DESAT input
3	GND2	P	Secondary side GND. Connect to IGBT Emitter
4	OUTH	O	Gate drive output (Positive)
5	VCC2	P	Secondary power supply input (15 V typ.)
6	OUTL	O	Gate drive output (Negative)
7	CLAMP	I/O	Active Miller clamp input / output
8	VEE	P	Negative power supply input. Connect to GND2 for Unipolar supply application.
9	GND1	P	Primary side GND
10	INA	I	Non-inverted gate drive input
11	INB	I	Inverted gate drive input
12	RDY	O	Power-good output
13	FOB	O	Inverted fault output (L level output at error)
14	RSTB	I	Reset input. Apply a low pulse to reset fault (FOB) latch.
15	VCC1	P	Primary side power supply input (5 V typ.)
16	N.C.	-	Non-Connection

3.2 Gate resistor consideration

The external gate resistors (RGH, RGL) are connected to OUTH/OUTL.
As shown in Table.2, there is much performance dependent on gate resistor and some performance has a relationship of the trade-off. And suitable resistance value is dependent on power device specifications.
So, it is necessary to decide resistance value by taking into consideration the power device specifications.
On the other hand, GDU has absolute maximum ratings for gate drive output peak current (15A) and junction temperature (150°C). Therefore, it is necessary to connect resistance satisfying these limitations at least.

Table 2. Performance dependent on gate resistor

Gate resistor

Small ⟷ Large

Switching speed	Fast	Slow
Switching loss	Small	Large
Gate drive output peak current	Large	Small
VDS surge	Large	Small
EMI	Bad	Good
GDU device heating	Large	Small

:Good
:Bad

3.2.1 Gate drive output peak current

The minimum gate resistance value necessary for GDU is decided by the absolute maximum ratings (Gate drive output peak current, Junction temperature).
The gate drive output peak current is defined as follows. It is necessary to decide external gate resistance value satisfying absolute maximum rating (15A).

$$I_{OUTH} = \frac{VCC2 - VEE}{R_{OUT} + R_{GH} + R_{G\_int}} \quad (1)$$

$$I_{OUTL} = \frac{VCC2 - VEE}{R_{OUT} + R_{GL} + R_{G\_int}} \quad (2)$$

R_{OUT}: GDU output NMOS on-resistance (pull-up/pull-down) 0.3Ω typ.

R_{GH}, R_{GL}: External gate resistor.

R_{G_int}: Internal gate resistance of the SiC or IGBT module.

3.2.2 Power loss calculation

The power dissipation must be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as follows.

$$P_{GD} = P_{GDQ} + P_{GSW} \quad (3)$$

P_{GD}: Total power loss

P_{GDQ}: Quiescent power loss

P_{GSW}: Switching power loss

Quiescent power loss is given by

$$P_{GDQ} = VCC1 \times I_{VCC1} + (VCC2 - VEE) \times I_{VCC2} \quad (4)$$

Switching power loss is given by

$$P_{GSW} = (VCC2 - VEE) \times Q_g \times f_{SW} \times R_{ratio} \quad (5)$$

Q_g: Gate charge of power device

f_{SW}: Switching frequency

R_{ratio}: Coefficient determined by internal Ron and external gate resistor

Coefficient Rratio is given by

$$R_{ratio} = \frac{1}{2} \times \left(\frac{R_{OUT}}{R_{OUT} + R_{GH} + R_{G_{int}}} + \frac{R_{OUT}}{R_{OUT} + R_{GL} + R_{G_{int}}} \right) \quad (6)$$

When the gate resistor of GDU device outside (R_{GH}, R_{GL}, R_{G_int}) is 0, R_{ratio} is 1. This is the condition where the power consumption of the GDU device is maximized.

Calculation example

$VCC1 = 5\text{V},\ VCC2 - VEE = 20\text{V},\ I_{VCC1} = 3\text{mA},\ I_{VCC2} = 5\text{mA},$

$Q_g = 4400\text{nC},\ f_{SW} = 15\text{kHz},\ R_{OUT} = 0.3\Omega,\ R_{GH} = R_{GL} = 2\Omega,\ R_{G\_int} = 0.7\Omega,$

$P_{GDQ} = 115\text{mW}$ (Quiescent power loss),

$P_{GSW} = 132\text{mW}$ (Switching power loss),

$P_{GD} = 247\text{mW}$ (Total power loss)

When the board temperature is 125°C, the junction temperature can be estimated as

$$\begin{aligned} T_j &= T_b + \Psi_{JB} \times P_{GD} \\ &= 125℃ + 31.8℃/\text{W} \times 0.247\text{W} \\ &= 133\ [℃] \end{aligned} \quad (7)$$

Ψ_{JB}: RAJ2930004AGM junction-to-board characterization parameter,
Based on JESD51-2 environment, JESD51-7 test board (4 layers board)

3.2.3 Conclusion of gate resistor selection

Chapter 3.2 shows the gate resistor explanation and the method of the gate resistor setting.
GDU has absolute maximum ratings for gate drive output peak current and junction temperature.
By these limitations, necessary minimum gate resistance value for GDU normal operation is decided
And the external gate resistance that addition needs is dependent on power device specifications (Q_g, R_{G_int}, *VGS(=VCC2-VEE)*, f_{sw}).
Therefore it is also necessary to consider the power device when making an external gate resistance value decision. After minimum gate resistance for GDU is decision, if there are EMI and VDS surge issues, adjust resistance value as needed.

3.3 DESAT consideration

RAJ2930004AGM has a DESAT functionality as an over current protection.

3.3.1 DESAT design outline

In general, DESAT protection absolutely needs to satisfy the following relationship (8) and (9).

$$t_1 + t_2 < t_{SC} \tag{8}$$

$t_1 + t_2$: DESAT protection time (see 3.3.2)

t_{SC}: Power device SCWT (Short Circuit Withstand Time), e.g. SiC:3us, IGBT:6us

$$V_{DESATth} > V_{DESATnormal} \tag{9}$$

$V_{DESATnormal}$: DESAT pin voltage in normal operation

Where

$$V_{DESATnormal} = V_f + I_{charge} \times (R_{DESAT} + R_{ON}) \tag{10}$$

DESAT function is abnormal-off protection, therefore need some consideration for noise to avoid unintended off. To increase the noise immunity of DESAT pin, Low Pass Filter with C_{blank} and R_{DESAT} should be formed. C_{blank} and R_{DESAT} should be big at the noise immunity point of view, on the other hand t_{BLANK} becomes long when C_{blank} becomes big. Therefore, DESAT protection time and noise immunity are trade-off. In case R_{DESAT} is bigger, $V_{DESATnormal}$ (=V_f + I_{charge} x (R_{DESAT}+ R_{on})) also becomes bigger. So $V_{DESATth}$ and $V_{DESATnormal}$ become close to each other and the malfunction by the noise becomes easy to happen.

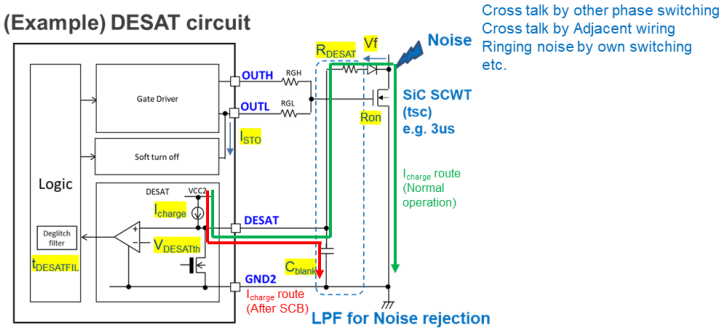


Figure 4. DESAT circuit diagram

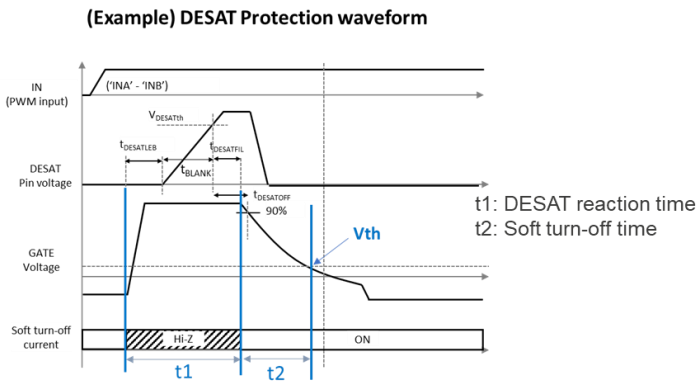


Figure 5. DESAT protection timing diagram

3.3.2 RAJ2930004AGM DESAT parameter

In case of RAJ2930004AGM, t_1 and t_2 at Figure 5 are defined as follows.
Parameter (C_{blank}) must be determined to satisfy (8)

$$t_1 + t_2 < t_{SC} \tag{8}$$

$$t_1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL} \tag{11}$$

$$t_2 = -C_{iss} \times R_{STO} \times \ln\left(\frac{V_{th}}{V_{GS}}\right) \tag{12}$$

Table 3. RAJ2930004AGM parameter

$t_{DESATLEB}$	200ns (typ) fixed
t_{BLANK}	t_{BLANK} = C_{blank} x $V_{DESATth}$ / I_{charge} C_{blank} : Determined by customer considering noise tolerance $V_{DESATth}$: 8.9V (typ) fixed I_{charge} : 500uA (typ) fixed
$t_{DESATFIL}$	140ns (typ) fixed
I_{STO} (R_{STO})	400mA (typ) fixed at OUTL = VEE+8V (20Ω (typ) equivalent)

3.3.3 DESAT protection time calculation example

Following Table shows DESAT protection time calculation example that used Wolfspeed SiC and Infineon IGBT. Generally, SCWT of SiC is around 3us and IGBT is around 6us so RAJ2930004AGM can protect from short circuit destruction.

	SiC	IGBT
$V_{DESATth}$ (V)	8.9	8.9
I_{charge} (mA)	0.5	0.5
C_{blank} (pF)	22	100
R_{DESAT} (kΩ)	6.8	6.8
R_{STO} (Ω)	20	20
Vgs (V)	15	15
Vth (V)	2.5	5.8
Ciss (nF)	38	80
$t_{DESATLEB}$ (ns)	200	200
t_{BLANK} (ns)	392	1780
$t_{DESATFIL}$ (ns)	140	140
	Correlation	Correlation
t1 (us)	0.7	2.1
t2 (us)	1.4	1.5
t1+t2 (us)	2.1	3.6

SiC: EAB450M12XM3 (Wolfspeed)
IGBT: FS950R08A6P2BBPSA1 (Infineon)

Generally
SiC SCWT: 3us
IGBT SCWT: 6us

Figure 6. DESAT protection time calculation example

3.3.4 tBLANK setting notes

t_{BLANK} can be adjusted by adjusting C_{blank}. As shown in following Graph, when decreased C_{blank}, t_{BLANK} becomes short. However, when applying a small C_{blank}, noise margin decreases (The LPF cut-off frequency determined by C_{blank} and R_{DESAT} increases) and the risk of malfunction due to noise increases.
So, it is necessary to set C_{blank} while being careful about the noise level of DESAT pin.

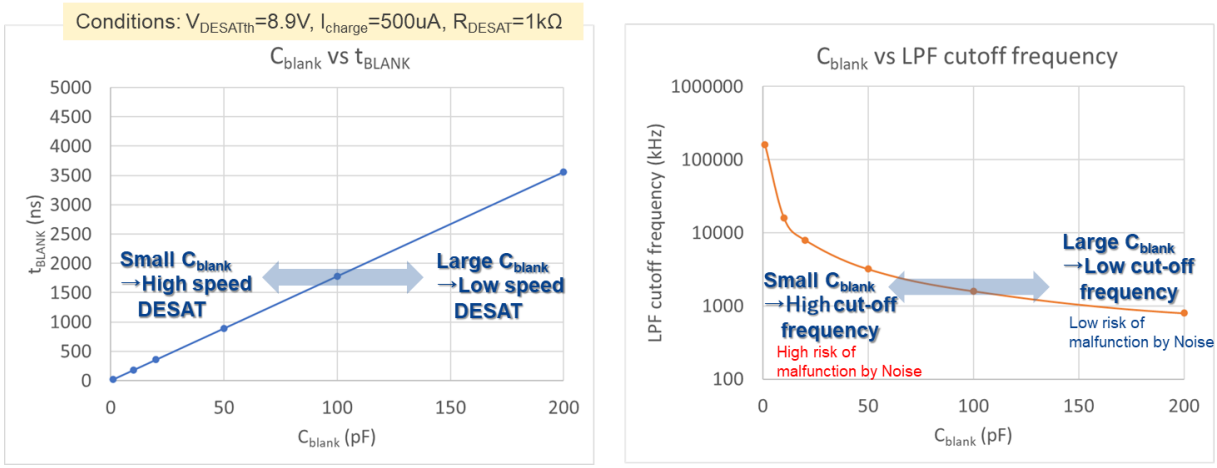


Figure 7. Relationship of C_{blank} and t_{BLANK}, of C_{blank} and LPF cut-off frequency

3.3.5 Soft turn-off during DESAT

During DESAT protection, soft turn-off function works. The reason for this function is to prevent destruction of the power device by the huge voltage spike (VDS overshoot) caused by parasitic inductance in the power loop.

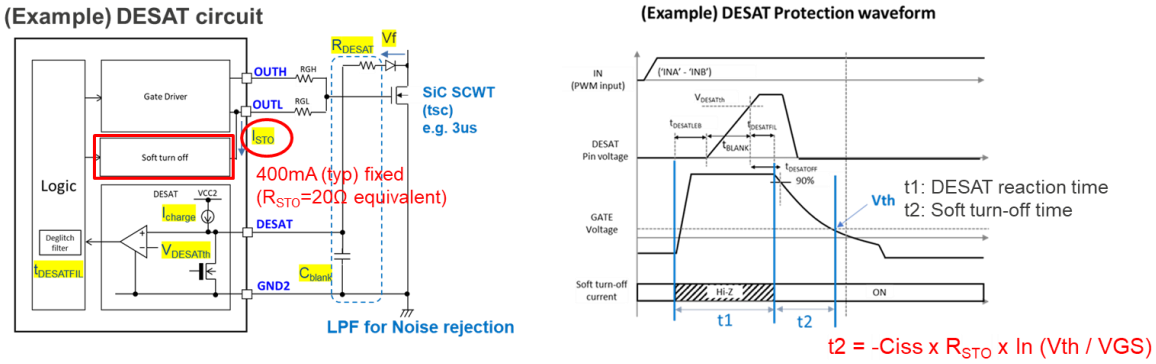


Figure 8. Soft turn-off operation during DESAT

3.3.6 Noise immunity improvement

For noise immunity improvement of DESAT pin, it is necessary to consider both PCB layout and external parts choice.

PCB layout

To prevent malfunction by switching noise (ringing noise) at the turn-on, DESAT line should be as short as possible to reduce L_{DESAT} in Figure 9.
To prevent DESAT line from noise (cross talk) of other signal line, it is better to be shielded by GND2.

External components choice

It is better to select DESAT Diode with a small junction capacitance ($C_{junction}$) to reduce noise level of DESAT pin. The noise level of DESAT pin is decided by the ratio of C_{blank} and $C_{junction}$.

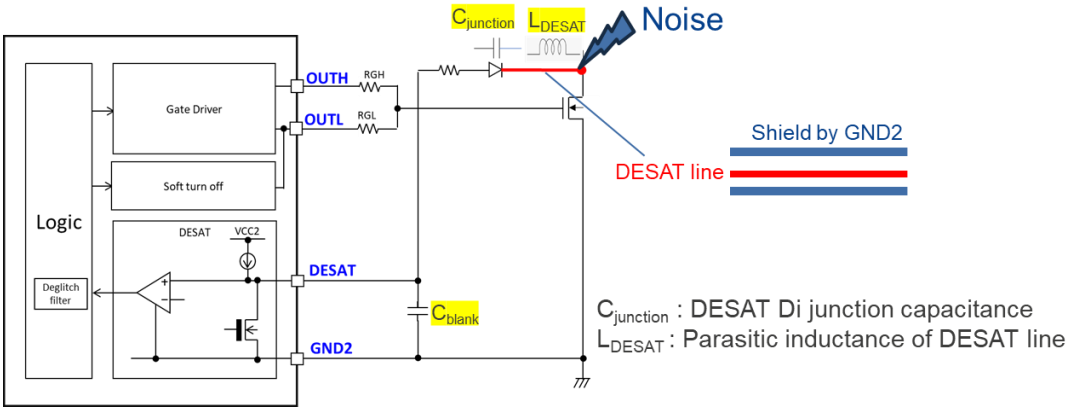


Figure 9. Noise immunity improvement

3.3.7 DESAT parameter setting example

As a DESAT parameter setting method example, please refer to below procedures.

Conditions

Power device: Renesas SiC (SCWT:3us(TBD), Vth:4V (TBD), Ciss:40nF (TBD))

GDU: Renesas RAJ2930004AGM

Setting method

Toward SCWT=3us requirement, set the target DESAT protection time to 2us with some margin.

(1) Calculate t2 (Soft turn off time) as soft turn off current 400mA (R_{STO}=20Ω equivalent)

$$t_2 = -40\text{nF} \times 20\Omega \times \ln\left(\frac{4\text{V}}{15\text{V}}\right) = 1057\ [\text{ns}]$$

(2) Calculate target t_{BLANK}

$$\text{Target } t_{BLANK} < 2\mu\text{s} - 1.057\mu\text{s} - t_{DESATLEB}(= 0.200\mu\text{s}) - t_{DESATFIL}(= 0.140\mu\text{s}) = 603\ [ns]$$

(3) Calculate maximum C_{blank} as $V_{DESATth}$ = 8.9V, I_{charge} = 500μA

$$C_{blank} < 603\text{ns} \times \frac{500\mu\text{A}}{8.9\text{V}} = 33.9\ [\text{pF}]$$

So selected C_{blank} = 33pF

(4) Calculate maximum R_{DESAT} as Vf=0.6V

$$R_{DESAT} < \frac{8.9\text{V} - 0.6\text{V}}{500\mu\text{A}} = 16.6\ [\text{k}\Omega]$$

When cut-off frequency is set to 1MHz (Assuming a turn-on time of 50ns, filter time 150ns (x3 margin))

$$R_{DESAT} = \frac{1}{2\pi \times 33\text{pF} \times 1\text{MHz}} = 4.8\ [\text{k}\Omega]$$

So selected R_{DESAT} = 4.7kΩ

Cut-off frequency of LPF by C_{blank}, R_{DESAT} is set to a value that is at least twice the turn-on time. (This is to prevent malfunction due to ringing during turn-on)
Turn-on time is the time until the VDS(VCE) of the power device drops. And it depends on the input capacitance and gate resister of power device.

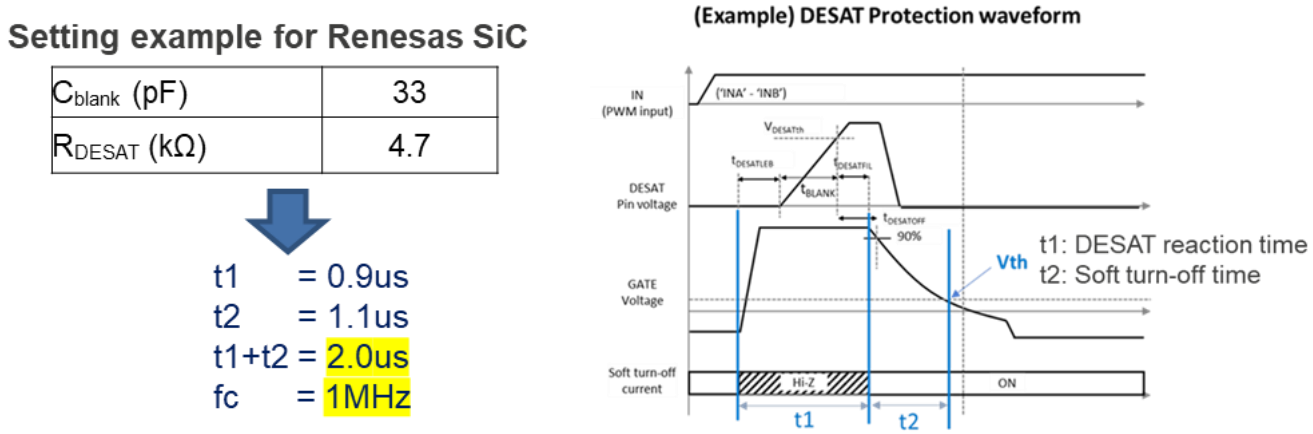
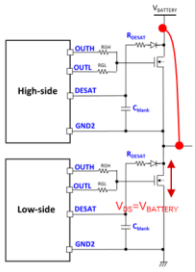
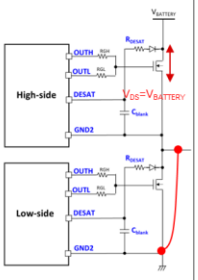
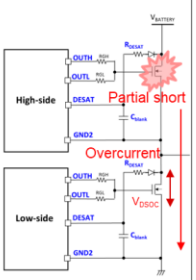
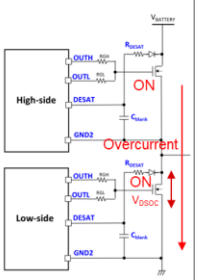
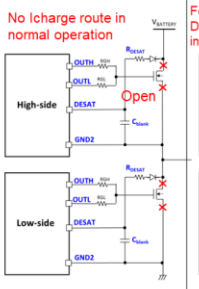
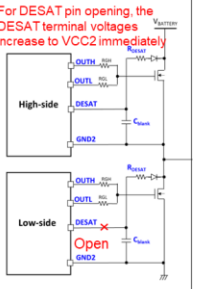


Figure 10. DESAT parameter setting example

3.3.8 Fault case example

Below Table is an example of fault cases which DESAT works.

Table 4. Fault cases

	Case1	Case2	Case3	Case4	Case5	Case6
Fault case	SCB (Short Circuit to Battery)	SCG (Short Circuit to GND)	Overcurrent (Due to partial short)	Through-current (Due to deadtime overlap by incorrect MCU signals)	Power device open	DESAT pin open
						
DESAT reaction time (t1)	$t1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL}$ $t_{DESATLEB}$=140ns $t_{DESATFIL}$=140ns $t_{BLANK} = C_{blank} \times V_{DESATth} / I_{charge}$	$t1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL}$ $t_{DESATLEB}$=140ns $t_{DESATFIL}$=140ns $t_{BLANK} = C_{blank} \times V_{DESATth} / I_{charge}$	$t1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL}$ $t_{DESATLEB}$=140ns $t_{DESATFIL}$=140ns t_{BLANK}=-$C_{blank} \times R_{DESAT} \times \ln(1-V_{DESATth} / V_{DESAT})$ $V_{DESAT} = Vf + I_{charge} \times R_{DESAT} + V_{DSOC}$	$t1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL}$ $t_{DESATLEB}$=140ns $t_{DESATFIL}$=140ns t_{BLANK}=-$C_{blank} \times R_{DESAT} \times \ln(1-V_{DESATth} / V_{DESAT})$ $V_{DESAT} = Vf + I_{charge} \times R_{DESAT} + V_{DSOC}$	$t1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL}$ $t_{DESATLEB}$=140ns $t_{DESATFIL}$=140ns $t_{BLANK} = C_{blank} \times V_{DESATth} / I_{charge}$	$t1 = t_{DESATLEB} + t_{BLANK} + t_{DESATFIL}$ $t_{DESATLEB}$=140ns $t_{DESATFIL}$=140ns t_{BLANK} = 0ns

3.3.9 Conclusion of DESAT functionality

Chapter 3.3 shows DESAT explanation and the method of DESAT parameter setting.
However, it is necessary to adjust each parameters depending on the specifications (SCWT, C_{iss}, V_{th} etc.) of the power device.
There is a trade-off between “DESAT protection time” and “Noise immunity” like following Table.
So, it is necessary to decide a parameter in consideration for both performance.
In addition, by reducing the parasitic elements (L_{DESAT}, $C_{junction}$) of the circuit, a small C_{blank} can be applied.
And DESAT protection time can be shortened.

Table 5. List of parameters to influence DESAT protection

Parameter		For short DESAT protection time	For strong noise immunity
Gate Driver	$V_{DESATth}$	Lower is better (RAJ2930004AGM is 8.9V fixed)	Higher is better (RAJ2930004AGM is 8.9V fixed)
	I_{charge}	Larger is better (RAJ2930004AGM is 500uA fixed)	Smaller is better (RAJ2930004AGM is 500uA fixed)
	I_{STO}	Larger is better (RAJ2930004AGM is 400mA fixed)	Smaller is better (RAJ2930004AGM is 400mA fixed)
External parts	C_{blank}	Smaller is better (e.g. 22pF)	Larger is better (e.g. 100pF)
	R_{DESAT}	No influence	Larger is better
	$C_{junction}$	No influence	Smaller is better
PCB	L_{DESAT}	No influence	Smaller is better

3.4 Active Miller Clamp and Negative Voltage consideration

RAJ2930004AGM has an on-chip Active Miller Clamp (AMC) and support VEE negative voltage input to prevent self turn-on of power device.

3.4.1 Self turn-on phenomenon

As shown in Figure 11, when the Low-side is OFF and High-side becomes ON, VDS voltage of Low-side increases rapidly. And the voltage to be decided by the ratio of Cgd and Cgs occurs at the gate. Furthermore, through Cgd, an electric current flow to R_{GL} and abnormal voltage occurs at the gate. Due to this increase at the gate voltage, Low-side may malfunction (turn-on). This is self turn-on.

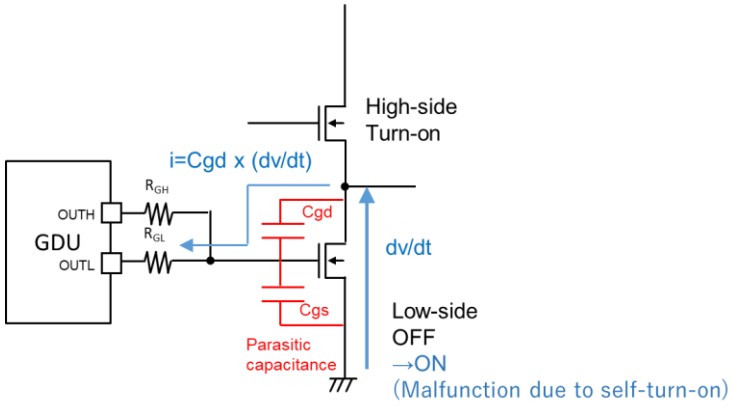


Figure 11. Self turn-on

3.4.2 Self turn-on measures

To prevent self turn-on, RAJ2930004AGM has an internal AMC function. The threshold voltage of AMC is VEE+2V. If the CLAMP pin voltage falls below VEE+2V, the gate is short-circuited to the VEE with low resistance.
However, if the power device has lower threshold voltage and bigger Cgd, AMC may be not enough.
In that case, apply negative voltage to VEE (min -16.5V) for stronger OFF.

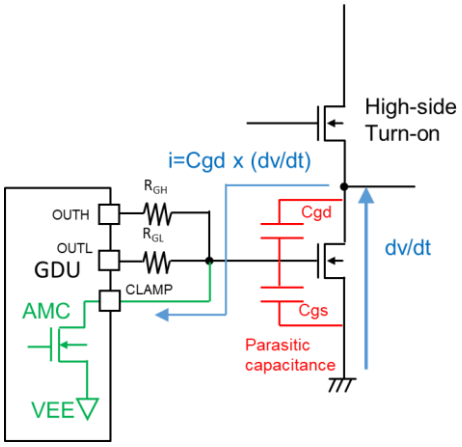


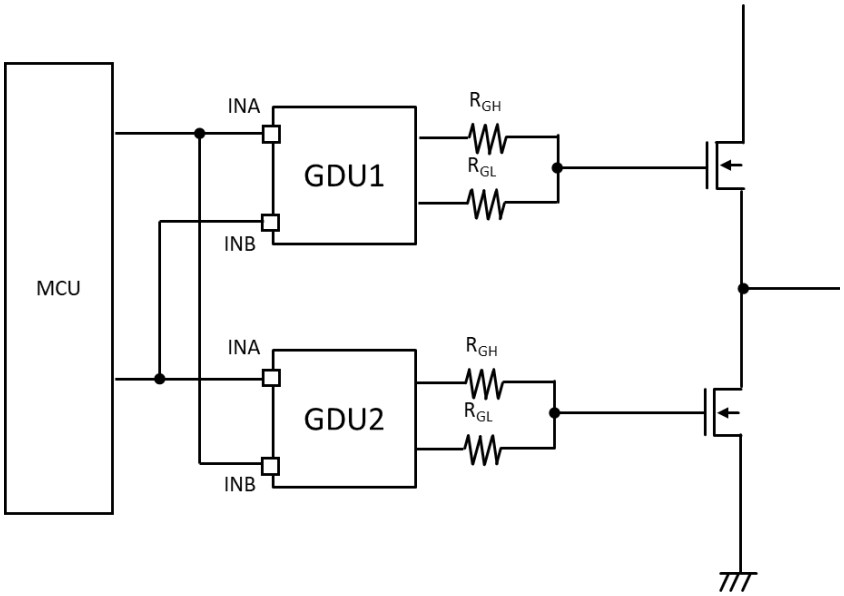
Figure 12. Active Miller Clamp

3.5 Shoot through protection consideration

The RAJ2930004AGM features the PWM interlock for INA and INB, which can be used to prevent the phase leg shoot through issue.

As shown in Figure 13, to use the PWM interlock function, INA of GDU1 is connected INB of GDU2.

By this connection, when INA of GDU1 is high, even if high is input into INA of GDU2 by error, it becomes OFF forcibly.



#	INA	INB	OUTH / OUTL	Power device State
1	L	X	L	OFF
2	X	H	L	OFF
3	H	L	H	ON

Figure 13. PWM interlock for a Half Bridge

4. Conclusion

Traction inverter system is indispensable for xEV. To drive IGBT or SiC MOSFET, Gate Driver IC which includes isolation functionality plays an important role in that system. Renesas Gate Driver IC products offer great contribution to inverter systems for its optimization, through the functionality and features. Please visit Renesas.com and if further information is needed, please contact us (http://www.renesas.com/us/en/contact-us).

Revision History

Revision	Date	Page	Changes
1.00	Feb.26.24		Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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