NEC

Application Note

DMX512

78K0/Ix2 Series

Lighting ASSP

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NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668, Japan
Tel: 044 4355111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554,
U.S.A.
Tel: 408 5886000
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211 65030
http://www.eu.necel.com/

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908 691133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01 30675800

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 6387200

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02 667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven,
The Netherlands
Tel: 040 2654010

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27
ZhiChunLu Haidian District,
Beijing 100083, P.R.China
Tel: 010 82351155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2511-2512, Bank of China
Tower,
200 Yincheng Road Central,
Pudong New Area,
Shanghai 200120, P.R. China
Tel: 021 58885400
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NEC Electronics Hong Kong Ltd.
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
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NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R.O.C.
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238A Thomson Road,
#12-08 Novena Square,
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Yeoksam-Dong, Kangnam-Ku, Seoul,
135-080, Korea Tel: 02-558-3737
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Chapter 1 DMX512 Communication Protocol

1.1 Control Interface

The DMX data stream clocks out at a rate of 250 kHz, which means each bit is measured in 4 microseconds. The DMX512 signal is transmitted via RS485, which is the industry standard interface.

The RS485 standard uses two or three wires to transmit digital HIs and LOs:

- The +signal wire (+s)
- The –signal wire (–s)
- The 0 wire or ground wire (0 V)

Figure 1-1 shows the DMX receiver hardware interface.

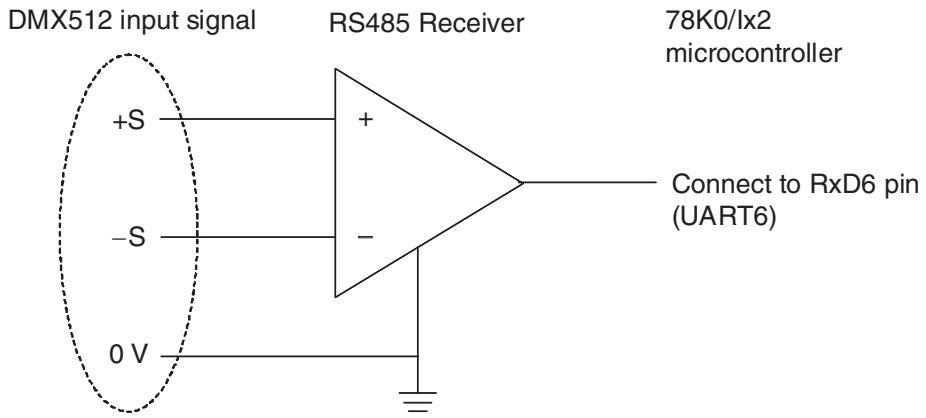
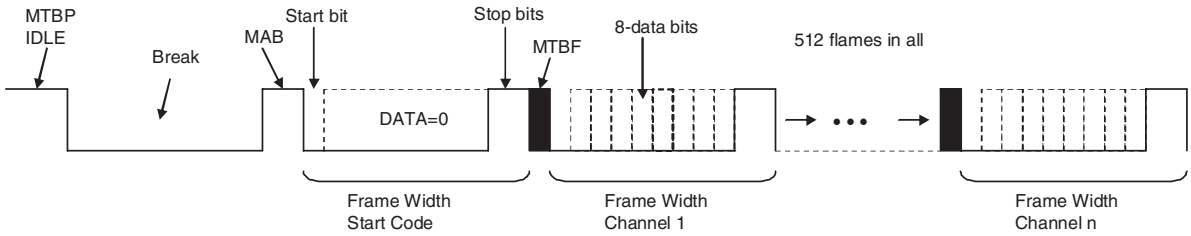


Figure 1-1 DMX512 Receiver Hardware Interface

Figure 1-2 shows the DMX timing chart.



	MIN.	TYP.	MAX.	Unit
Break	88	88	1,000,000	μs
MAB		8		μs
Frame Width		44		μs
Start/Data/Stop bits		4		μs
MTBF	0	NS	1,000,000	μs
MTBP	0	NS	1,000,000	μs

Figure 1-2 DMX512 Timing Chart

Remark NS: not specified

The meanings of addresses and data freely are defined by users. For example, while the DMX512 protocol is used to control stage lighting, one lamp has several addresses and data can be defined as the brightness, position, and so on.

The first byte after the start code (SC) is automatically taken as the data value for address 1, the next data value is for address 2, and so on. The slave counts the data and uses that which belongs to its address to start dimming processing.

Figure 2-1 shows the flowchart of the dimming control by the DMX512 protocol communication interface. In this example, the 3 LED channels are controlled using independent address.

Chapter 2 Dimming Control by DMX

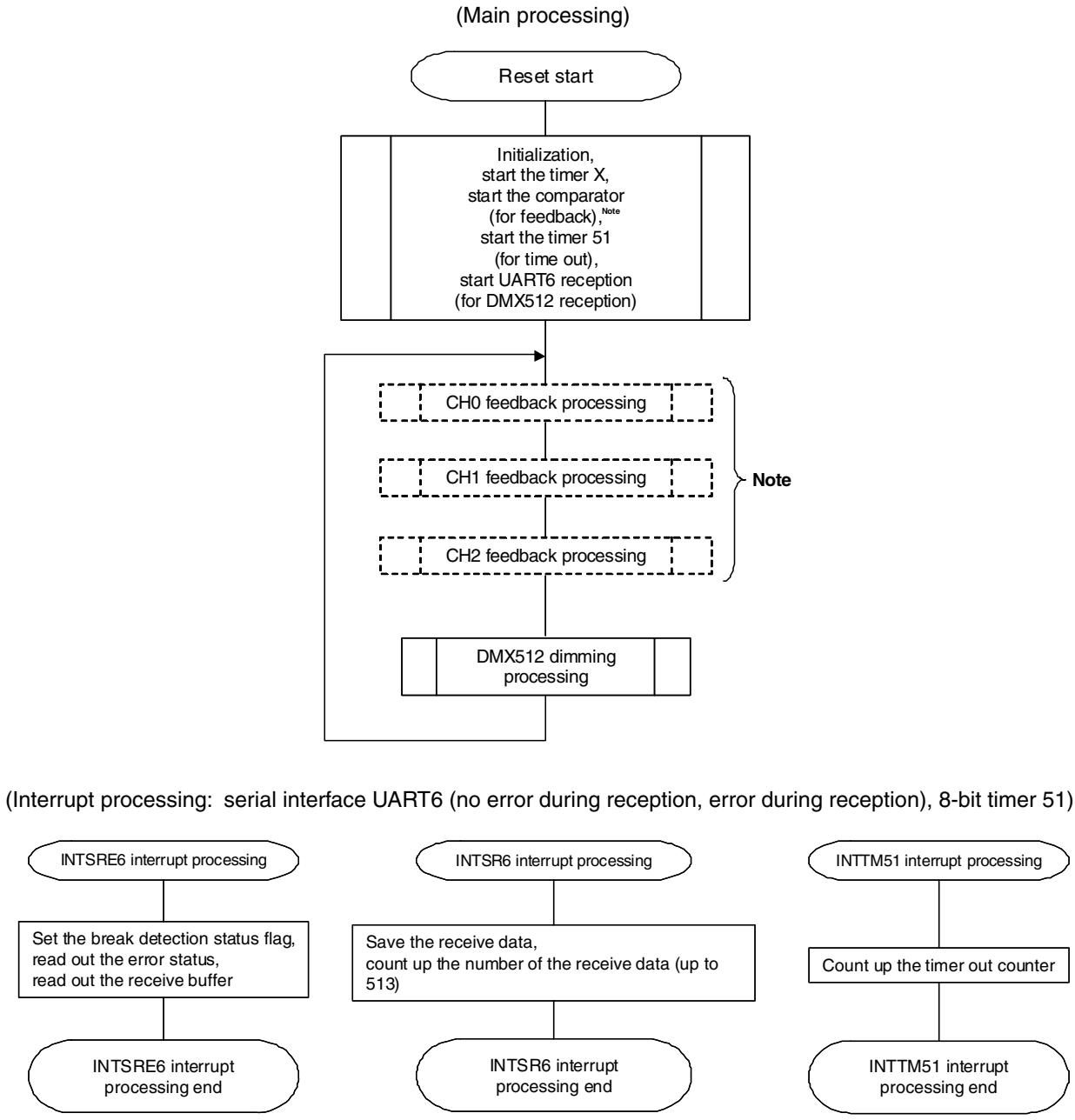


Figure 2-1 Flowchart of Dimming Control by DMX512 Protocol Communication Interface (1/2)

Note Using the comparator feedback processing only.

Caution Dimming processing controlled by DMX512 interface starts when the serial interface UART6 receives an error interrupt.

Remark The break detection status flag is used to show that the break time of the DMX512 signal has been detected.

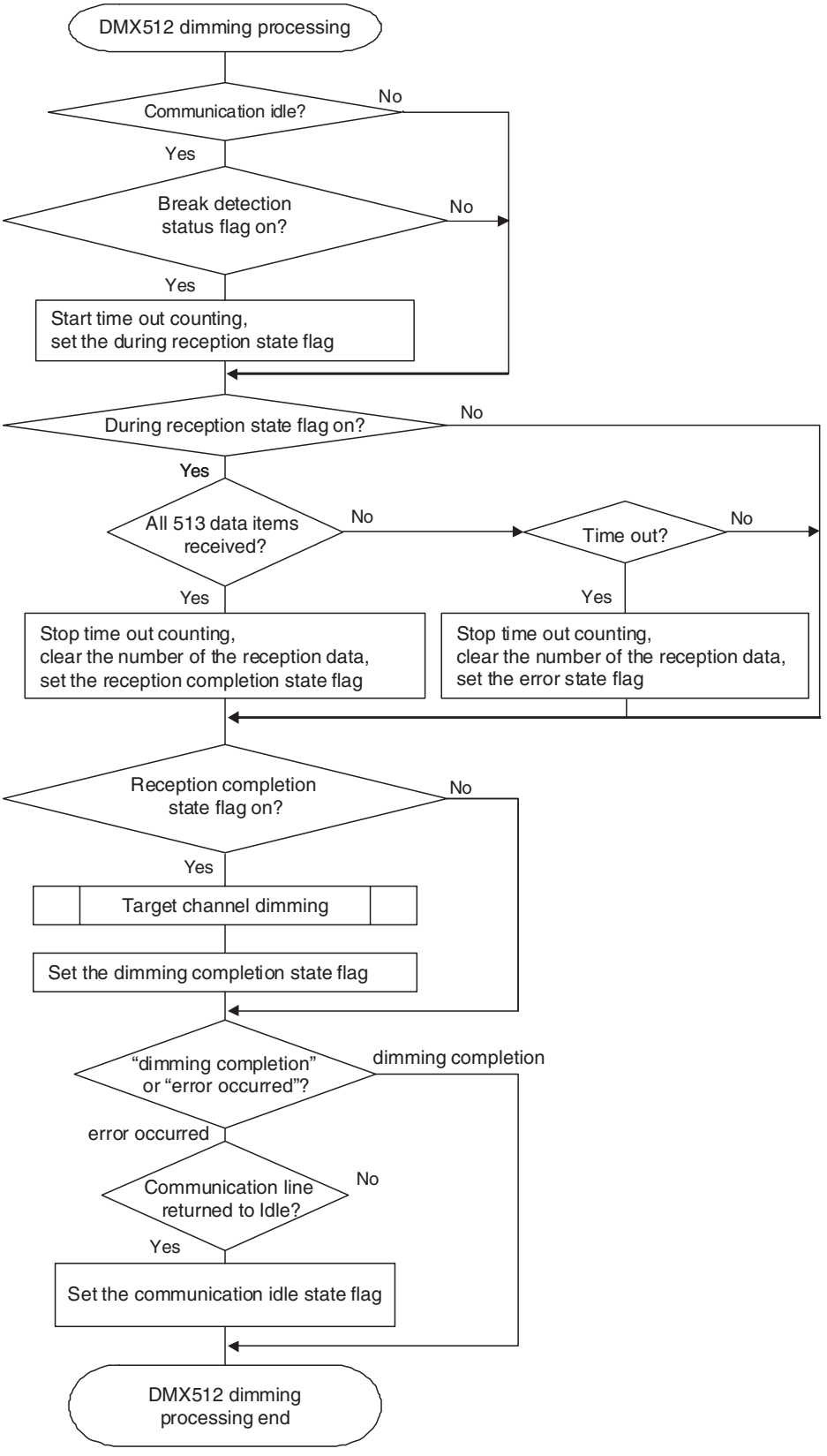


Figure 2-2 Flowchart of Dimming Control by DMX512 Protocol Communication Interface (2/2)

Caution Dimming processing controlled by DMX512 interface starts when the serial interface UART6 receives an error interrupt.

Remark The status flag is used to show that the communication status has been detected during reception.

Chapter 3 Appendix: Code Examples

3.1 Initialization of UART6 for DMX communications

```
void UART6_DMX_init(void)
{

   PORT_MODE_TXD6 = OUTPUT;       /* set output to TXD6 port mode */
   PORT_TXD6 = LEVEL_HIGH;        /* set High-Level to TXD6 port */
   PORT_MODE_RXD6 = INPUT;        /* set input to RXD6 port mode */
   UADLCTL = UADLCTL_INIT_VALUE;  /* set UART mode to UADLCTL */
   CKSR6 = CKSR6_INIT_VALUE;      /* set baud rate */
   BRGC6 = BRGC6_INIT_VALUE;
   POWER6 = BIT_SET;              /* internal operation clock enabled */

                                  /* transmission             :enable */
                                  /* reception                :enable */
                                  /* parity                   :none parity */
                                  /* character length of data :8bit */
                                  /* number of stop bits      :2bit */
   ASIM6 |= ASIM6_INIT_VALUE;

   SRMK6 = INTERRUPT_UNMASKED;    /* interrupt by UART6 reception is permitted */
   SRPR6 = PRIORITY_HIGH;
}
```

3.2 Receive a byte through DMX interface

```
unsigned short  UART6_DMX_getValue( unsigned char ucChannel )
{
   unsigned char ucDutyElement = 0;

   /* when the number of channel is in the tolerance */
   if ((ucChannel >= 1) && (ucChannel <= 3)) {
      ucDutyElement = g_ucDMXData[ucChannel];         /* return reservation duty value */
   }

   return g_ucConvertValue[ucDutyElement];
}
```

3.3 UART DMX Interrupt

```
__interrupt void  UART6_DMX_receive_interrupt( void )
{
    unsigned char ucError = ASIS6 & 0x07;
    unsigned char ucRcv = RXB6;

    if((ucError & 0x02) == 0x02) {
        if(g_ucDMXStatus != DMX_RCV_DATA) {
            breakCheckStop();
        }
        g_ucDMXStatus = DMX_RCV_BREAK;
        breakCheckStart();
    }
    else {
        switch(g_ucDMXStatus) {
```

```
        case DMX_RCV_BREAK:
            breakCheckStop();
            g_ushFrameCount = 0;
            g_ucDMXStatus = DMX_RCV_DATA;
        case DMX_RCV_DATA:
            if(ucError == 0) {
                if( g_ushFrameCount == 0 )
                {
                    if( ucRcv == 0x00 )
                    {
                        g_ucDMXStartCode = 0x00;
                    }
                    else
                    {
                        g_ucDMXStartCode = 0xFF;
                    }
                }
                if( g_ucDMXStartCode == 0x00 ){
#ifdef DMX_CHANNEL_NO_LED1
                    if( g_ushFrameCount == DMX_CHANNEL_NO_LED1 )
                    {
                        g_ucDMXData[1] = ucRcv;
                    }
#endif
#ifdef DMX_CHANNEL_NO_LED2
                    if( g_ushFrameCount == DMX_CHANNEL_NO_LED2 )
                    {
                        g_ucDMXData[2] = ucRcv;
                    }
#endif
#ifdef DMX_CHANNEL_NO_LED3
                    if( g_ushFrameCount == DMX_CHANNEL_NO_LED3 )
                    {
                        g_ucDMXData[3] = ucRcv;
                    }
#endif
                    if( g_ushFrameCount == 512 )
                    {
                        g_ucDMXStatus = DMX_WAIT_BREAK;
                        g_ucDMXStartCode = 0xFF;
                    }
                }
            }
            g_ushFrameCount++;
            break;
        default:
            break;
        }
    }
}

void breakCheckStart(void)
{
    TMC00 = TMC00_DMX_STOP_VALUE;   /* stop operation clock supply for 16bit timer */
    CRC00 = CRC00_DMX_VALUE;        /* CR000 operates as compare register */
    TOC00 = TOC00_DMX_VALUE;        /* TO00 is not output */
    PRM00 = PRM00_DMX_VALUE;
    CR000 = CR000_DMX_VALUE;

    MUXSEL &= MUXSEL_DMX_VALUE;

    TMIF000 = FLAG_DOWN;            /* INTTM000 interrupt flag clear */
    TMMK000 = INTERRUPT_UNMASKED;   /* INTTM000 disabled */
    TMPR000 = PRIORITY_HIGH;
    g_uc1Sec = 0;
    TMC00 = TMC00_DMX_START_VALUE;
}

void breakCheckStop()
{
    TMMK000 = INTERRUPT_MASKED;     /* INTTM000 disabled */
    TMC00 = TMC00_DMX_STOP_VALUE;   /* stop operation clock supply for 16bit timer */
    TMIF000 = FLAG_DOWN;            /* INTTM000 interrupt flag clear */
```

```
}

__interrupt void  DMX_breakCheck_interrupt( void )
{
    g_uc1Sec++;
    if(g_uc1Sec == 2) {
        breakCheckStop();
        g_ucDMXStatus = DMX_WAIT_BREAK;
    }
}
```

3.4 Definitions

```
#define    DMX_WAIT_BREAK          0
#define    DMX_RCV_BREAK           1
#define    DMX_RCV_DATA            2

#define    TMC00_DMX_STOP_VALUE    0x00
#define    TMC00_DMX_START_VALUE   0x0C
#define    CRC00_DMX_VALUE         0x00
#define    TOC00_DMX_VALUE         0x00
#define    MUXSEL_DMX_VALUE        0x0F

/* value that should be stored in register to set interval time (1second) */
#define    CR000_DMX_VALUE            39062
#define    PRM00_DMX_VALUE            0x02

/* definition of interrupt mask setting value */
#define    INTERRUPT_UNMASKED  0
#define    INTERRUPT_MASKED    1

/* definition of flag variables setting value */
#define    FLAG_DOWN           0
#define    FLAG_UP             1

/* definition of priority setting value */
#define    PRIORITY_HIGH       0
#define PRIORITY_LOW           1
```