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April 1st, 2010
Renesas Electronics Corporation

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M32C/85 Group

Application Example of Multiple-Channel PWM Using DMAC

1. Abstract

The following document describes procedures and examples of use to perform multiple-channel PWM output using DMAC.

2. Introduction

Application examples described in this document are applied to the following microcomputer and condition:
Applicable Microcomputer : M32C/85 Group

This program can be used for the other M16C Families which have the same SFR (Special Function Register) as the one in the M32C/85 Group. However, since some functions may be modified such as added functions, please ensure in a manual. Please evaluate sufficiently when using this application note.

3. Description of Use Example

Application examples which perform 64 PWM outputs from the ports P0 to P7 every timing of Timer B0 underflow using Timer B0 and 4 DMACs are described after preparing PWM output pattern on ROM.

Example of Use :

- System condition
  VCC1=VCC2=5.0V, XIN=8MHz, PLL=quadruple, f1=32MHz

- DMAC setting

	DMA Request Factor	Transfer Mode	Transfer Unit	Transfer Direction
DMA0	Timer B0 Interrupt Request	Repeat Transfer	16 Bit	Memory(forward)→Fixed address(P0) (Output to P0 to P1 in 16-bit unit)
DMA1				Memory(forward)→Fixed address(P2) (Output to P2 to P3 in 16-bit unit)
DMA2				Memory(forward)→Fixed address(P4) (Output to P4 to P5 in 16-bit unit)
DMA3				Memory(forward)→Fixed address(P6) (Output to P6 to P7 in 16-bit unit)

- TB0 setting
  Timer mode, count source=f1(32MHz), Period (Modify between 100μs to 900μs)

Operation :

PWM output is performed to 64 ports of P0 to P7 which function as output port by DMA transfer every underflow period of Timer B0. (connect (pull-up) to VCC1 via resistor since P7_0 and P7_1 are ports for the N-channel open drain output). Also, PWM pulse output width is modified by changing the timer value of Timer B0 during Timer B0 interrupt process. Figure 3.1 shows the PWM Output Timing Chart.

Precautions :

When timer pulse output is performed combining Timer B and DMAC, note the following points.

- DMA transfer priority
  When DMA request is generated simultaneously, transfer is performed by the priority of DMA0>DMA1>DMA2>DMA3.
- Delay cycle number of DMA transfer
  When transfer is performed under the conditions of this use example (program allocation area=internal ROM, transfer source=internal ROM, transfer distination=SFR area), delay is generated in 0 to 5 cycles transfer of the CPU clock. (The delayed cycle numbers are changed depending on wait numbers of memory when using the external memory).
- Delay time when Timer B starts
  The execution time of the instruction until Timer B starts after setting the port direction register to output is assumed as delay time for the first pulse output when Timer B starts.
- Delay time of pulse output
  The actual pulse output is output behind DMA transfer cycle numbers and DMA transfer delay cycle numbers after Timer B interrupt request is generated.

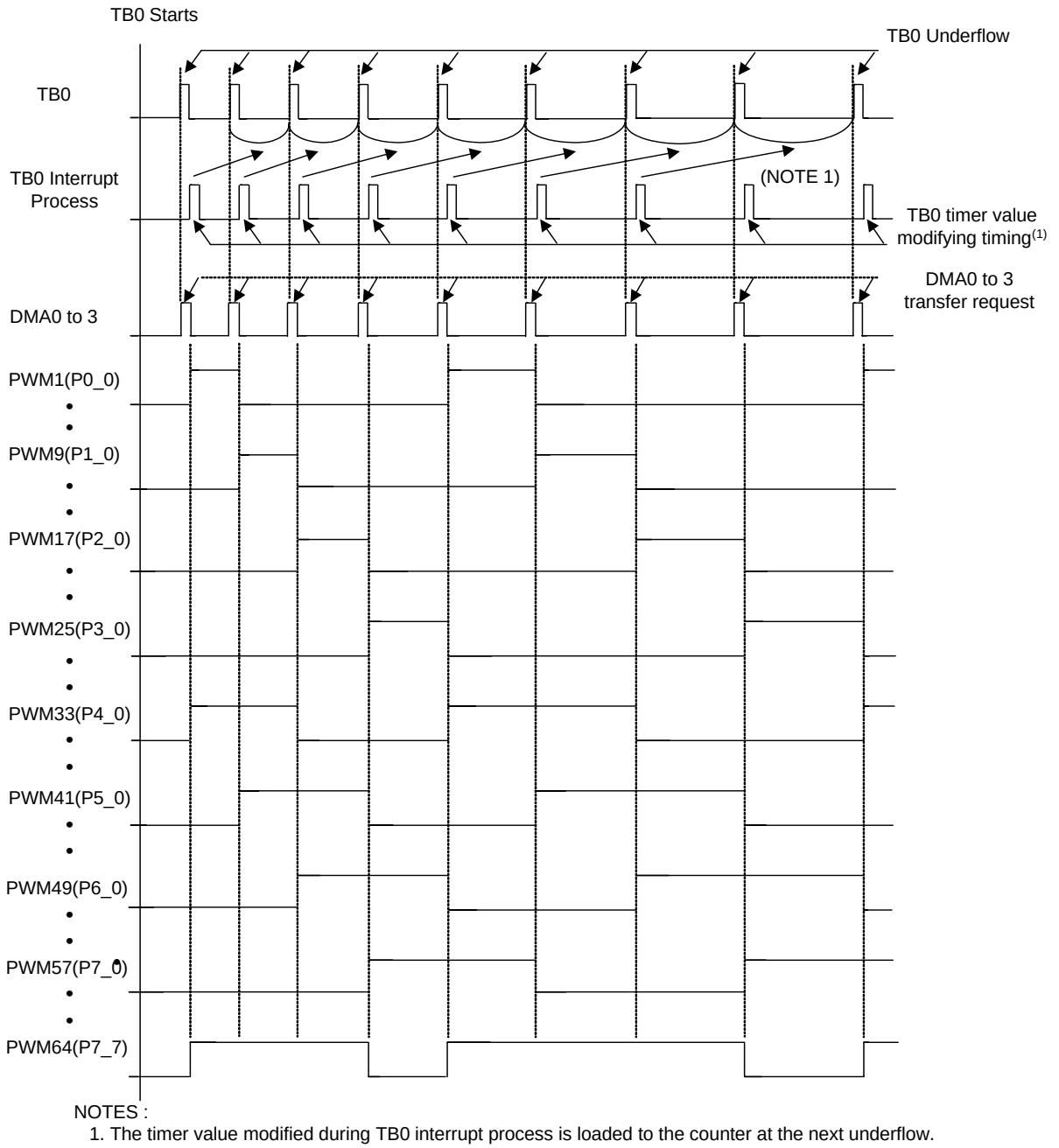
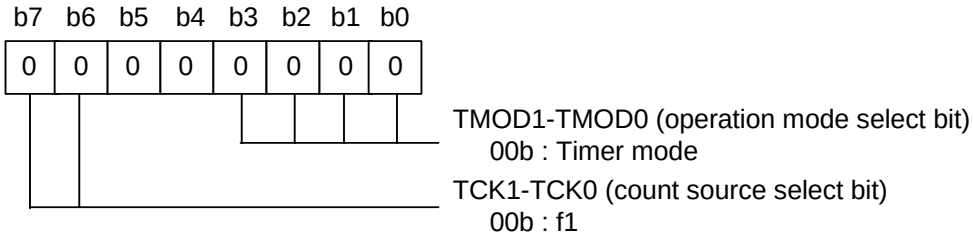


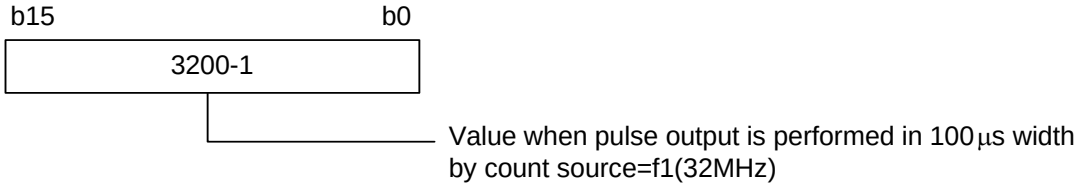
Figure 3.1 PWM Output Timing Chart

(1) Timer B0 (DMA0 to 3 request factors) setting

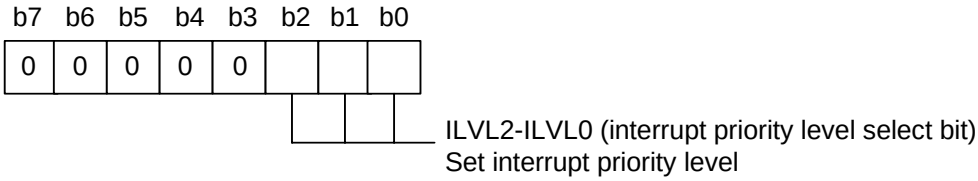
• Set TB0MR register (Timer B0 mode register)



• Set PWM pulse width default value to TB0 (Timer B0 register)

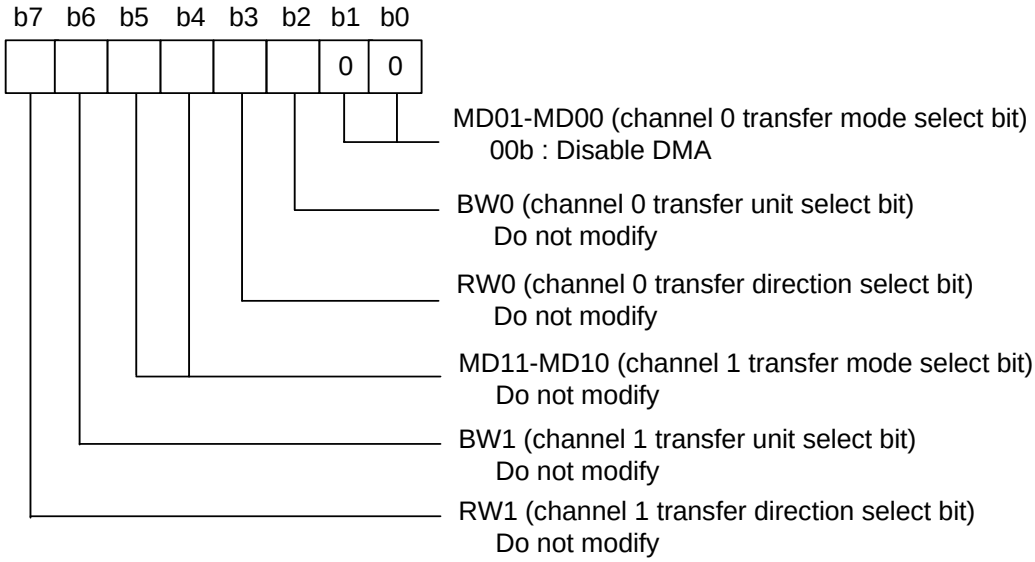


• Set TB0IC (Timer B0 interrupt control register)

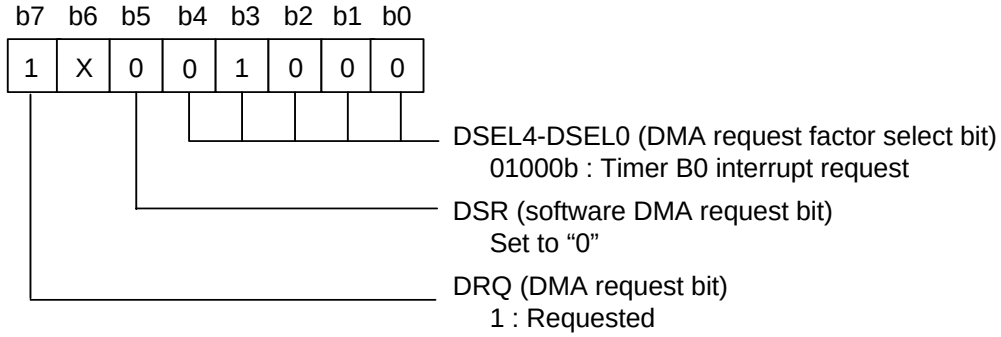


(2) DMA0 setting

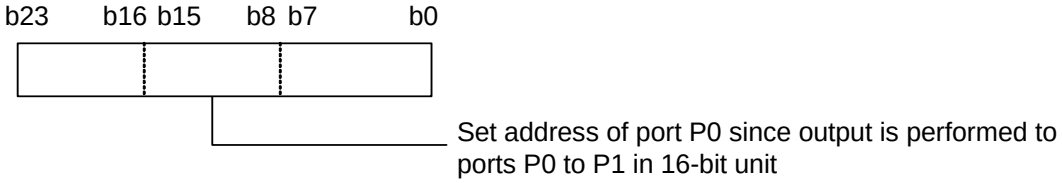
• Set (disable DMA0) DMD0 register (DMA mode register 0)



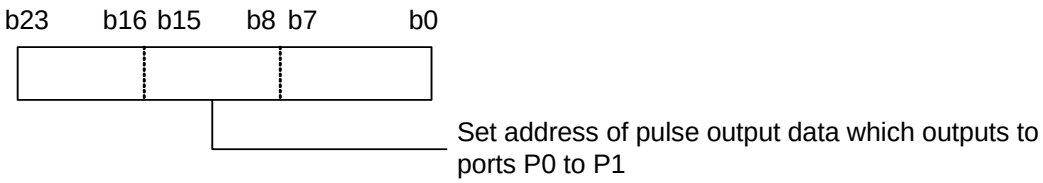
• Set DM0SL register (DMA0 factor select register)



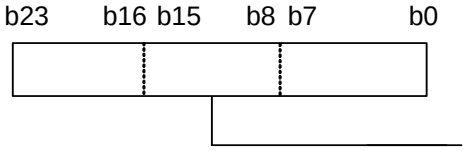
• Set DSA0 register (DMA0 SFR address register)



• Set DRA0 register (DMA0 memory address reload register)

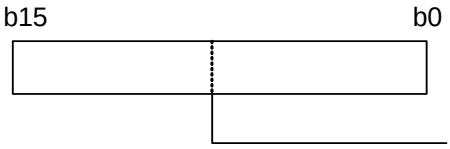


• Set DMA0 register (DMA0 memory address register)



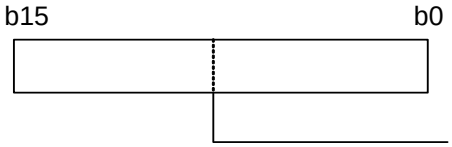
Set address of pulse output data which outputs to ports P0 to P1

• Set DRC0 register (DMA0 transfer count reload register)



Set numbers of pulse output data

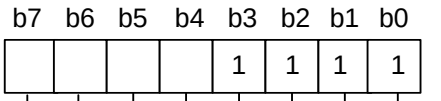
• Set DCT0 register (DMA0 transfer count register)



Set numbers of pulse output data

• Insert dummy cycle
Enable DMA after setting the DM0SL register and waiting for 6 cycles by BCLK.
This document shows inserting 6 NOPs waits for 6 cycles.

• Re-set (enable DMA0) DMD0 register (DMA mode register 0)



MD01-MD00 (channel 0 transfer mode select bit)
11b : Repeat transfer

BW0 (channel 0 transfer unit select bit)
1 : 16 bit

RW0 (channel 0 transfer direction select bit)
1 : Memory (forward) → Fixed address

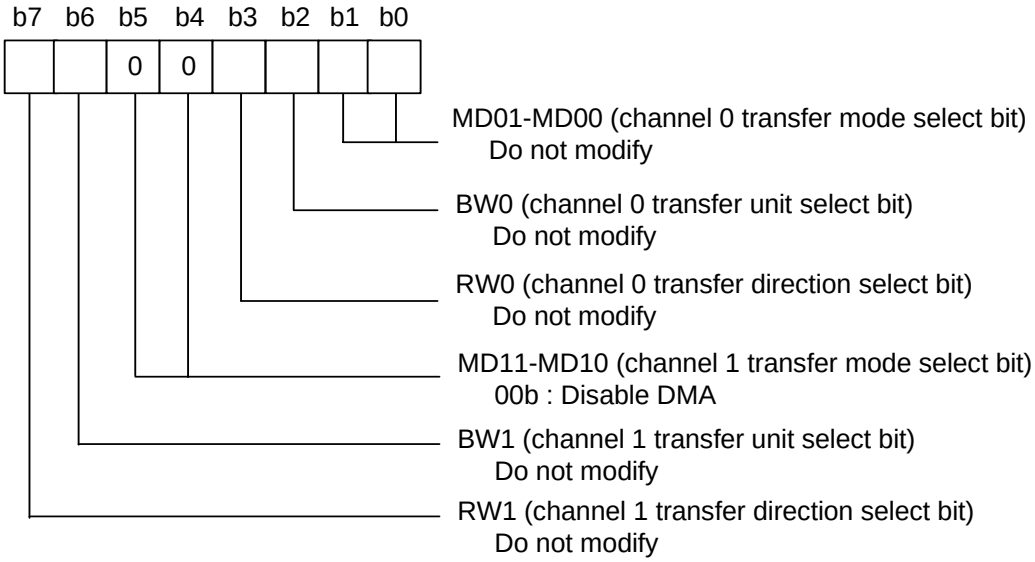
MD11-MD10 (channel 1 transfer mode select bit)
Do not modify

BW1 (channel 1 transfer unit select bit)
Do not modify

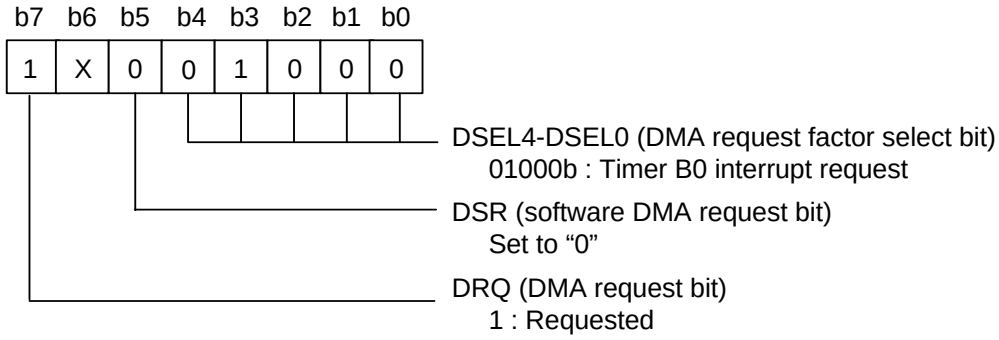
RW1 (channel 1 transfer direction select bit)
Do not modify

(3) DMA1 setting

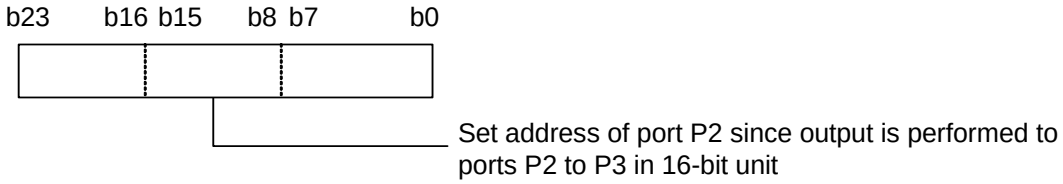
• Set (disable DMA1) DMD0 register (DMA mode register 0)



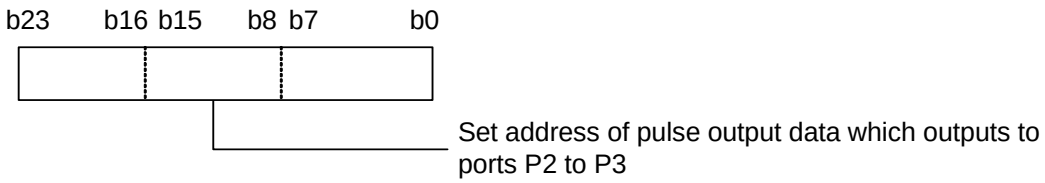
• Set DM1SL register (DMA1 factor select register)



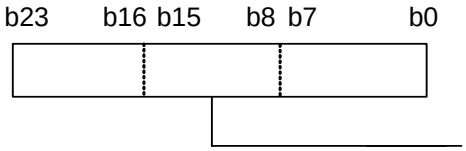
• Set DSA1 register (DMA1 SFR address register)



• Set DRA1 register (DMA1 memory address reload register)

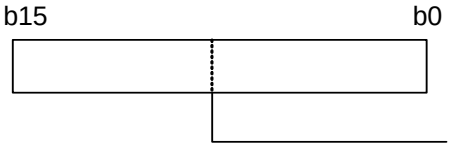


• Set DMA1 register (DMA1 memory address register)



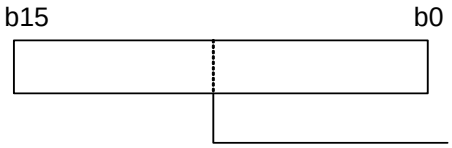
Set address of pulse output data which outputs to ports P2 to P3

• Set DRC1 register (DMA1 transfer count reload register)



Set numbers of pulse output data

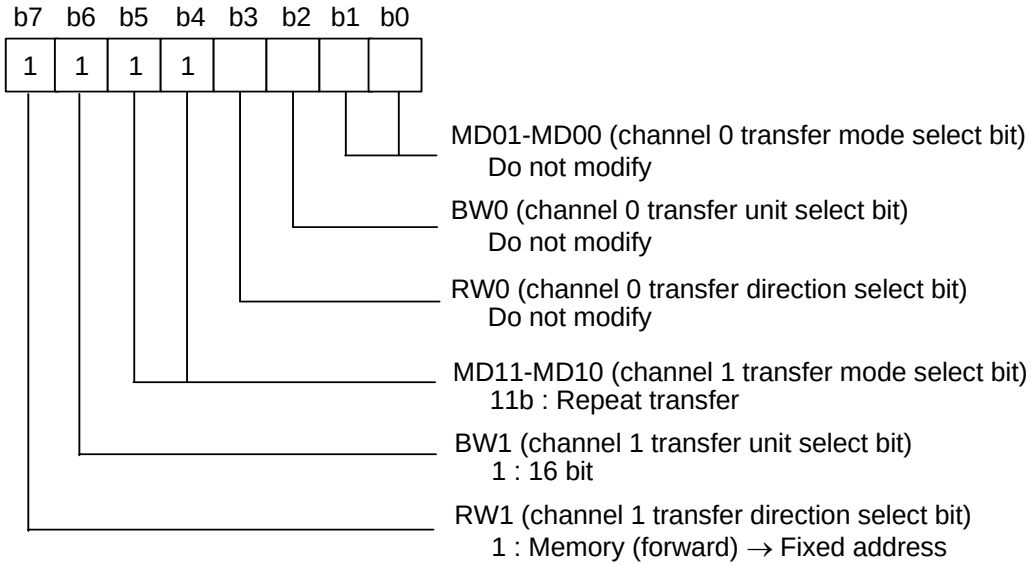
• Set DCT1 register (DMA1 transfer count register)



Set numbers of pulse output data

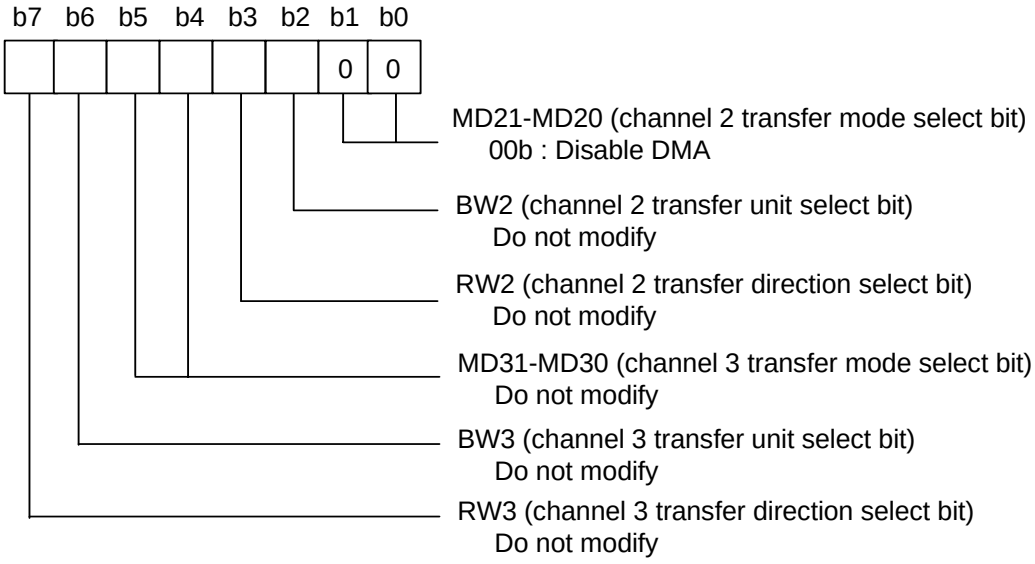
• Insert dummy cycle
Enable DMA after setting the DM1SL register and waiting for 6 cycles by BCLK.
This document shows inserting 6 NOPs waits for 6 cycles.

• Re-set (enable DMA1) DMD0 register (DMA mode register 0)

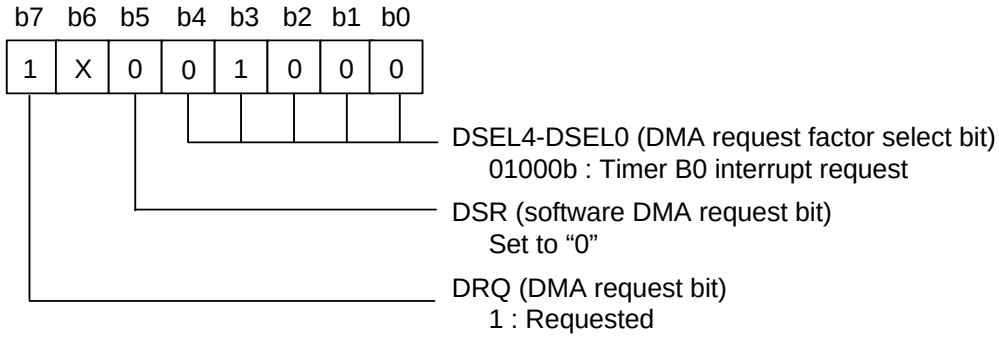


(4) DMA2 setting

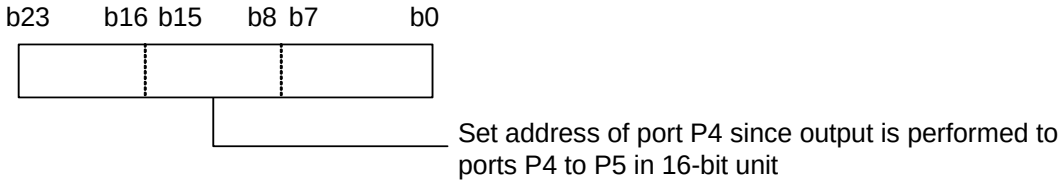
• Set (disable DMA2) DMD1 register (DMA mode register 1)



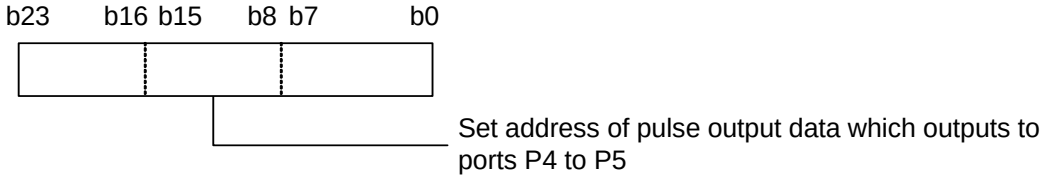
• Set DM2SL register (DMA2 factor select register)



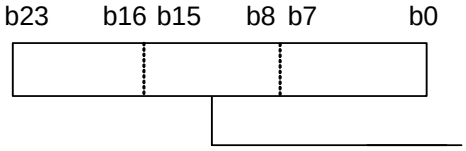
• Set DSA2 register (DMA2 SFR address register)



• Set DRA2 register (DMA2 memory address reload register)

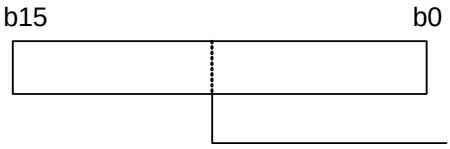


• Set DMA2 register (DMA2 memory address register)



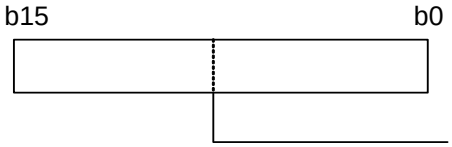
Set address of pulse output data which outputs to ports P4 to P5

• Set DRC2 register (DMA2 transfer count reload register)



Set numbers of pulse output data

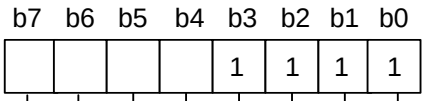
• Set DCT2 register (DMA2 transfer count register)



Set numbers of pulse output data

• Insert dummy cycle
Enable DMA after setting the DM2SL register and waiting for 6 cycles by BCLK.
This document shows inserting 6 NOPs waits for 6 cycles.

• Re-set (enable DMA2) DMD1 register (DMA mode register 1)



MD21-MD20 (channel 2 transfer mode select bit)
11b : Repeat transfer

BW2 (channel 2 transfer unit select bit)
1 : 16 bit

RW2 (channel 2 transfer direction select bit)
1 : Memory (forward) → Fixed address

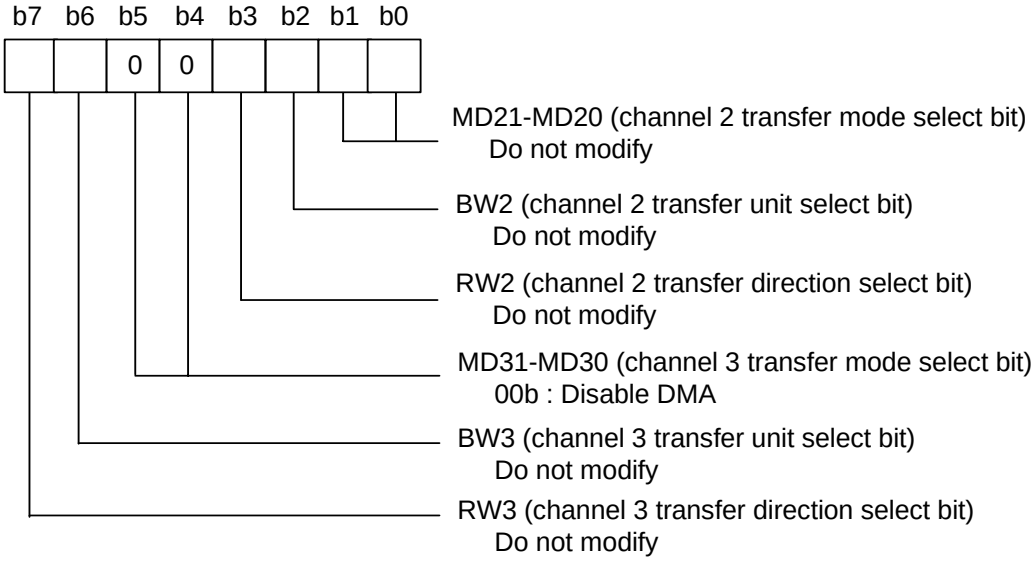
MD31-MD30 (channel 3 transfer mode select bit)
Do not modify

BW3 (channel 3 transfer unit select bit)
Do not modify

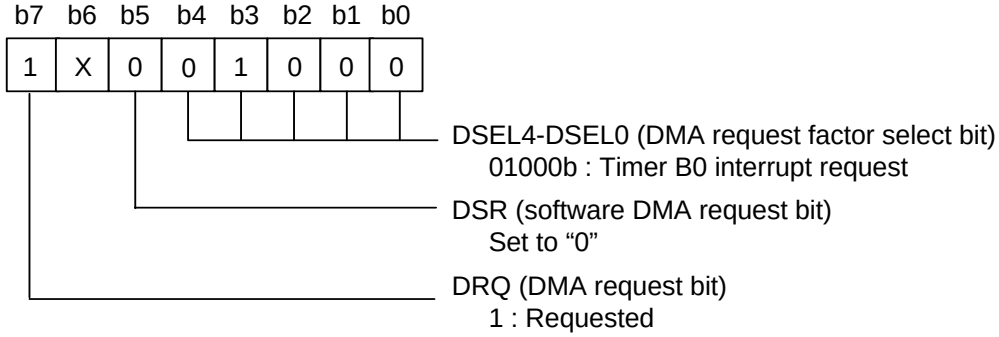
RW3 (channel 3 transfer direction select bit)
Do not modify

(5) DMA 3 setting

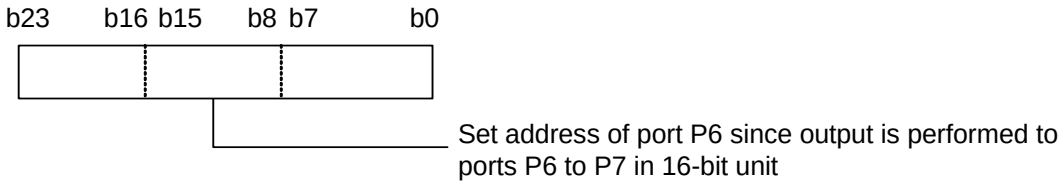
• Set (disable DMA3) DMD1 register (DMA mode register 1)



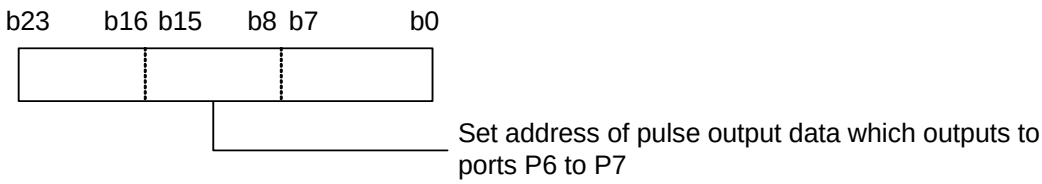
• Set DM3SL register (DMA3 factor select register)



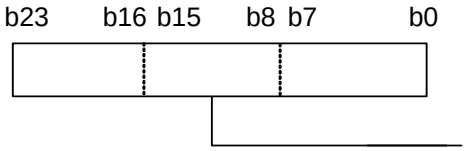
• Set DSA3 register (DMA3 SFR address register)



• Set DRA3 register (DMA3 memory address reload register)

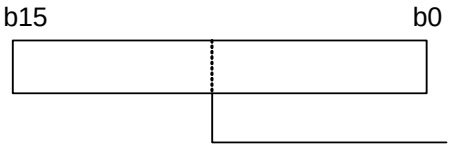


• Set DMA3 register (DMA3 memory address register)



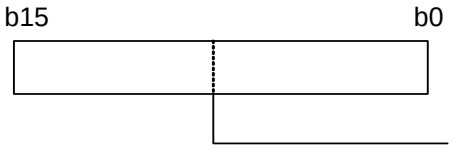
Set address of pulse output data which outputs to ports P6 to P7

• Set DRC3 register (DMA3 transfer count reload register)



Set numbers of pulse output data

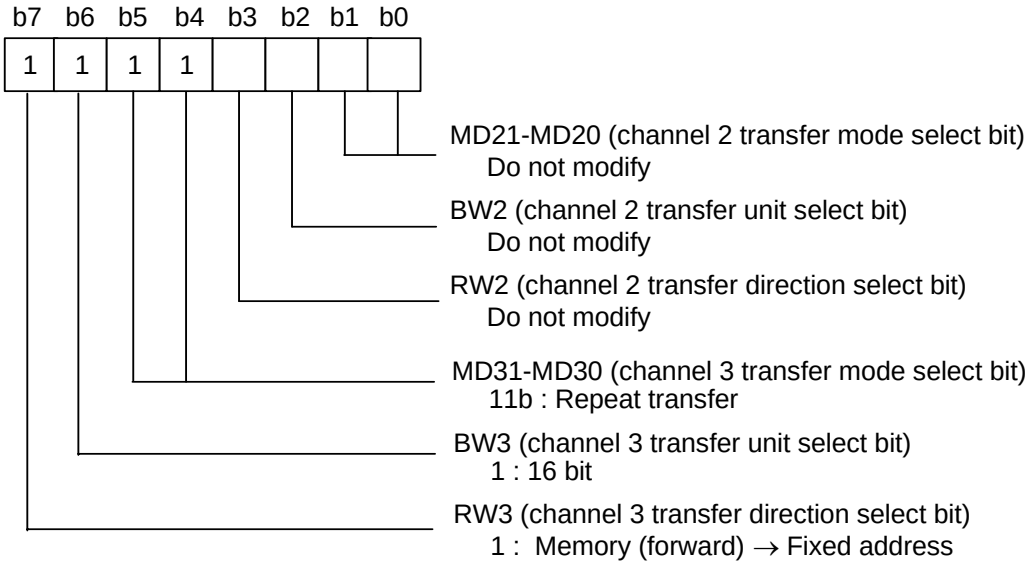
• Set DCT3 register (DMA3 transfer count register)



Set numbers of pulse output data

• Insert dummy cycle
Enable DMA after setting the DM3SL register and waiting for 6 cycles by BCLK.
This document shows inserting 6 NOPs waits for 6 cycles.

• Re-set (enable DMA3) DMD1 register (DMA mode register 1)



(6) Set a port for PWM output to an output port

• Set default value to P0 to P7 registers

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0

Pi_j (i=0 to 7, j=0 to 7) (Port Pi_j bit)
0 : Output "L" as default value

• Set to output port in PD0 to PD7 registers (port PD0 to PD7 direction register)

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1	1	1	1

PDi_j (i=0 to 7, j=0 to 7) (Port Pi_j direction bit)
1 : Output mode

(7) Set an interrupt to enable (I flag = "1")

(8) Timer B0 starts

• Set TABSR register (count start flag)

b7	b6	b5	b4	b3	b2	b1	b0
		1					

TB0S (Timer B0 count start flag)
1 : Timer B0 count starts

(9) Timer B0 interrupt process
Modify the value in the TB0 register (Timer B0 register) to modify PWM pulse output width.

4. Reference Program

A program example which performs 64 PWM outputs between 100µs to 900µs period using Timer B0 and DMA0 to 3 is shown as follows.

Operation condition : VCC1=VCC2=5.0V, XIN=8MHz, PLL=quadruple, f1=32MHz

```
/***********************************************************************/
/*                                                                     */
/*  M32C/85 Group Program Collection                                   */
/*                                                                     */
/*  FILE NAME : rjj05b0579_src.c                                       */
/*  CPU       : M32C/85 Group                                          */
/*  FUNCTION  : The sample program of the 64ch multiplex PWM output    */
/*            using DMAC.                                              */
/*  HISTORY   : 2004.09.15 Ver 1.00                                    */
/*                                                                     */
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/*                                                                     */
/***********************************************************************/

/*****************************************/
/*    include file                       */
/*****************************************/
#include "sfr32c8586.h"     // Special Function Register Header File

/*****************************************/
/*    Function declaration               */
/*****************************************/
void tb0_int(void);         // TB0 interrupt routine

/*****************************************/
/*    Global variable declaration        */
/*****************************************/
                    // PWM ch0-ch15 output data.
const unsigned short     pwm0_data[8] =
      {0x0101, 0x0202, 0x0404, 0x0808, 0x1010, 0x2020, 0x4040, 0x8080 };
const unsigned short     pwm1_data[8] =
      {0x0303, 0x0606, 0x0c0c, 0x1818, 0x3030, 0x6060, 0xc0c0, 0x8181 };
const unsigned short     pwm2_data[8] =
      {0x0707, 0x0e0e, 0x1c1c, 0x3838, 0x7070, 0xe0e0, 0xc1c1, 0x8383 };
const unsigned short     pwm3_data[8] =
      {0x0f0f, 0x1e1e, 0x3c3c, 0x7878, 0xf0f0, 0xe1e1, 0xc3c3, 0x8787 };

unsigned short           tb_value;      // TB0 current value

/*****************************************/
/*    #define declaration                */
/*****************************************/
#define TB_INI_VALUE    3200-1   // TB0 initial value
#define TB_MAX_VALUE    32000-1  // TB0 maximum value
#define TB_UP_VALUE     3200     // TB0 incremental value

/*****************************************/
/*    DMAC register declaration          */
/*****************************************/
```

```
                        // CPU internal registor
unsigned short  dmd0;
#pragma DMAC    dmd0    DMD0    // DMD0(DMA mode register0)
unsigned short  dct0;
#pragma DMAC    dct0    DCT0    // DCT0(DMA0 transfer count register)
unsigned short  drc0;
#pragma DMAC    drc0    DRC0    // DRC0(DMA0 transfer count reload register)
void _far       *dma0;
#pragma DMAC    dma0    DMA0    // DMA0(DMA0 memory address register)
void _far       *dsa0;
#pragma DMAC    dsa0    DSA0    // DSA0(DMA0 SFR address register)
void _far       *dra0;
#pragma DMAC    dra0    DRA0    // DRA0(DMA0 memory address reload register)

unsigned short  dmd1;
#pragma DMAC    dmd1    DMD1    // DMD1(DMA mode register1)
unsigned short  dct1;
#pragma DMAC    dct1    DCT1    // DCT1(DMA1 transfer count register)
unsigned short  drc1;
#pragma DMAC    drc1    DRC1    // DRC1(DMA1 transfer count reload register)
void _far       *dma1;
#pragma DMAC    dma1    DMA1    // DMA1(DMA1 memory address register)
void _far       *dsa1;
#pragma DMAC    dsa1    DSA1    // DSA1(DMA1 SFR address register)
void _far       *dra1;
#pragma DMAC    dra1    DRA1    // DRA1(DMA1 memory address reload register)

/*************************************/
/*    SFR declaration                */
/*************************************/
#pragma ADDRESS     plc0_w      0026H   // PLL control register 0 & 1
unsigned short      plc0_w;

/*****************************************/
/*    Main Program                       */
/*****************************************/
void main(void)
{
   short   dmd0_tmp;                // DMD0 register temp
   short   dmd1_tmp;                // DMD1 register temp
   short   pll_wait;                // PLL wait counter

   prcr = 3;
   plc0_w = 0x0254;                  // PLL clock = Main clock x4.
   plc0   = 0xd4;                   // Start PLL.
                            // It waits until a PLL clock is stabilized.
   for (pll_wait=0;pll_wait<4500;pll_wait++);
   cm17 = 1;                        // Main clock = PLL clock.
   mcd = 0x12;                       // Set main-clock no division mode.
   prcr = 0;

   // A setup a TB0(For DMA request cause).
   tb0mr = 0x00;                     // Set TB0MR register.
                            //  <TMOD1-0> : timer mode
                            //  <TCK1-0>  : f1

   tb_value = TB_INI_VALUE;
   tb0 = tb_value;                  // Set TB0 register.
```

```
                        //  Pulse output cycle=1ms(XIN=32MHz)

tb0ic = 6;                  // Set TB0 interrupt priority level = 6.

// A setup of DMA0.
dmd0_tmp =  dmd0;               // DMA0 inhibit(DMD0)
dmd0_tmp &= 0x00fc;               //  <MD01-00> : DMA0 inhibit
dmd0     =  dmd0_tmp;             //

dm0sl = 0x88;                   // Set DM0SL register.
                        //  <DSEL4-0> : TB0
                        //  <DRQ>     : DMA requested

dsa0  = &p0;                    // Set DSA0 register.
dma0  = &pwm0_data[0];            // Set DMA0 register.
dra0  = &pwm0_data[0];            // Set DRA0 register.
dct0  = 8;                  // Set DCT0 register.
drc0  = 8;                  // Set DRC0 register.
                        // Dummy cycle insertion
asm("NOP    ");                 //  It waits by 6 cycles by BCLK.
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");

dmd0_tmp |= 0x0f;               // DMA0 permission(DMD0)
                        //  <MD01-00> : repeat transfer
                        //  <BW0>     : 16bit
                        //  <RW0>     : Memory to Fixed address
dmd0     = dmd0_tmp;

// A setup of DMA1.
dmd0_tmp =  dmd0;               // DMA1 inhibit(DMD0)
dmd0_tmp &= 0x00cf;               //  <MD11-10> : DMA1 inhibit
dmd0     =  dmd0_tmp;             //

dm1sl = 0x88;                   // Set DM1SL register.
                        //  <DSEL4-0> : TB0
                        //  <DRQ>     : DMA requested

dsa1  = &p2;                    // Set DSA1 register.
dma1  = &pwm1_data[0];            // Set DMA1 register.
dra1  = &pwm1_data[0];            // Set DRA1 register.
dct1  = 8;                  // Set DCT1 register.
drc1  = 8;                  // Set DRC1 register.
                        // Dummy cycle insertion
asm("NOP    ");                 //   It waits by 6 cycles by BCLK.
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");

dmd0_tmp |= 0xf0;               // DMA1 permission(DMD0)
                        //  <MD11-10> : repeat transfer
                        //  <BW1>     : 16bit
                        //  <RW1>     : Memory to Fixed address
```

```
dmd0     = dmd0_tmp;

// (3) A setup of DMA2.
dmd1_tmp =  dmd1;               // DMA2 inhibit(DMD1)
dmd1_tmp &= 0x00fc;               //  <MD21-20> : DMA2 inhibit
dmd1     =  dmd1_tmp;           //


asm("mov.b  #088h, _dm2sl_addr");   // Set DM2SL register.
                        //  <DSEL4-0> : TB0
                        //  <DRQ>     : DMA requested
asm("fclr   I");                // Interrupt disabled.
asm("fset   B");                // Register-bank1 enable
asm("ldc    #_p4_addr, sb");        // Set DSA2(SB) regisster.
asm("ldc    #_pwm2_data, svp");     // Set DRA2(SVP) register.
asm("mov.l  #_pwm2_data, a0");      // Set DMA2(A0) register.
asm("mov.w  #8, r2");               // Set DRC2(R2) register.
asm("mov.w  #8, r0");               // Set DCT2(R0) register.
asm("fclr   B");                // Register-bank1 disable
                        // Dummy cycle insertion
asm("NOP    ");                 //   It waits by 6 cycles by BCLK.
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");

dmd1_tmp |= 0x0f;               // DMA2 permission(DMD1)
                        //  <MD21-20> : repeat transfer
                        //  <BW0>     : 16bit
                        //  <RW0>     : Memory to Fixed address
dmd1     = dmd1_tmp;


// (4) A setup of DMA3.
dmd1_tmp =  dmd1;               // DMA3 inhibit(DMD1)
dmd1_tmp &= 0x00cf;               //  <MD31-30> : DMA3 inhibit
dmd1     =  dmd1_tmp;           //


asm("mov.b  #088h, _dm3sl_addr");   // A setup of DM3SL(DRQ=1, TA1)
                        //  <DSEL4-0> : TB0
                        //  <DRQ>     : DMA requested
asm("fclr   I");                // Interrupt disabled.
asm("fset   B");                // Register-bank1 enable
asm("ldc    #_p6_addr, fb");        // Set DSA3(FB) register.
asm("ldc    #_pwm3_data, vct");     // Set DRA3(VCT) register.
asm("mov.l  #_pwm3_data, a1");      // Set DMA3(A1) register.
asm("mov.w  #8, r3");               // Set DRC3(R3) register.
asm("mov.w  #8, r1");               // Set DCT3(R1) register.
asm("fclr   B");                // Register-bank1 disable
                        // Dummy cycle insertion
asm("NOP    ");                 //   It waits by 6 cycles by BCLK.
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
asm("NOP    ");
```

```
    dmd1_tmp |= 0xf0;                   // DMA3 permission(DMD1)
                                //  <MD11-10> : repeat transfer
                                //  <BW1>     : 16bit
                                //  <RW1>     : Memory to Fixed address
    dmd1      = dmd1_tmp;

    // A setup a Port(For PWM output).
    p0  = 0;
    p1  = 0;
    p2  = 0;
    p3  = 0;
    p4  = 0;
    p5  = 0;
    p6  = 0;
    p7  = 0;
    pd0 = 0xff;                     // P0 is output port.
    pd1 = 0xff;                     // P1 is output port.
    pd2 = 0xff;                     // P2 is output port.
    pd3 = 0xff;                     // P3 is output port.
    pd4 = 0xff;                     // P4 is output port.
    pd5 = 0xff;                     // P5 is output port.
    pd6 = 0xff;                     // P6 is output port.
    pd7 = 0xff;                     // P7 is output port.

    asm("fset i");                  // Interrupt enabled.

    tb0s = 1;                       // TB0 start.

    while(1);

}

/****************************************/
/*  TB0 interrupt routine               */
/****************************************/
#pragma INTERRUPT/B tb0_int
// "/B" = Instead of saving the registers to the stack,
//        you can switch to the alternate registers.

void tb0_int(void)
{
                                // A next timer value is calculated.
    tb_value += TB_UP_VALUE;
    if (tb_value >= TB_MAX_VALUE) tb_value = TB_INI_VALUE;

    tb0 = tb_value;                 // Next timer value set.

}
```

5. Reference Document

Hardware Manual
M32C/85 Group Hardware Manual
Use the latest version on the Renesas Technology Corporation Semiconductor Home Page

6. Home Page and E-mail Support

Renesas Technology Corporation Semiconductor Home Page
http://www.renesas.com

M16C Family MCU Technical E-mail Support
E-mail: support_apl@renesas.com

REVISION HISTORY	M32C/85 Group Application Example of Multiple-Channel PWM Using DMAC

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