

TCM38C17 Quad Combo Interface to HC55181 and HC5503

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Introduction

The TCM38C17 is a four-channel PCM combo. The term combo implies a CODEC and filters. This means that in addition to the ADC and DAC, the antialiasing filter and the smoothing filters are also on the chip. The TCM38C17 complies with CCITT/(D3/D4) G.711 and G.714 Channel Bank Specifications. [1] Figure 1 shows the block diagram of a single TCM38C17 channel.

The TCM38C17 uses sigma-delta converter technology and provides the option of selecting A-Law or μ -Law companding. It has a single PCM I/O for a simplified PCM interface. Each channel can interface a full-duplex, 4-line voice telephone circuit with a time-division-multiplexed system. The crosstalk between channels is less than -100dB, which means that the TCM38C17 saves board space without any crosstalk. The TCM38C17 provides 8V_{P-P} full-signal differential receiver output.

These parts typically are used in line card applications. The major components on a line card include a combo, SLIC, microcontroller, voltage regulators, and transient voltage suppressors. The SLIC, in addition to other things, converts the analog signal from two-wire to four-wire and vice-versa. In this process, some of the signal applied at the receive

channel of the SLIC appears at the transmit channel, deteriorating voice quality. This would result in the person hearing his own voice back through the handset. To reduce this effect, a transhybrid balance circuit is used between the combo and the SLIC. The transhybrid balance circuitry given below provides some degree of isolation, but for better performance, the transhybrid must include op amps.

TCM38C17 Interface to the HC5503 SLIC

This section gives details on interfacing the TCM38C17 with HC5503 SLIC. The test setup consists of:

- HC5503 SLIC Evaluation Board
- TCM38C17 Test Board
- Bread board to implement the transhybrid circuitry

Figure 2 shows the test setup to measure how much of the signal appears at test point 3 when a signal is applied at test point 2.

The transhybrid circuitry given does not use an op amp. Instead, it consists only of resistors and capacitors. The amplifier forms the input stage of the TCM38C17. Some of the specifications of this amplifier are given in Table A-1 in the Appendix.

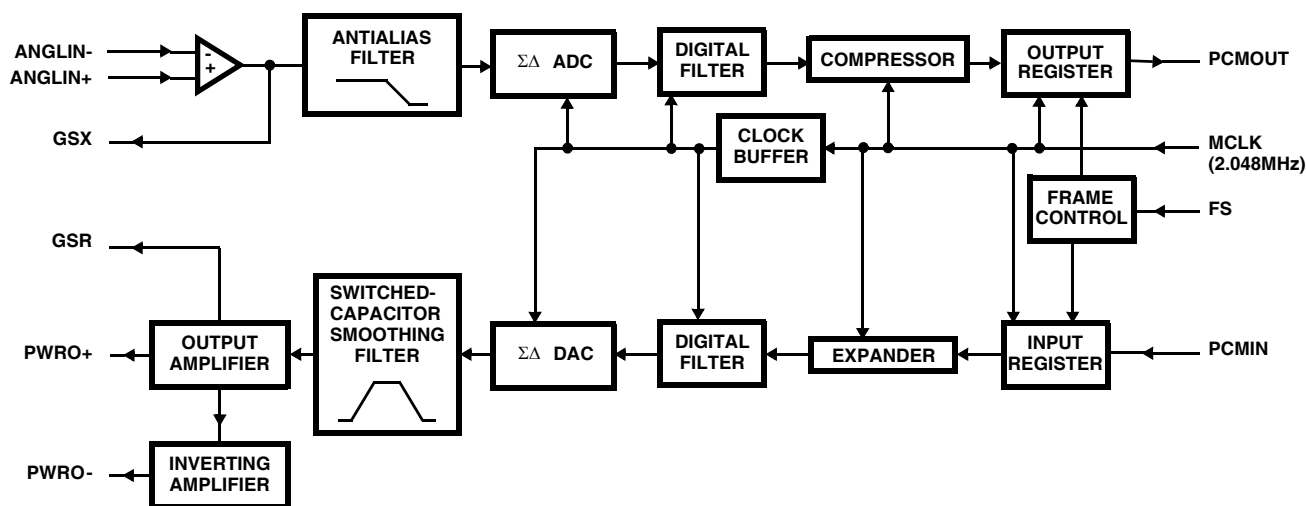


FIGURE 1. BLOCK DIAGRAM OF A TCM38C17 CHANNEL

Figure 3 shows the interface between one channel of the TCM38C17 and the Intersil HC5503 SLIC.

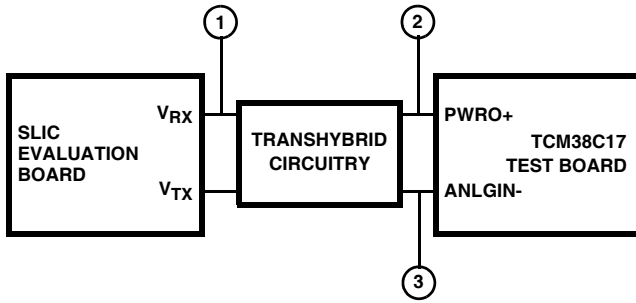


FIGURE 2. TEST SETUP

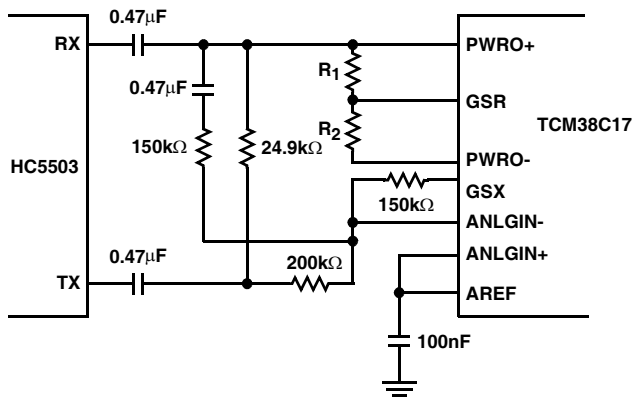


FIGURE 3. QCOMBO INTERFACE TO THE INTERSIL 5503 SLIC

The transhybrid circuit works due to the inversion of the signal from the receive port to the transmit port. The voltage at R_X is negative of the TX, so if the currents at the two ports are the same, then the input signal could be removed from the output signal. The resistors R_1 and R_2 can be changed to adjust the gain, which is given by the following equation:

$$A = \frac{R_1 + R_2}{4 \left(R_2 + \frac{R_1}{4} \right)} \quad (\text{EQ. 1})$$

The input and output gain adjustment are discussed in detail in PCM CODEC/Filter Combo Family: Device Design-In and Application Data.[2] Figure 3 shows the TCM38C17's output used in the single-ended configuration. The analog input gain can be fixed simply by using the feedback loop through GSX. The AREF pin provides a reference voltage of 2.375V that is connected to ANLGIN+ for bias.

Using the configuration in Figure 3, the transhybrid loss was calculated, using the formula: transhybrid loss = $20 \times \log(V_O/1V_{RMS})$, where V_O is the voltage at test point 3. The data was gathered by measuring the output at different frequencies in the voice band range. A $1V_{RMS}$ signal was applied at test point 2. The results are given in Table 1.

TABLE 1. TRANSHYBRID LOSS CALCULATION FOR HC5503

FREQUENCY (Hz)	TEST POINT 3 (V_{AC})	TRANSHYBRID LOSS (dB)
400	0.026	-31.7
800	0.014	-37.1
1200	0.012	-38.4
1600	0.010	-40
2000	0.009	-40.9
2400	0.009	-40.9
2800	0.008	-41.9
3200	0.008	-41.9
3600	0.008	-41.9

Without the transhybrid circuitry, the signal that is fed into the receive pin of the SLIC appears at the transmit pin. To check the whole loop, a 1kHz, $1V_{RMS}$ signal was applied at the receive pin of the SLIC and the transhybrid circuit was removed. The signal appears at the transmit pin, which is connected to the analog input of the TCM38C17; using digital loop back, the analog output at the PWRO+ pin was observed. This configuration is shown in Figure 4.

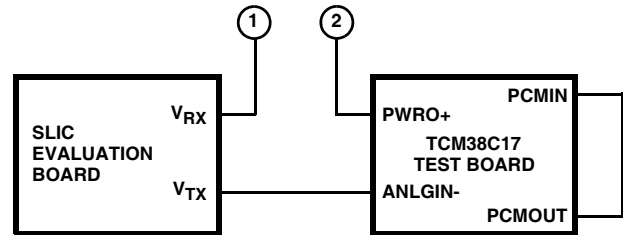


FIGURE 4. TEST SETUP WITHOUT TRANSHYBRID CIRCUIT

The scope plot for the setup in Figure 4 at test point 2 is given in Figure 5. To make a comparison, the input signal scope plot and its FFT are provided in the Appendix in Figure A-1. Also in the Appendix (in Figure A-2), is the signal at the PWRO+ pin and its FFT, with a $1V_{RMS}$ signal at the analog input with unity gain setting, and with PCMIN connected to PCMOUT. So Figure A-2 gives the output signal using digital loopback. The Appendix also provides a description on how to read the scope plots.

To test the whole system with the transhybrid balance included, the following configuration was also tested.

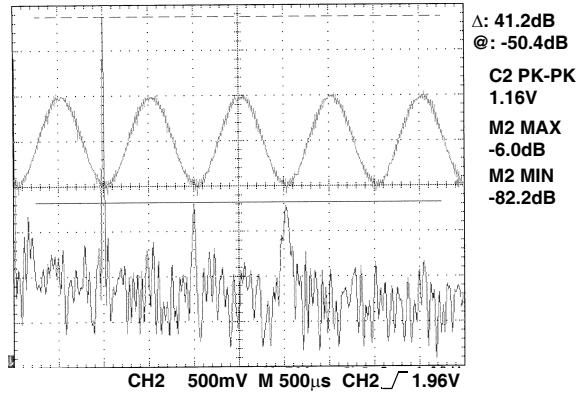


FIGURE 5. SCOPE PLOT FOR THE CONFIGURATION IN FIGURE 4

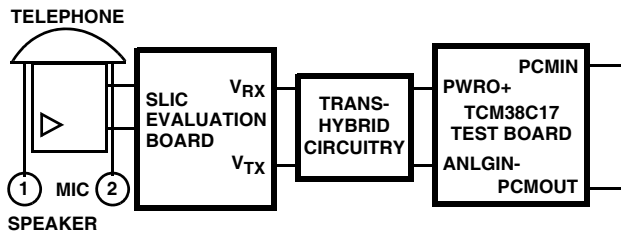


FIGURE 6. TEST SETUP FOR THE COMPLETE SYSTEM

In this case, a 1V_{RMS} signal was applied to the microphone of the telephone (test point 2) and the output was observed at the speaker (test point 1); so the signal goes from the SLIC to the TCM38C17 and back through the transhybrid circuit. Figure 7 gives the scope plot showing the voltage at test point 1.

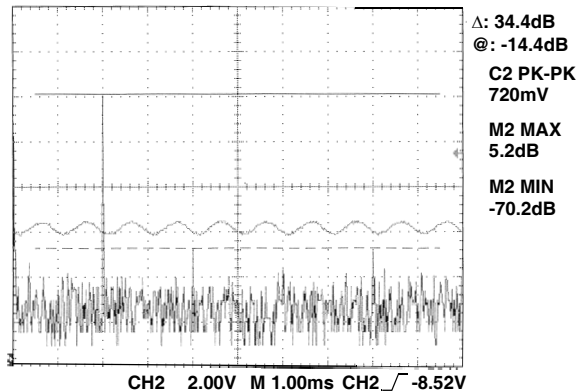


FIGURE 7. SCOPE PLOT FOR THE CONFIGURATION IN FIGURE 6

TCM38C17 Interface to the HC5518 SLIC FAMILY

Figure 8 gives the interface between one channel of the TCM38C17 and the Intersil HC5503 SLIC.

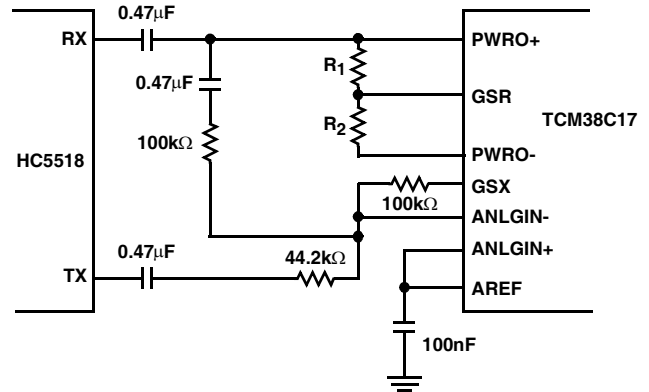


FIGURE 8. QCOMBO INTERFACE TO THE HC5503 SLIC

The same tests done for the HC5503 SLIC were carried out for the HC5518 SLIC. The results, given in Table 2, are based on a test setup similar to that given in Figure 2.

TABLE 2. TRANSYBRID LOSS CALCULATION FOR HC5518

FREQUENCY (Hz)	TEST POINT 3 (V _{AC})	TRANSYBRID LOSS (dB)
400	0.017	-35.4
800	0.010	-40
1200	0.012	-38.4
1600	0.016	-35.9
2000	0.02	-34
2400	0.023	-32.8
2800	0.026	-31.7
3200	0.029	-30.8
3600	0.031	-30.2

Using the HC5518 in the configuration shown in Figure 4, the voltage at test point 2 is as follows:

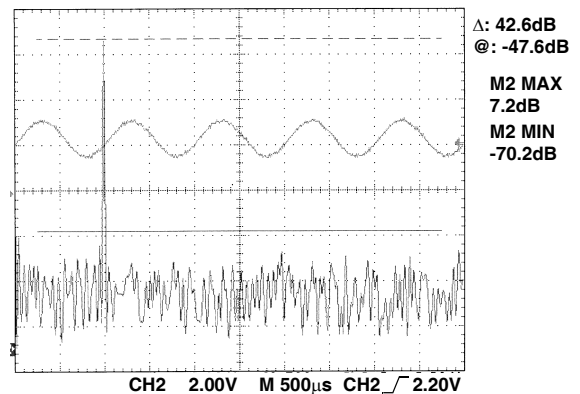


FIGURE 9. SCOPE PLOT FOR THE CONFIGURATION IN FIGURE 4, VOLTAGE AT TEST POINT 2

For the complete system test using the HC5518, the results are given in Figure 10.

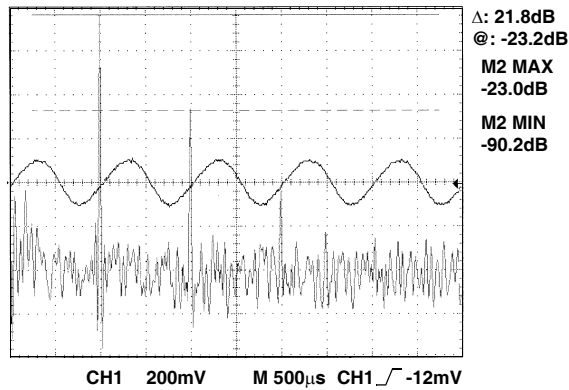


FIGURE 10. SCOPE PLOT FOR THE CONFIGURATION IN FIGURE 6, VOLTAGE AT TEST POINT 2

TIMING ISSUES

Combos are designed to be interfaced to digital PCM telephone networks, which can be of two types. A T1 system operates at a 1.544MHz clock rate and allows for time-division-multiplexing of 24 voiceband channels. The time intervals for a T1 signal are shown in Figure 11. T1 systems are used in the US, Canada, Japan and in parts of some other countries.

On the other hand, an E1 system operates at a 2.048MHz clock rate. An E1 system multiplexes 30 voiceband channels. An E1 frame consists of 32 eight-bit bytes, thirty bytes (channels) of these are used for voice transmission. Figure 12 shows a diagram of a PCM-30 frame. E1 systems are used in countries not listed in the previous paragraph.

All networks tied to the PSTN (public switched telephone network) operate synchronously at the given rate. At a digital end office, where the digital data is converted to analog, this clock is used to generate a frame synchronization pulse train. The frame sync information is used to assign a channel to its time slot within the frame. Up to 24 channels may be separated from the bit stream, based on their bit positions. On the other hand, an E1 system operates at a 2.048MHz clock rate. An E1 system multiplexes 30 voiceband channels. An E1 frame consists of 32 eight-bit bytes, thirty bytes (channels) of these are used for voice transmission. Figure 12 shows a diagram of

a PCM-30 frame. E1 systems are used in countries not listed in the previous paragraph.

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Upon receiving a frame sync, an individual combo will send its eight bits of data at 1.544MHz or 2.048MHz (depending on the system) and then wait through the remaining channels until its turn arrives again. While it waits, it samples the analog signal and converts it to digital data, which waits in the output buffer until the next frame sync.

T1 and E1 frames are 125µs in time duration. The TCM38C17 is more suited to an E1 system. It does not allow dynamic time slot assignment. The device has four separate FS pins for the four channels. The FS signal for the four channels has to be provided according to the timing given in Figure 13.

The TCM38C17 can extract or insert any four channels, which meet the timing requirements, from/to the T1 or E1 bit stream. The four channels are labeled 0, 1, 2, 3 inside the TCM38C17, regardless of the corresponding channel numbers in the T1 or E1 frame.

It is clear from the figure that FS signals for the channels have to be separated by 31.25µs. The MCLK for the TCM38C17 is fixed at 2.048MHz. For a 125µs frame, there are 256 complete cycles of the MCLK. Eight complete cycles of the MCLK are needed to shift the digital data in and out. Hence we have 32 time slots. The 31.25µs gap between the FS signals has 64 MCLK cycles implying 8 time slots. First, due to the limit on the MCLK, the TCM38C17 can be used for an E1 system. Second, the 31.25µs requirements implies that one TCM38C17 can use four time slots in an E1 frame. This means that an optimum solution would be to have eight TCM38C17s on one board, and that would cover the whole E1 frame. This is illustrated in Figure 14.

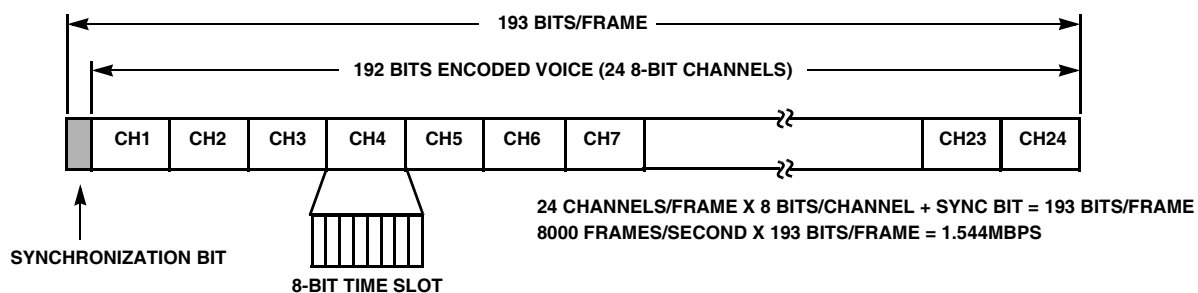


FIGURE 11. A T1 PCM FRAME

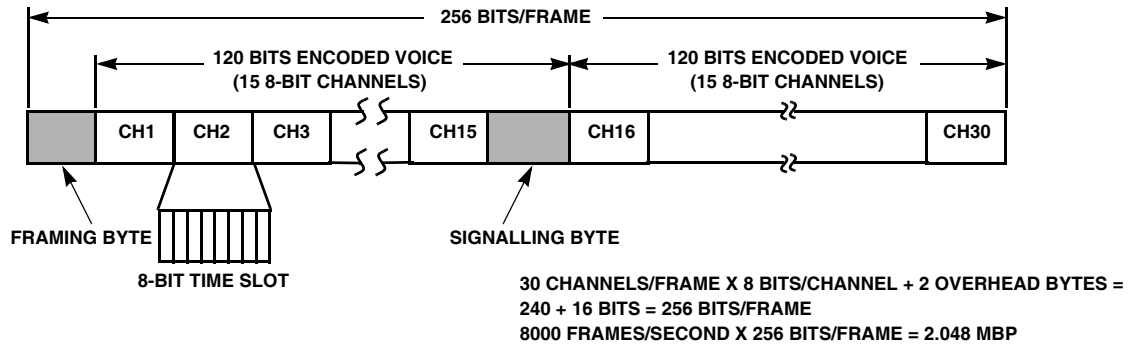


FIGURE 12. AN E1 FRAME

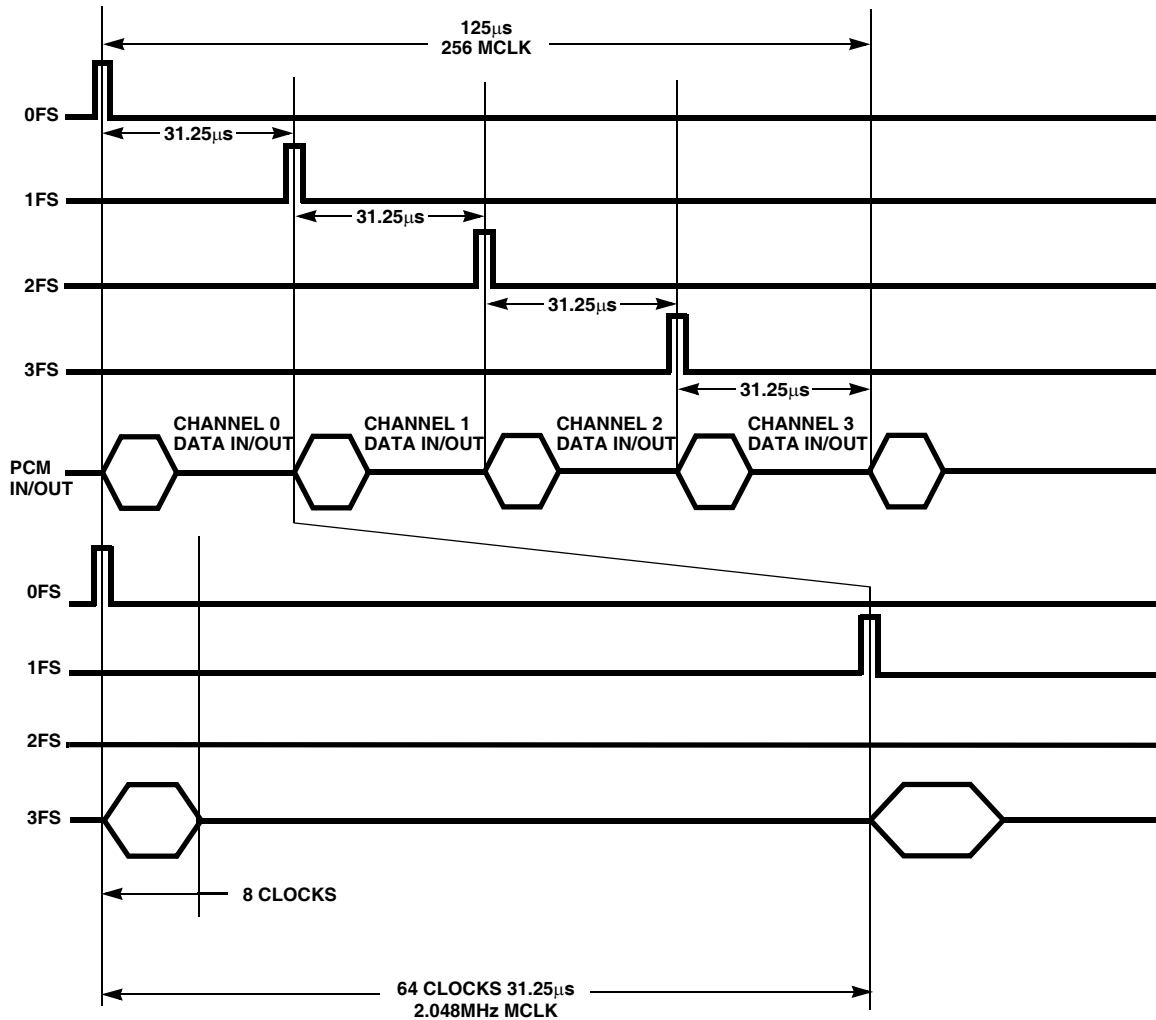


FIGURE 13. FRAME SYNC TIMING

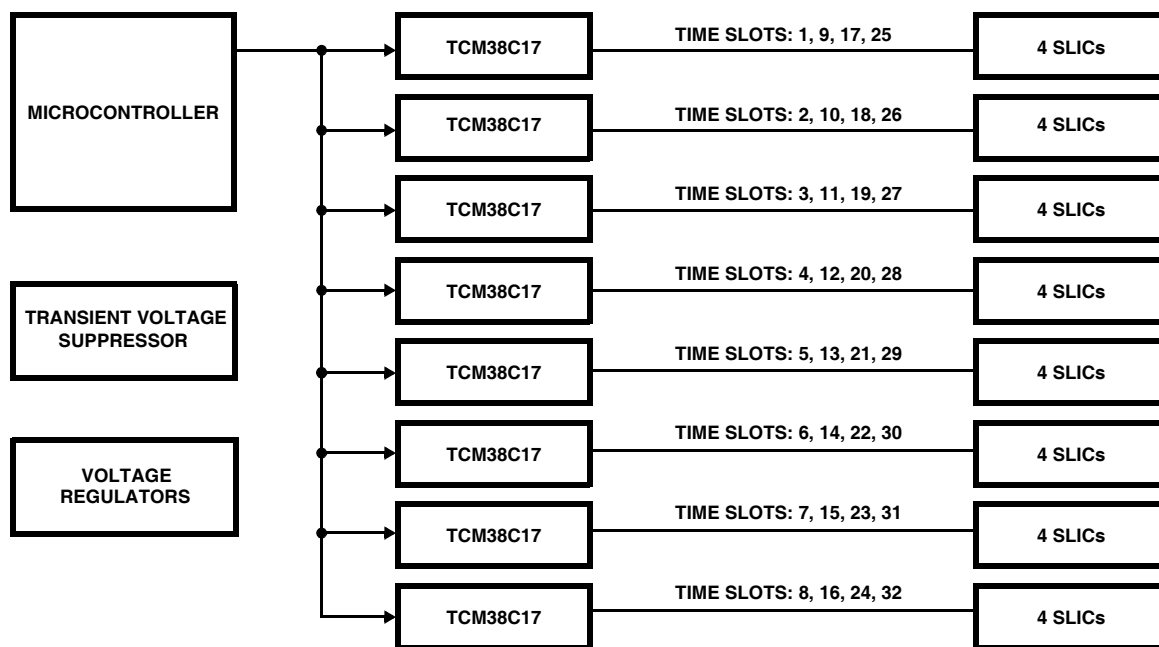


FIGURE 14. BLOCK DIAGRAM OF A CARD FOR E1 APPLICATIONS

Summary

The TCM38C17 is very well suited for line-card applications and can interface with various different types of SLICs. This report gives a brief description of how to interface the TCM38C17 with two different SLICs. It also provides frequency domain plots to give an estimate of the signal compared with the noise. The noise floor can be lowered further with better board design. The noise figures are greater than would be expected because of a microcontroller of the TCM38C17 test board. Active components can also be used in the design of the transhybrid balance to improve its performance further.

References

- [1] CCITT ITU-T G.711, G.712, G.714 Recommendations.
- [2] PCM CODEC/Filter Combo Family: Device Design-In and Application Data, Texas Instruments Incorporated, 1996 (SLWA006).
- [3] Wireless and Telecommunications Products Data Book, Texas Instruments Incorporated, 1996 (SLWD001).
- [4] Understanding Telephone Electronics, Stephen J. Bigelow, SAMS Publishing.
- [5] TCM4207A and TCM29C13 Telephone Line Card Application Report, Texas Instruments Incorporated.
- [6] LSSGR Technical Reference TR-TSY-000064, Section 7, Bell Communications Research.
- [7] AN9736 Application Note, Intersil Corporation, "Operation of the HC5503EVAL Evaluation Board", AnswerFAX Doc. No. 99736.
- [8] AN9813 Application Note, Intersil Corporation, "HC5518XEVAL Evaluation Board User's Guide", AnswerFAX Doc. No. 99813.

About the Author

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Appendix

Performance Data

TABLE A-1. TCM38C17 INPUT AMPLIFIER SPECIFICATIONS

PARAMETER	TX AMPLIFIER			UNIT
	MIN	TYP	MAX	
Input Current at ANLGIN+ and ANLGIN-		± 100		nA
Input Offset Voltage at ANLGIN+ and ANLGIN-		± 5		mV
CMRR at ANLGIN+ and ANLGIN-	55			dB
Open-Loop Voltage Amplification at ANLGIN+ and ANLGIN-	60			dB
Open-Loop Unity-gain Bandwidth at ANLGIN+ and ANLGIN-		900		kHz
Input Resistance at ANLGIN+ and ANLGIN-		1-		M Ω

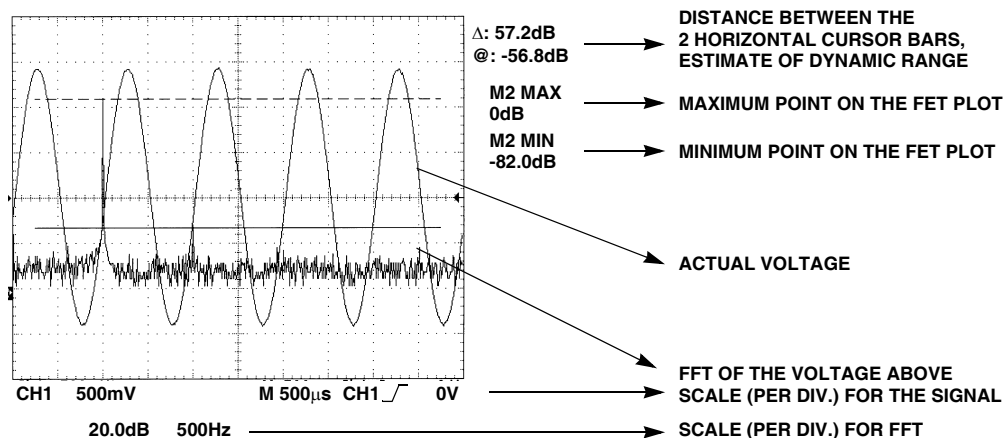


FIGURE A-1. 1V_{RMS} ANALOG INPUT FROM SIGNAL GENERATOR

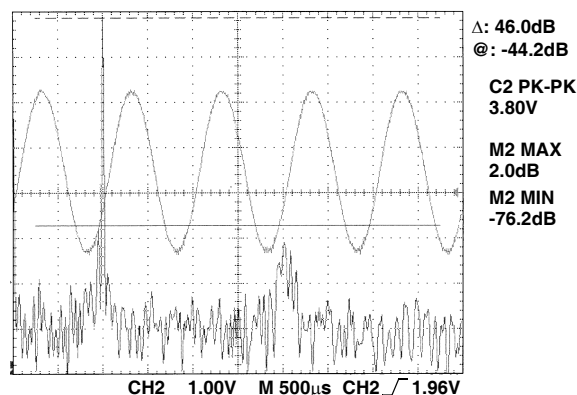


FIGURE A-2. SIGNAL AT PWRO+ PIN, USING DIGITAL LOOPBACK WITH 1V_{RMS} SIGNAL AT THE ANALOG INPUT WITH UNITY GAIN

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