HIP2060, N-Channel Half-Bridge Power MOSFET Array

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Abstract

The HIP2060 is a dual MOSFET array topology in a half-bridge configuration which represents a new innovation of power semiconductor devices that integrates two matched power transistors in a chip. The HIP2060 power MOSFET array is an attractive solution in minimizing the cost, weight, and size of high-volume electronic systems. This application note discusses the design constraints of device construction, package implementation, thermal consideration, and device specification of power MOS topologies. The advantages, classical issues, and circuit application considerations of a power MOS transistor array are also presented.

Introduction

Cost-effectiveness and efficiency in integrating power devices is extremely important when designing low-cost, lightweight and smaller electronic systems. Motivation to integrate multiple discrete devices into a single chip reduces board size and cost. This dual DMOS array design that is internally connected in half-bridge configuration is an example.

The present design philosophy of the power electronics community demands compact, smaller, lightweight and more efficient board utilization. Thus, there is an advantage of power device “array” integration compared to its discrete counterpart. Integrating two or more power devices on a chip has become an economically viable solution to satisfy these demands. Each of the devices in the array is isolated on the chip so there is no need for heat sink isolation. This array concept is very attractive for most applications where multiple power devices are needed.

Accordingly, the internal connection of the device array in the chip is generally dependent on its intended application. A dual N-Channel MOSFET array connected in half-bridge configuration has the advantage of reduced pin count, less PCB premium, reduced EMI due to common grounded (“quite”) heat sink, improved device matching and many more. The half-bridge configuration is very popular in many applications circuits such as motor speed controls, power supplies, voice coil motors, resistive and inductive loads and class D power amplifiers. An example of package implementation and the five-terminal schematic diagram of the half-bridge DMOS array is shown in Figure 1.

There are design subtleties in power DMOS array topologies. There are also constraints on its device construction, package implementation, and device specification. Some inherent characteristics of the device can also affect its overall performance. In addition, electrothermal problems are of great concern when dealing with both low and high power electronics circuits. The HIP2060 power semiconductor device array is designed with these issues in mind and offers solutions to eliminate these concerns and meet the criterion of high quality performance and reliability.

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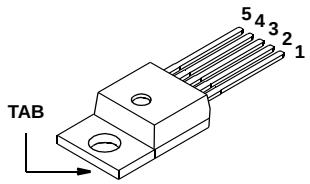

FIGURE 1A.

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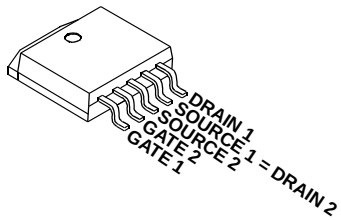


FIGURE 1B.

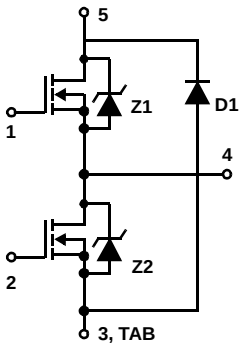


FIGURE 1. HIP2060 POWER MOSFET ARRAY PACKAGE AND HALF-BRIDGE CIRCUIT SCHEMATIC

The HIP2060 power device is rated at maximum continuous drain-to-source current $I_{DS(ON)}$ of 10A and drain-to-source breakdown voltage BV_{DSS} of 60V over operating junction and case temperature range (-40°C to +150°C). Its low $r_{DS(ON)}$ of 0.15Ω (max) at room temperature is well suited for most applications.

MOSFET Device Structure and Parasitic Elements

The device cross section of the quasi-vertical double-diffused metal oxide semiconductor (QVDMOS) cell is shown in Figure 2. A planar contact of the second layer of metal (metal2) is essential to reduce the resistances at the drain and source terminals. The metal2 layer is also needed to support higher current conduction. On the other hand, the second metal layer contributes to the total area of parasitic parallel plate capacitance although not significant because of thick dielectric oxide between the metal1 and metal2 layers. This multi-layer metallization technique is required because the drain and source terminals contact the top surface of the chip.

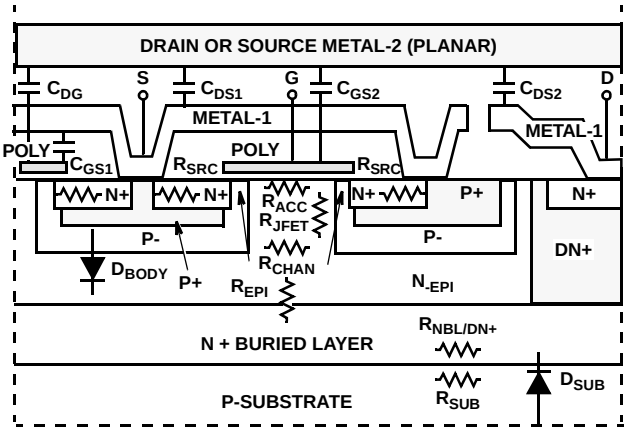


FIGURE 2. CROSS-SECTIONAL VIEW OF QVDMOS TRANSISTOR SHOWING CAPACITANCE, RESISTANCE, AND P-N JUNCTION DIODE ELEMENTS

In Figure 2, most of the area in the "JFET" region (where majority carriers reside) dominates the total resistance of the device at lower voltages. However, at higher voltages, the lightly-doped n-epitaxial region creates a high-resistive path between the drain and source and serves an important function in determining the $r_{DS(ON)}$. The depth and the doping concentration of the epi layer varies directly with its sheet resistivity and B_{VDSS} rating. Each of the different approaches of achieving high voltage capability while maintaining low on-state resistance offer various performance trade-offs that require careful consideration (see Reference 1). For example, to maintain low $r_{DS(ON)}$ while increasing the voltage blocking capability increases the area of the device which also increases the parasitic resistance and capacitance. These parasitic elements limit the ability of the device to turn-on and turn-off at a faster rate. Moreover, raising the breakdown voltage capability causes an increase in the forward voltage drop of power FET which could degrade system efficiency.

Because of the majority-carrier characteristic of MOS field-effect transistors (MOSFET), the switching speed is also affected by the behavior of the electrons in a typical N-Channel device. Device degradation due to hot-electron injection towards the gate oxide along the channel contributes to switching speed limitations and degrades device reliability (see Reference 2). While these factors are inherent to any MOSFET device, the QVDMOS structure has an advantage by minimizing the effect of these parasitic structural elements.

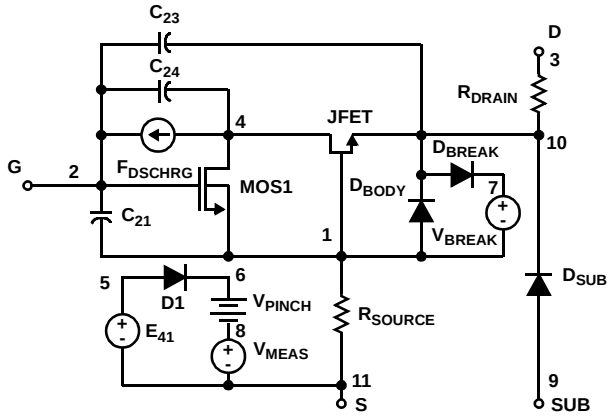
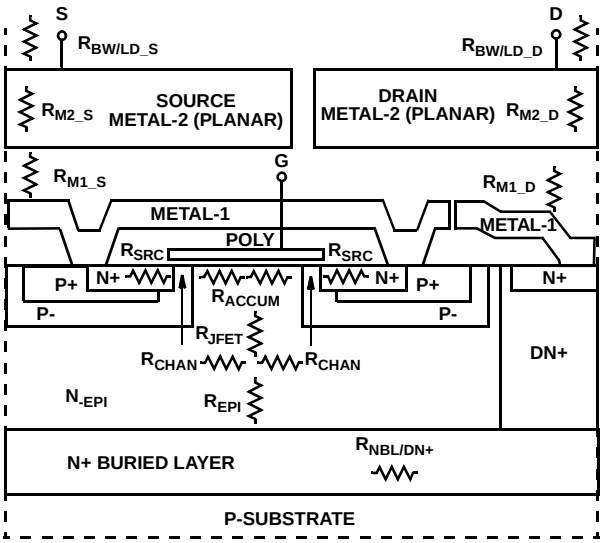


FIGURE 3. QVDMOS SUBCIRCUIT SCHEMATIC



$$r_{DS(ON)} = R_{BW/LD\_S} + R_{M2\_S} + R_{M1\_S} + R_{SRC1,\,2} + R_{CHAN\ 1,2} + R_{JFET} + R_{ACCUM} + R_{EPI} + R_{NBL/DN} + R_{M1\_D} + R_{M2\_D} + R_{SW/LD\_D}$$

NOTES:

R_{M1_D}, R_{M1_S}	=	Metal1 Resistances
R_{M2_D}, R_{M2_S}	=	Metal2 Resistances
R_{SRC}	=	Source N + Resistance
R_{CHAN}	=	Channel Resistance
R_{JFET}	=	J_{FET} Region Resistance
R_{ACCUM}	=	Accumulation Region Resistance
R_{EPI}	=	EPI Resistance
$R_{NBL/DN+}$	=	DN + /N_{BL} Resistance
R_{BW/LD_D}, R_{BW/LD_S}	=	Bondwire and Lead Resistances

FIGURE 4. QVDMOS $r_{DS(ON)}$ COMPONENTS

Composite Device Model

A netlist of PSPICE device model is listed in Appendix A and the subcircuit schematic of the QVDMOS is shown in Figure 3. Each of the two transistors in the half-bridge circuit are modeled

separately as a discrete component and specified in a general form as a composite device or subcircuit. A combination of all the various active elements shown in Figure 2 comprises the subcircuit device model. Basic approaches in modeling power vertical DMOSFET for use in computer-aided design are also discussed in References 3 and 4.The maximum current rating of a power MOSFET is determined by the device on-resistance at specified drain-to-source voltage operating in the linear region, metal interconnect, and bond wire resistance. The total $r_{DS(ON)}$ is the sum of all the resistances between the drain and source terminals (see Figure 4) which varies with applied gate voltage as shown in Figure 5. When assembled in a package, the bondwire and lead resistances are also added to the total resistance calculation. This is important to consider when designing power devices with very low $r_{DS(ON)}$.

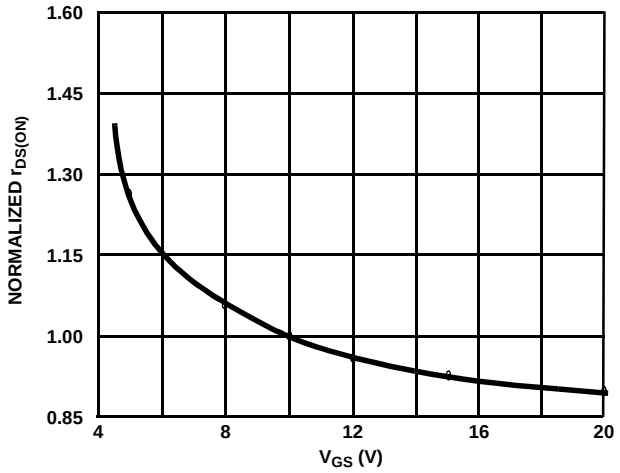


FIGURE 5. $r_{DS(ON)}$ vs V_{GS}

Typical Capacitance Characterization

One of the dynamic characteristics of a power MOSFET that can affect its switching performance is parasitic capacitance. There are three main capacitance parameters of a power MOSFET, namely, gate-to-drain capacitance C_{GD}, gate-to-source capacitance C_{GS}, and drain-to-source capacitance C_{DS}. A combination of these parameters will determine the typical input and output capacitance parameters C_{ISS}, C_{OSS}, and C_{RSS}. The test circuit used for C_{ISS} measurement is shown in Figure 6A. During test, the drain-to-source voltage V_{DS} is swept from 0V to 60V with gate-to-source voltage V_{GS} set to zero. For a high-speed switching device, the measurement is done at a test frequency of 1MHz with a precision multi-frequency capacitance meter (HP4175 LCR Meter). To ensure accuracy, the test equipment is carefully calibrated before actual measurement is taken. The test is performed using packaged product so that measured capacitance includes package parasitics.

In Figure 6A, resistor R1 serves as a bleeder to provide a very high impedance DC path from gate to source. Capacitor C1 is used to cancel the alternating current (AC) that may be generated from drain to gate due to Miller effect. On the other hand, capacitor C1 will also provide a closed path or “AC short” between the drain and source terminals. The common-source input capacitance (C_{ISS}) is the sum of C_{GS} and C_{GD} as in Equation 1.

$$C_{ISS} = C_{GS} + C_{GD} \quad \text{(EQ.1)}$$

The gate and source terminals are short-circuited when measuring the common-source output capacitance (C_{OSS}) as shown in Figure 6B. Resistors R1 and R2 combines a total series resistance of 1MΩ that serves to block any AC signal

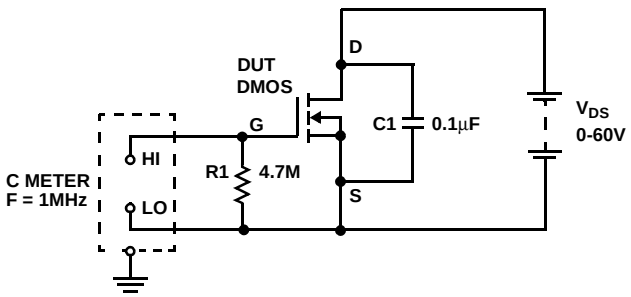


FIGURE 6A. TYPICAL CAPACITANCE TEST CIRCUIT FOR C_{ISS}

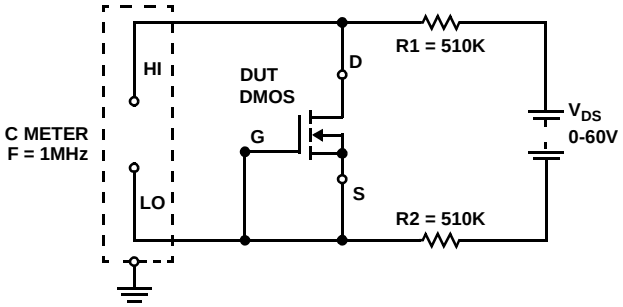


FIGURE 6B. TYPICAL CAPACITANCE TEST CIRCUIT FOR C_{OSS}

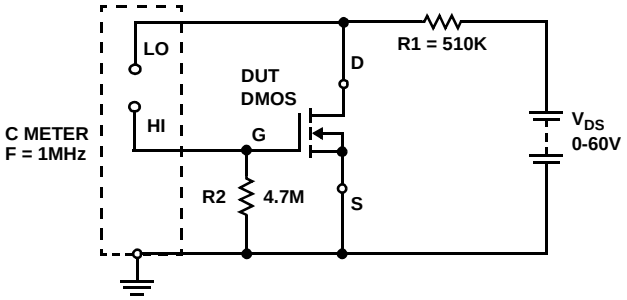


FIGURE 6C. TYPICAL CAPACITANCE TEST CIRCUIT FOR C_{RSS}

FIGURE 6.

that may drift from the capacitance meter towards the power supply, V_{DS}. C_{OSS} is equal to the sum of C_{DS} and C_{GD}.

$$C_{OSS} = C_{DS} + C_{GD} \quad \text{(EQ.2)}$$

The common-source reverse transfer capacitance (C_{RSS}) is extracted using the test circuit in Figure 6C. C_{RSS} is equal to the gate-to-drain capacitance, C_{GD}.

$$C_{RSS} = C_{GD} \quad \text{(EQ. 3)}$$

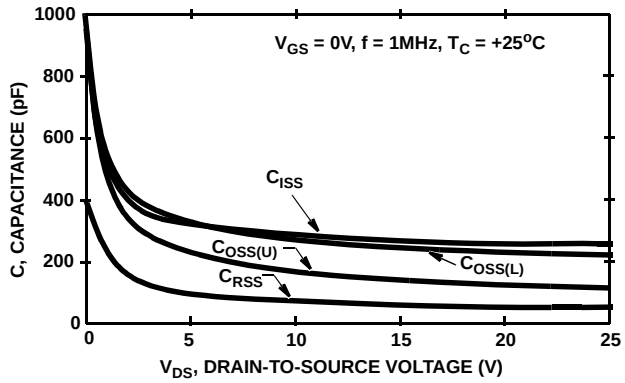


FIGURE 7. TYPICAL HIP2060 CAPACITANCE vs VOLTAGE

The compact design of the QVDMOS produces a very small device area, therefore resulting in less input capacitance. Figure 7 shows the typical capacitance versus drain-to-source voltage characteristics. The lower device exhibits higher output capacitance because of the addition of drain-to-substrate capacitance, hence, two output capacitances are specified in Figure 7 as $C_{OSS(U)}$ and $C_{OSS(L)}$ for upper and lower devices, respectively.

Gate Charge

Another dynamic characteristic of a power MOSFET is its gate charge. This parameter is listed in the data sheet to aid the system designer in determining the amount of current needed to charge and discharge the gate so that appropriate gate drive circuitry can be established. Figures 8A and 8B represent the basic waveform and test circuit for the gate charge measurement. The total gate charge Q_G (equal to gate current (I_{GS}) multiplied by time (t) is generally dependent on the gate bias voltage applied. In this example, $Q_{G(TOT)}$ is extracted at V_{GS} = 10V. A constant current I_{GS} of 7mA is applied to the gate of DUT (Device Under Test) and the gate voltage is recorded using an oscilloscope. A junction FET (JFET) device (not shown) with its drain tied to high potential with respect to the gate and source can be used to produce a constant gate-to-source current I_{GS} as desired. The current regulator in the test circuit is used to control the amount of drain current flowing in the DUT. The drain-to-source constant voltage V_{DS} varies from 20V to 50V. A compact test setup using very short wires should be done in order to prevent any stray inductance to cause overvoltage stress of the DUT. Undesirably large stray inductance can also cause ringing during test.

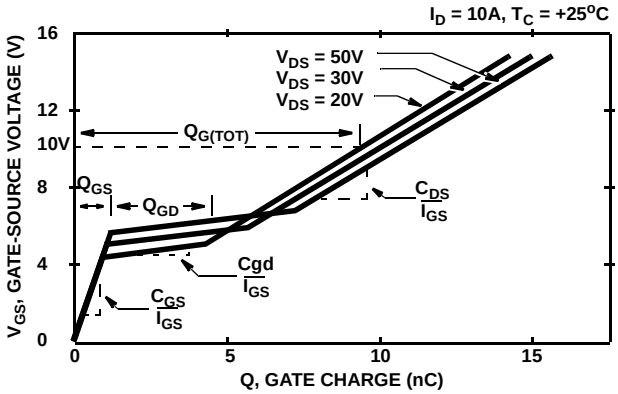


FIGURE 8A. BASIC GATE CHARGE WAVEFORM

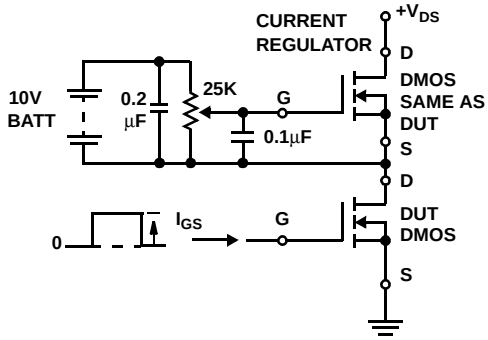


FIGURE 8B. GATE CHARGE TEST CIRCUIT

FIGURE 8.

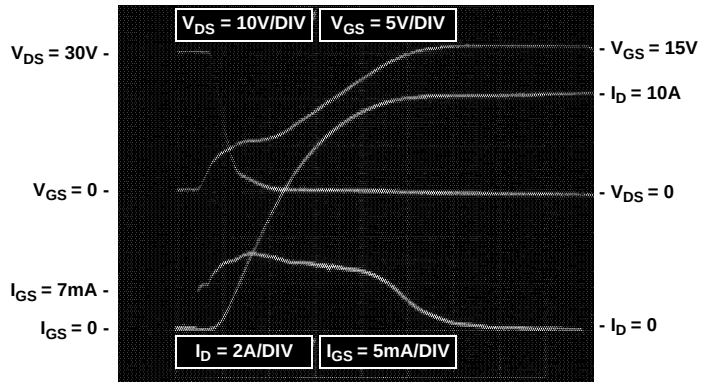


FIGURE 9. TYPICAL HIP2060 GATE CHARGE WAVEFORMS TIME = 500ns/DIV

Measured gate-to-source voltage versus gate charge data using the test circuit in Figure 8B is shown in Figure 9. At specified gate bias, the HIP2060 exhibits a very low gate charge primarily because of considerably small active area of the chip. This characteristic is very desirable for high speed switching applications.

Device Ruggedness and SOA

Unlike the bipolar junction transistor, MOSFETs that are fabricated using robust design methodology do not experience a second breakdown mechanism which usually causes premature device failure. Generally, MOS power devices are inherently rugged and can be designed and built to endure internal and external stress and severe operating environment.

Device ruggedness is defined as the ability to withstand stringent operating conditions within the bounds of its safe operating area (SOA). The SOA is established by the maximum ratings and recommended operating conditions specified in the data sheet. These specifications are operating guidelines to safeguard the device to the extent of its physical and structural design limits. In a worst case situation, the ability of the device to withstand harsh operating conditions is supported by a number of parameters set at absolute maximum ratings. Ruggedness tests done on the HIP2060 QVDMOS had proven the device to be very rugged at specified test conditions. The device is designed and optimized with improved dv/dt capability in order to prevent destructive failure due to a potential second breakdown mechanism of the parasitic bipolar (npn) transistor (see References 5 and 7).

To determine the ruggedness capability of the device, an unclamped inductive switching test procedure is performed using the test circuit shown in Figure 10A. The total energy is calculated in watts times second (W-s) using Equation 4.

$$\text{Energy (W - s)} = \int_0^{t_{AV}} IV\,dt \qquad \text{(EQ. 4)}$$

Integrating yields

$$E_{AS} = \frac{(I_{AS})(BV_{DSS})}{2}(t_{AV}) \qquad \text{(EQ. 5)}$$

In terms of inductance and voltage supply, E_{AS} can be calculated using the equation

$$E_{AS} = \frac{(L)\ (I_{AS})^2}{2}\ \frac{BV_{DSS}}{(BV_{DSS} - V_{DD})} \qquad \text{(EQ. 6)}$$

where BV_{DSS} is the avalanche voltage at peak avalanche current I_{AS}. V_{DD} is the voltage supply, L is the inductance of the air core inductor, and t_{AV} is the length of time when the device is at avalanche. Air core inductors are used in the test

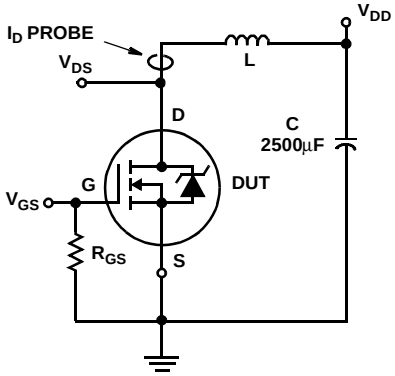


FIGURE 10A. UNCLAMPED INDUCTIVE SWITCHING TEST CIRCUIT

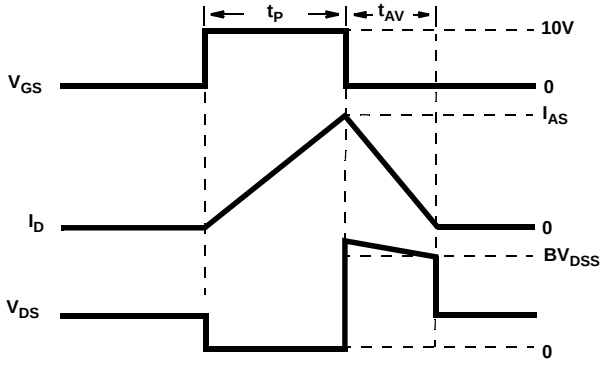


FIGURE 10B. UNCLAMPED INDUCTIVE SWITCHING INPUT AND OUTPUT WAVEFORMS AND

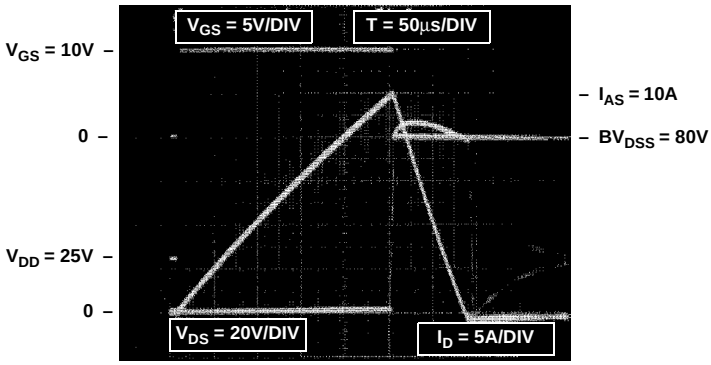


FIGURE 10C. OSCILLOSCOPE DATA TO DETERMINE SINGLE PULSE AVALANCHE ENERGY

FIGURE 10.

circuit to avoid possible core saturation problems. The factor $BV_{DSS}/(BV_{DSS}-V_{DD})$ in Equation 6 is a correction factor to account for the additional energy from the power supply. The total avalanche switching energy E_{AS} from the oscilloscope test data sample in Figure 10C is calculated as shown in Test A column of Table 1.

TABLE 1. AVALANCHE ENERGY TEST DATA

PARAMETER	TEST A	TEST B	TEST C	TEST D
L (mH)	0.54	1.0	2.0	2.25
Pulse Width, t_P (µs)	250	450	700	825
BV_{DSS} (V)	80	81	82	82
t_{AV} (µs)	100	200	360	380
E_{AS} (mJ)	40	75	145	160

NOTE: Test Condition: V_{DD} = 25V, V_{GS} = 10V, I_{AS} = 10A, Duty Cycle = 1.0%, Starting Case Temperature T_C = +25^{o}C

Power Device Array Design Subtleties and Advantages

The goal of power MOSFET array design is to combine two or more discrete transistors into a single package. As explained earlier, this has the advantage of reducing part count, pin count, and board space. Reducing pin count also has the added advantage of reducing stray inductance in each of the devices in the array.

Power Dissipation and Thermal Resistance

Two types of power dissipation are inherent to MOSFET devices. First is the static power dissipation that is due to leakage and conduction currents. Leakage currents, which result from device construction, contribute to losses during forward blocking mode and off-state conditions. The static power dissipation due to conduction currents, also known as the “on” losses, is associated with parasitic resistances. These on-state static characteristics are related to threshold voltage, on-resistance and forward transconductance of the device. Second is dynamic power dissipation due to switching, charging, and discharging of the device. Parasitic capacitances play an important role in these switching losses.

Primarily, the power consumption in a power MOSFET is a function of on-resistance and maximum current ratings. The drain current ratings are based on power dissipation, thermal resistance, and maximum operating temperature constraints. In a given ambient temperature, the junction temperature can be calculated by the product of total power dissipation and total thermal resistance. The total thermal resistance $R_{\Theta T}$ (in ^{o}C/W) is a combination of three different thermal resistance parameters associated with the power semiconductor device namely; junction-to-case thermal resistance $R_{\Theta JC}$, case-to-sink thermal resistance $R_{\Theta CS}$, and sink-to-ambient thermal resistance $R_{\Theta SA}$. The reliability of the device (its ability to withstand long and stringent operating conditions without failure) is directly related to the junction temperature. In order to maintain the junction temperature below its maximum rating, proper heat-sinking technique should be utilized. In view of this, a MOSFET array portrays a bigger advantage since there is no need to isolate the package from the heat sink. The package can be mounted directly to the heat sink without costly insulator kits. This will provide a securely-tight bonding of the package metal tab and heat sink. Without the insulators, the direct metal-to-metal contact will create a very low thermal resistance and much more effective heat-flow transfer path to dissipate the heat. Studies have also shown a significant reduction of the thermal resistance when heat-sink thermal compounds or thermal “grease” are used. Although considered to be a messy procedure, the use of thermal compounds is highly recommended to fill-up the uneven spaces or voids between the tab and the heat sink so heat flow transfer is more effective. This package and heat sink assembly procedure allows high chip power dissipation while maintaining low junction temperatures and increases product reliability.

Switching Performance

Power MOSFETs have their own dynamic characteristics such as input/output capacitance and switching times for turn-off/turn-on. The switching performance of the device depends largely on the RC time constant defined by the product of the gate input capacitance, its intrinsic gate resistance, and the gate drive circuit impedance and on the L/R time constant defined by the ratio of the stray inductance and the total on-resistance. External package connection is the main source of parasitic inductances. The dynamic characteristics of the device is listed in the data sheet to aid the designer in determining the power dissipation during switching between on and off states. The HIP2060 array has the advantages of lower input and output capacitance, low gate charge, low gate resistance and less stray inductances. These device features are very valuable for high-frequency circuit applications.

Drain and Gate Over-Voltage Stress

The maximum voltage ratings of drain-to-source, V_{DS}, and gate-to-source, V_{GS}, are specified in the MOSFET data sheet (see Reference 8). These specifications are used as guidelines for proper handling procedure to ensure longevity of the product operating life. Under any circumstances, the maximum gate-to-source voltage rating (typically ±20V) must not be exceeded. One of the failure mechanism of many MOSFET devices is their sensitivity to electrostatic discharges (ESD). These voltages are often high and very destructive and can rupture the gate oxide to create a gate-to-source or gate-to-drain “short” or “open” as the case may be. For ESD protection, a back-to-back zener clamping diode connected in series between the gate and source can minimize the potentially destructive gate voltage transients.

The QVDMOS has its inherent self-limiting device characteristics that can not be prevented, but rather, must be recognized and understood so that successful applications can be achieved. The construction of the device, layout and package assembly causes a considerable amount of parasitic capacitance and stray inductances due to on-chip metal interconnects, bondwires, package leads, and metal routings

on the printed circuit board (PCB). Although designed to be rugged, power devices are very susceptible to voltage transients during switching. This voltage overshoots are mainly due to induced voltage in stray inductances of the drain and source nodes. Drain over voltage often occur during device turn-off transition. When the common-source parasitic inductor stores energy during turn-on of the “freewheeling” internal body diode, the induced voltage can create a large overshoot of the drain voltage. If the stray inductance is large, the overshoot voltage can exceed the breakdown voltage rating of the device. One way to reduce the overshoot voltage is to slow down the turn-off time of the device. Another way is to use either externally or internally connected voltage clamp diodes across the device, or each device in the case of the half-bridge circuit.

The integrated feature of the MOSFET array design offers the advantage of smaller stray inductance in the package due to its reduced pin count. The half-bridge configuration of the dual power MOSFETs integrated in a single chip significantly reduces the stray inductance, especially at the PHASE node, which is otherwise not possible in a dual discrete (half-bridge) format.

Diode Reverse Recovery

In many application circuits, the intrinsic body diode in a power MOSFET serves as a “freewheeling” or “clamping” rectifier. Although its function sounds very attractive, the commutation process imposes power dissipation. Reverse recovery losses are attributed by the ability of the internal body diode of a MOS device to remove its stored charge before allowing itself to regain high reverse blocking resistance. The stored charge is generated during a short interval when the diode is in reverse blocking mode. The test circuit shown in Figure 11A and 11B represents a typical application circuit used in determining the reverse recovery time of the intrinsic body diode.

Figure 11A shows a dual QVDMOS array with the lower device being configured as a low side switch. It serves as the “on and off” switch to enable the supply current to pass through the inductor connected across the upper device. The upper device M1 is normally off with its gate terminal tied to source (PHASE node of the half-bridge). When M2 is on, supply current I_{DS} passes through the inductor towards the bottom rail. The induced voltage in the inductor will then supply current, I_{SD}, through the upper device’s intrinsic body diode during off-condition of transistor M2. The voltage across the diode of M2 is maintained below the MOS breakdown voltage BV_{DSS} rating to prevent the diode from operating in a potentially destructive avalanche region during reverse blocking mode. The diode voltage should be maintained below BV_{DSS} - (L x di/dt) value where L is the parasitic inductance approximately 7.5nH of the source electrode and di/dt is the rate of change of the drain current.

Similar test procedure is performed to determine the diode recovery charge of the intrinsic body diode of the lower device M2 where transistor M1 of the half-bridge is used in a high side switch configuration as shown Figure 11B. Suitable inductor, L1, values range from 10 to 50µH. Capacitance, C1, is at least 1000µF to provide enough drain current equivalent to 10A. Experimental data of the upper (M1) and lower (M2) devices’ intrinsic body diode are shown in Figure 12B and 12C, respectively. The slightly longer recovery time of the lower device’s body diode is due to the extra added parasitic capacitance of drain-to-substrate junction because both the substrate and source (pin labeled SOURCE2) of lower device are internally connected in the final package configuration.

The diode recovery curve is illustrated in detail in Figure 13. Here, the pn junction is acting as a battery because of stored charge. The diode is supplying additional conducting current in a reverse direction and constant charges Q1 and Q2 are generated. The recovery charge Q_{RR} is the sum of Q1 and Q2 and its inverse ratio is called the snappines of the body diode. The slope of the current as it approaches $I_D = 0$ is determined by the gate drive current and the external elements.

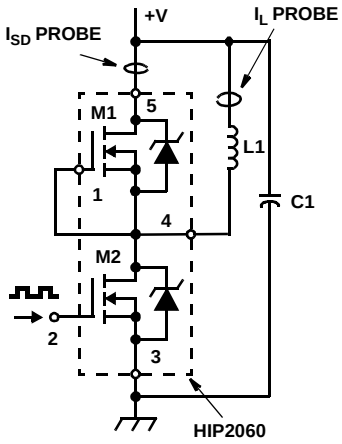


FIGURE 11A. REVERSE RECOVERY TEST CIRCUIT FOR LOW SIDE SWITCH CONFIGURATION

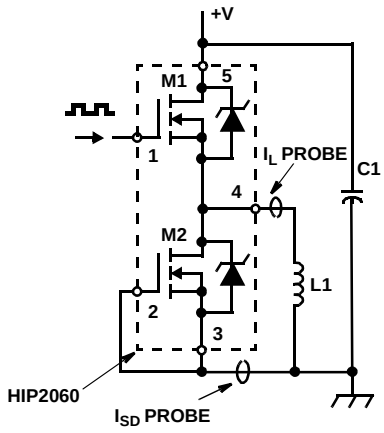


FIGURE 11B. REVERSE RECOVERY TEST CIRCUIT FOR HIGH SIDE SWITCH CONFIGURATION

FIGURE 11.

At any given di/dt, the reverse recovery charge is:

$$Q_{RR} = \frac{1}{2} t_{RR} I_{RR} \quad \text{(EQ. 7)}$$

and the reverse recovery current is

$$I_{RR} = \frac{di}{dt} \frac{Q1}{(Q1 + Q2)} t_{RR} \quad \text{(EQ. 8)}$$

Snappiness is the ratio of Q2 and Q1,

$$S = \frac{Q2}{Q1} \quad \text{(EQ. 9)}$$

Therefore,

$$I_{RR} = \frac{di}{dt} \frac{t_{RR}}{(S + 1)} \quad \text{(EQ. 10)}$$

Substituting Equation 10 to Equation 7 gives

$$Q_{RR} = \frac{1}{2} t_{RR} \frac{di}{dt} \frac{t_{RR}}{(S + 1)} \quad \text{(EQ. 11)}$$

$$t_{RR} = \left(\frac{2 (S + 1)}{\frac{di}{dt}} Q_{RR} \right)^{1/2} \quad \text{(EQ. 12)}$$

$$I_{RR} = \left(\frac{2 Q_{RR} \frac{di}{dt}}{S + 1} \right)^{1/2} \quad \text{(EQ. 13)}$$

Substrate Injection

The standard fabrication process of the popular vertical DMOS technology to build discrete power devices is to use an n-type starting wafer substrate which is normally connected as the drain node of the finished product. However, that disadvantages because the drain of the true VDMOS is the back of the die and electrically connected to the n-substrate. Hence, it is not possible to build multiple or an array of power devices unless they have a common drain or heat-sink isolators. Another disadvantage is that since the back of the die is the drain of the device, the package tab is typically connected to the drain. In many

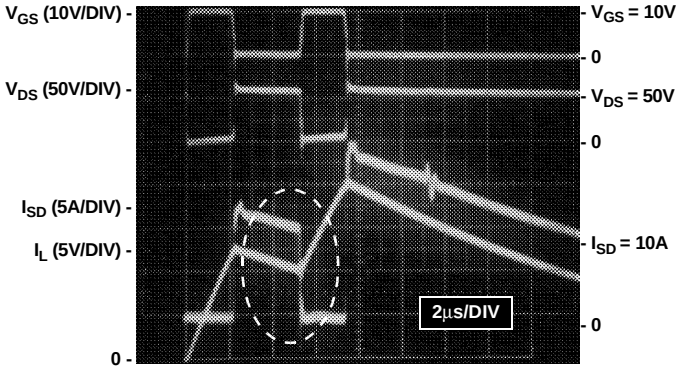


FIGURE 12A. INTRINSIC DIODE REVERSE RECOVERY (t_{RR}) OF HIP2060 QVDMOS INDICATED BY DOTTED INCIRCLED AREA OF PICTURE

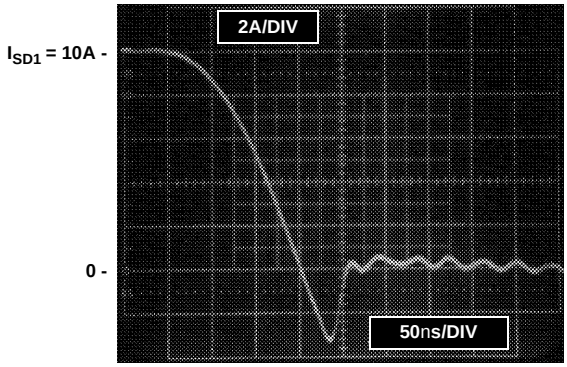


FIGURE 12B. INTRINSIC DIODE REVERSE RECOVERY (t_{RR}) OF HIP2060 QVDMOS FOR UPPER DEVICE

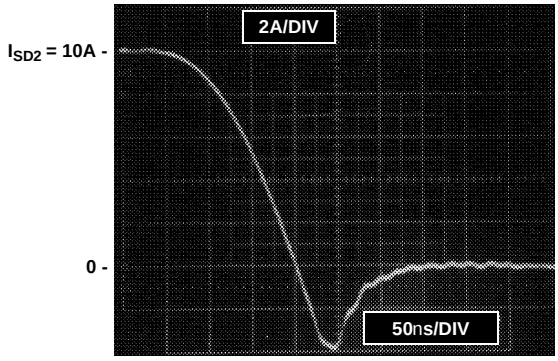


FIGURE 12C. INTRINSIC DIODE REVERSE RECOVERY (t_{RR}) OF HIP2060 QVDMOS FOR LOWER DEVICE

FIGURE 12.

applications this requires the package to be isolated, thus, increasing the thermal impedance and assembly cost of the final configuration.

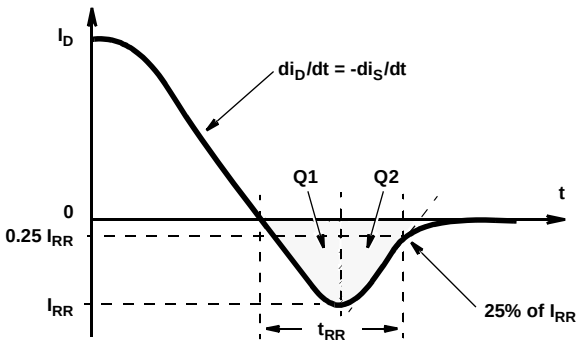


FIGURE 13. DIODE REVERSE RECOVERY WAVEFORM

On the other hand, the design of quasi-VDMOS structure utilizes a p-type substrate (see Figure 14) in order to isolate each power MOSFET device when integrated in a single chip.

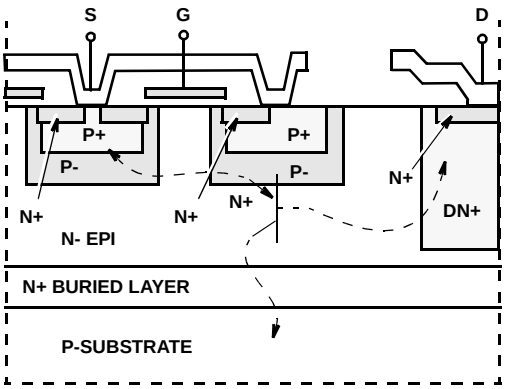


FIGURE 14A. PNP IN QVDMOS

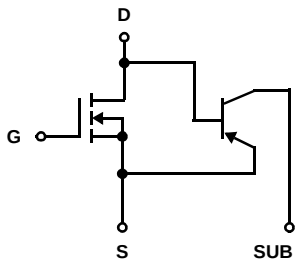


FIGURE 14B. EQUIVALENT CIRCUIT

FIGURE 14.

The same technique is used when integrating low voltage logic circuits and power devices (commonly known as intelligent power). In most cases, the p-substrate is tied to GND. The resulting structure makes a bipolar junction transistor (a vertical p-n-p) where the substrate serves as the p-collector. This pnp structure creates a possible path of collector (or substrate leakage) current that originates from the MOS transistor above it. In low power and low-frequency applications, this leakage current is too small to be a concern. However, in high power and high-frequency operating conditions, a fraction of source-to-drain current, I_{SD}, will drift into the substrate which can be translated into power dissipation and energy loss. Substrate current, I_{SUB}, injection is caused by the parasitic vertical pnp represented by the nodes of the DMOS as shown in Figure 14. Test data shown in Figure 15 is extracted with pulsed steps of 300µs at room temperature with the DMOS gate tied to ground.

The current-gain factor ($\alpha_F = I_C/I_E$) in Figure 15 indicates the fraction of carriers injected from the emitter (DMOS source) that reach the collector (DMOS substrate). Emitter current I_E is the difference between base current I_B and collector current I_C. Achieving very low substrate current injection is desirable for most circuit applications so that power dissipation due to substrate injection is negligible. In the HIP2060 MOSFET array design, this is obtained by the n+ buried layer's ability to suppress the pnp action. Moreover, the substrate is electrically connected to the source of the low-side switch of the half-bridge, effectively clamping to a V_{BE} minimizing power dissipation.

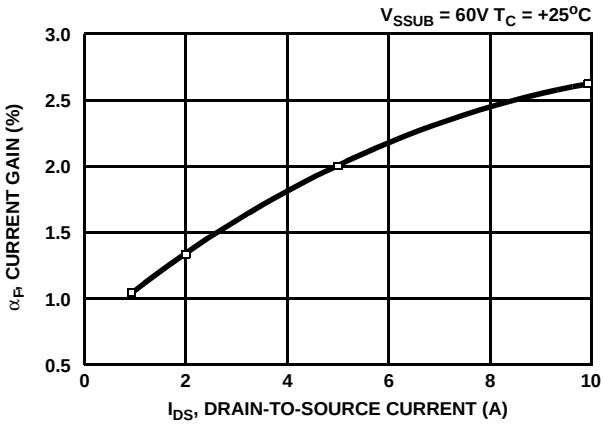


FIGURE 15. HIP2060 QVDMOS BODY DIODE SUBSTRATE INJECTION. PERCENT OF CURRENT GAIN vs DRAIN-TO-SOURCE CURRENT

Reduced EMI - An Advantage of Power MOSFET Arrays

Careful assessment of the "pros and cons" must be done before making decisions as to what type of power semiconductor device should be used and what type of package is most suitable for the intended circuit applications. The problem of electromagnetic interference (EMI) in many high-frequency circuit applications has been dealt with power switching designers for a long time. One source of this problem has been traced to the mechanical arrangement of a power discrete package when mounted on a heat sink since the package tab is the drain of the FET and the heat sink is typically tied to chassis ground. The mounting process requires costly plastic insulator kits, therefore, creating large stray capacitance between the drain and the heat sink which are typically at high and low potential, respectively. As simple as it is, this problem creates a complexity in designing the whole system.

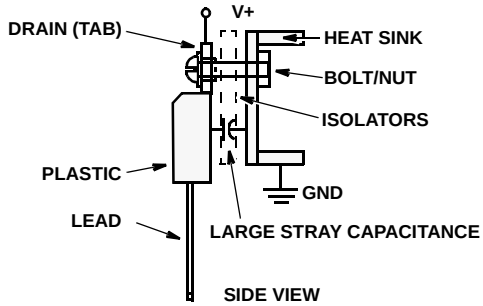


FIGURE 16A. TYPICAL METHOD OF MOUNTING DISCRETE POWER MOSFET PACKAGE ON THE HEAT SINK

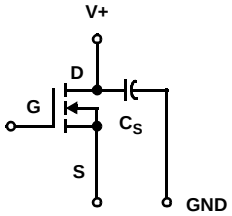


FIGURE 16B. EQUIVALENT CIRCUIT SHOWING LARGE STRAY CAPACITANCE C_S

FIGURE 16.

An illustration of the package and heat sink configuration is shown in Figure 16. The figure represents a classical mounting technique when using a conventional (discrete) power MOSFET. Large stray capacitance is present between the high-potential drain (tab) and the grounded heat sink. The charging and discharging of the “unwanted” capacitance can create potential EMI problems and could be more severe, especially when multiple power FETs are used.

In an integrated MOSFET array, each QVDMOS is being isolated in the chip by using a p-substrate which is also the back of the die that serves as contact when solder-attached to the package. Although a junction diode D1 exists as shown in Figure 1, its capacitance value is negligible in terms of dealing with EMI problems. A very attractive feature of the MOSFET array is that the package tab does not have to be the drain (see Figure 17), thereby eliminating the need for heat sink isolation. This advantage over power discretes provides a common heat-sinking technique, so EMI problems are significantly reduced (if not totally eliminated) and further decreases the complexity of a system design.

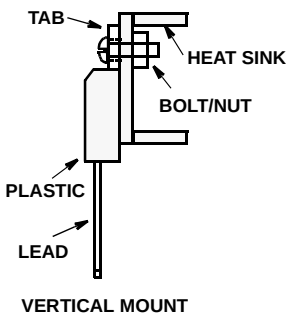


FIGURE 17A. VERTICAL MOUNTING OF HIP2060 ARRAY PACKAGE TO THE HEAT SINK

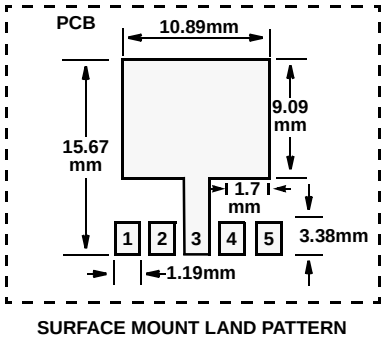


FIGURE 17B. SURFACE MOUNTING OF HIP2060 ARRAY PACKAGE TO THE HEAT SINK

FIGURE 17.

Power MOSFET Array in Circuit Applications and System Guidelines

Various application circuits are shown in Appendix B. A class-D audio amplifier is shown in Figure 21. In the simplified diagram, two HIP2060’s form a H-bridge switch in place of four discrete power devices, thus, providing a significant board space savings and part count reduction. The schematic shows a high frequency H-bridge driver IC (HIP4080) which provides the ability to operate from $10V_{DC}$ to $80V_{DC}$ busses for driving H-bridges that operate in class-D switch-mode, using two HIP2060 half-bridges as switch elements (see Reference 9). Figures 22 and 23 show two different circuit applications utilizing the half-bridge and three phase-bridge topologies.

From a circuit application standpoint, there is a so-called short-circuit power dissipation that is due to short circuit current that flows through the half-bridge when both transistors are on. This event happens when cross-conduction condition occurs, that is, when both transistors are turned-on at the same time. This condition (also known as “shoot-through”), could result in severe stress to the individual FETs in the half-bridge. It must then be properly controlled by the gate drive circuitry to allow sufficient “deadtime” to occur to prevent excessive conduction currents and energy stresses through the transistors. It should also be noted that small shoot-through currents can be converted into power dissipation and energy loss.

Exercising the following guidelines provides an advantage when using the HIP2060 on system board level applications:

1. For vertical mount (using a straight-leaded TO-220 package), two HIP2060’s can be mounted, using a single heat sink since the dual FETs are isolated. There is no need to use costly insulators kits when attaching a heat sink to the package tab as shown in Figure 17A. This will provide a securely-mounted power semiconductor device and a very low heat transfer resistance between the package and the heat sink. As mentioned in the previous section, a significant reduction (an improvement) of the thermal resistance can be achieved when using heat-sink thermal compounds or thermal “grease”. This is highly recom-

mended to provide a very effective heat flow transfer.

2. The power device can be surface-mounted on the PCB using TO-263-style packages. This will provide a low profile circuit board which is very attractive for compact applications. The tab can be mounted or soldered directly to the PCB layout (land pattern) as in Figure 17B, showing the maximum dimensions for JEDEC MO-169AB packages. A complete package outline drawing for both TO-220 and TO-263 style packages is listed in Reference 8. The package TAB of the HIP2060 is at circuit ground. This configuration minimizes the parasitic capacitance across the high frequency node and significantly reduces the potential problem of EMI. An example of surface mounting configuration and pad area/heat sink requirements and thermal resistance calculations are listed in Appendix B.
3. A system designer should be aware that the tab and pin 3 of the package are internally connected and such should be dealt with accordingly in current sensing applications.

Summary and Conclusions

A new innovation of power semiconductor devices has been introduced - a dual MOSFET array topology in half-bridge configuration. The product represents a very attractive solution in minimizing the cost, weight and size of an electronic system especially in high-volume applications. The device's high reliability and ruggedness added to its very good switching performance makes the dual array topology an economically viable solution. Furthermore, the unique package implementation reduces pin count and eliminates heat sink isolation due to its grounded tab. Reduced EMI problems also presents a big advantage when using MOSFET arrays.

The HIP2060 power half-bridge MOSFET array consists of two matched N-Channel enhancement-mode MOS transistors integrated in one chip, thus, providing board layout area, heat sink savings, as well as, reduced part count for applications such as motor controls, uninterruptible power supplies, switch mode power supplies, voice coil motors, and Class D power amplifiers.

Acknowledgment

The author wishes to thank Mr. Jeff Mansmann for his technical support and discussions.

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[8] Intersil Data Sheet File Number 3983.

[9] Intersil Application Notes AN9404 and AN9405.

[10] Intersil Application Notes AN8610 and AN9209.

[11] Micrel Application Hint 17.

Appendix A

A. PSPICE Model Listing

The following is the device model netlist for the HIP2060 half-bridge power MOSFET array. The stray inductance, L_S (typically 7.5nH), of the drain and source leads are connected inside the dual MOSFET subcircuit as shown in Listing 1. This PSPICE PowerFET macromodel is discussed further in Reference 10.

Listing 1. HIP2060 Subcircuit Model Netlist

```
*Model File: "HIP2060.lib"; Rev. 5/30/95
.SUBCKT HIP2060   1   2   3   4   5
X1     6   1   7   3   HIP2060_1
LS1   5   6   7.5n
X2     7   2   8   3   HIP2060_1
LS2   7   4   7.5n
LS3   8   3   7.5n
.ENDS
.SUBCKT HIP2060_1   3   2   11   9
MOS1         4     2     1   1   NMOS1
JFET         10   1     4   J1
D1             5     6     D1
DBODY      1     10   D2
DBREAK     10   7     D3
DSUB         9     3     D4
VBREAK     7     1     DC 90
C21            2     1      850P
C23            2     10    50P
C24            2     4      1350P
RDRAIN      3     10   1.5e-03
RSOURCE   1     11   17.5e-03
FDSCHRG   4     2     VMEAS 1.0
E41            5     11   4   1   1.0
VPINCH      6     8     DC   10.0
VMEAS       8     11   DC   0.0
.MODEL NMOS1 NMOS LEVEL=3 (VTO=2.75
+ TOX=5e-08 KP=3.150e-03 PHI=0.65 GAMMA=2.55
+ VMAX=6.42e+07 NSUB=4.33e+16 THETA=0.6097
+ ETA=0.0015 KAPPA=1.275 L=1u W=5950u)
.MODEL J1 NJF (VTO=-15.0 BETA=10.736
```

+ LAMBDA=1.15e-02 PB=0.5848 IS=+1.0e-13
+ RD=3.53e-02 ALPHA=0.2)
.MODEL D1 D (IS=1.0e-15 N=0.03 RS=1.0)
.MODEL D2 D (IS=3.0e-13 RS=2.5e-03 TT=20N
+ CJO=350e-12)
.MODEL D3 D (IS=1.0e-13 N=1.0 RS=2.0)
.MODEL D4 D (IS=1.0e-13 RS=2.0e-03 CJO=197e-12)
.ENDS

B. Inductive Switching Circuit Using the QVDMOS Transistor Model

Figure 18 shows an inductive switching circuit in H-bridge configuration and its equivalent PSPICE circuit netlist in Listing 2. Two HIP2060 MOSFET arrays are used to form a H-bridge circuit driving an inductive load (a bidirectional motor) with an inductance, L_{LOAD}, of 2mH and series resistance, R_{LOAD}, equal to 15Ω. The intrinsic body diodes, represented by Z1, Z2, Z3, and Z4, are used as "freewheeling" or clamping diodes. Simulation waveforms of the H-bridge driver circuit are shown in Figure 19.

Listing 2. H-Bridge Circuit Netlist

*Circuit File: "hbridge.cir"
.options limpts=50000 itl5=10000 reltol=.0025 numdgt=5
X1 11 12 0 14 15 hip2060
X2 21 22 0 24 15 hip2060
Lload 14 8 2mH
Vload 8 9 0V
Rload 9 24 15ohm
Vplus 15 0 30V
Vgate1 11 14 pulse(0 10V 1.05m 25u 20u 4m 8m)
Vgate2 12 0 pulse(10V 0 1m 20u 20u 4.1m 8m)
Vgate3 21 24 pulse(10V 0 1m 20u 20u 4.1m 8m)
Vgate4 22 0 pulse(0 10V 1.05m 25u 20u 4m 8m)
.LIB "hip2060.lib"
.PROBE
.TRAN 100u 20m
.END

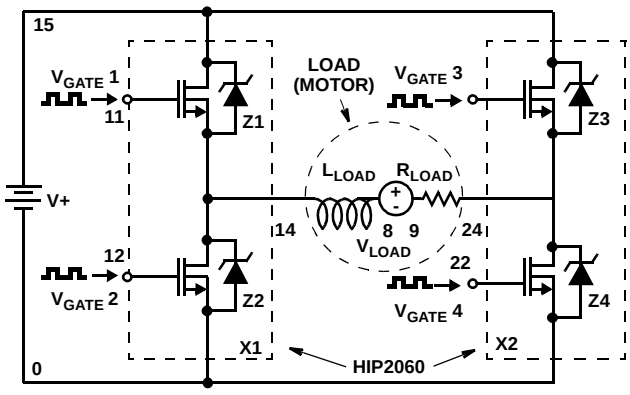

FIGURE 18. INDUCTIVE SWITCHING CIRCUIT - H-BRIDGE DRIVER FOR BIDIRECTIONAL MOTOR CONTROL APPLICATION CIRCUIT

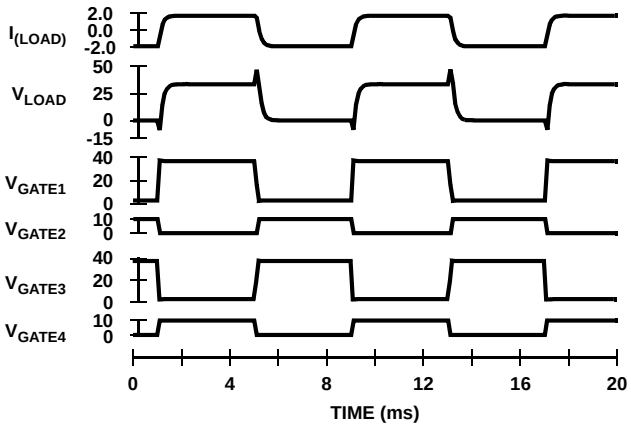

FIGURE 19. SIMULATION WAVEFORMS OF H-BRIDGE CIRCUIT SHOWING VOLTAGE (V) AND CURRENT (A) IN THE INDUCTOR, L_{LOAD}, AND GATE VOLTAGES vs TIME

Appendix B

A. Calculate PCB Pad Area/Heat Sink Requirements for Surface Mount Packages

A half-bridge configuration of surface mount packages is illustrated in Figure 20. The surface mount (TO-263 style) HIP2060 reduces EMI and simplifies the PCB layout compared with two surface mount (TO-262) "3055" transistors. For equivalent power dissipation (see Example 1), in terms of PCB utilization for heatsinking, one HIP2060 would use only 95mm^2 versus the two "3055's" requiring 5,400mm^2. (this assumes a ground plane is available for HIP2060 TAB connection).

Example 1:

Given: $T_A = 50^oC$ -Ambient temperature
$T_{J(MAX)} = 125^oC$ -Junction temperature(max)
$P_D = 3W$ -Power dissipation
$R_{\theta CS\_SP} = 0.1^oC\text{-in}^2/W$ -Specific thermal resistance, soldered to PCB pad

1. Find thermal resistance case-to-sink with respect to TAB area. (TO-263 TAB area = 0.096in^2, TO-262 TAB area = 0.0646in^2)
   a. Using one HIP2060:
      $R_{\theta CS} = (R_{\theta CS\_SP}) \div 0.096\text{in}^2 = 1.04^oC/W$
   b. Using Two RFD3055's:
      $R_{\theta CS} = (R_{\theta CS\_SP}) \div 0.0646\text{in}^2 = 1.55^oC/W$
2. Maximum temperature rise:
   $\Delta T = T_{J(MAX)} - T_A = 75^oC$
3. Required thermal resistance junction to ambient:
   $R_{\theta JA} = \Delta T/P_D = 75^oC/3W = 25^oC/W$
4. Heat sink-to-ambient thermal resistance for:
   a. One HIP2060: $R_{\theta SA} = R_{\theta JA} - (R_{\theta JC} + R_{\theta CS})$
      $= 25 - (1.86 + 1.04) = 22.1^oC/W$
   b. Two RFD3055's:
      $R_{\theta SA} = R_{\theta JA} - (R_{\theta JC} + R_{\theta CS})$
      $= 25 - (1.84 + 1.55) = 21.6\ ^oC/W$

5. Minimum PCB heat sink pad area (see Reference 11) when using:

   a. One HIP2060:
   If used on a PCB with no GND plane, then
   Pad area = 4950mm^2 = 2.77in. per side
   If used on a PCB with a GND plane, then
   Pad Area = 95mm^2 = 0.38in per side

   b. Two RFD3055's:
   If used on a PCB with no GND plane, then
   Pad Area = 5400mm^2 = 2.89in per side
   If used on a PCB with a GND plane, then
   Pad Area = 5400mm^2 = 2.89in per side

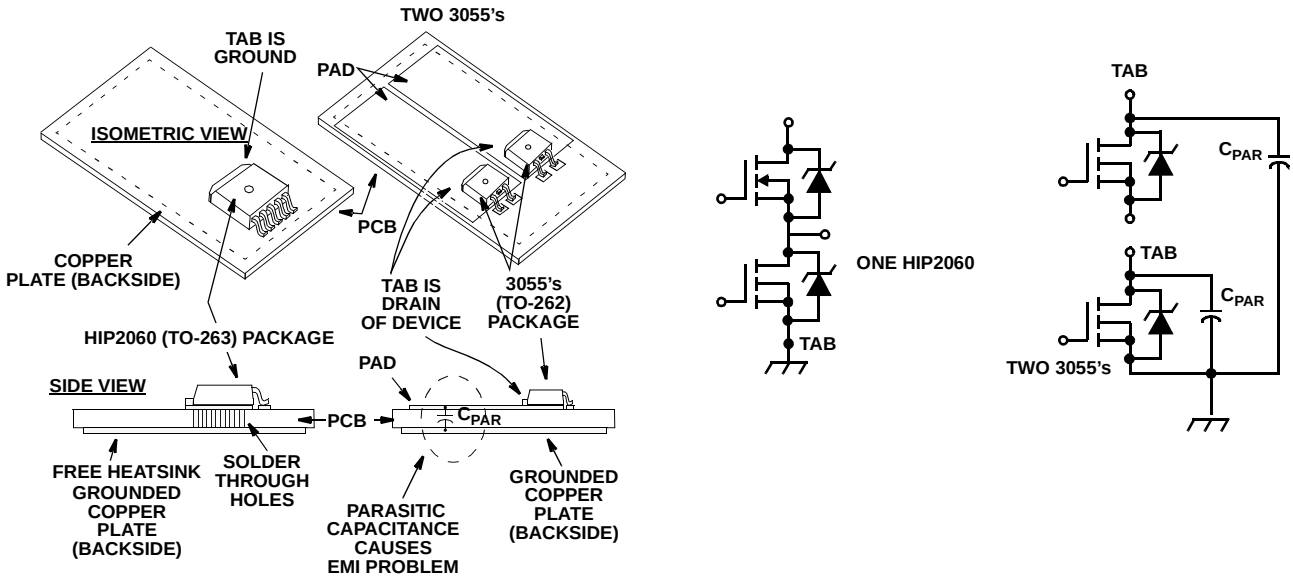

FIGURE 20. SURFACE MOUNTING CONFIGURATION OF HIP2060 MOSFET ARRAY COMPARED TO ITS DISCRETE COUNTERPART

Application Circuits

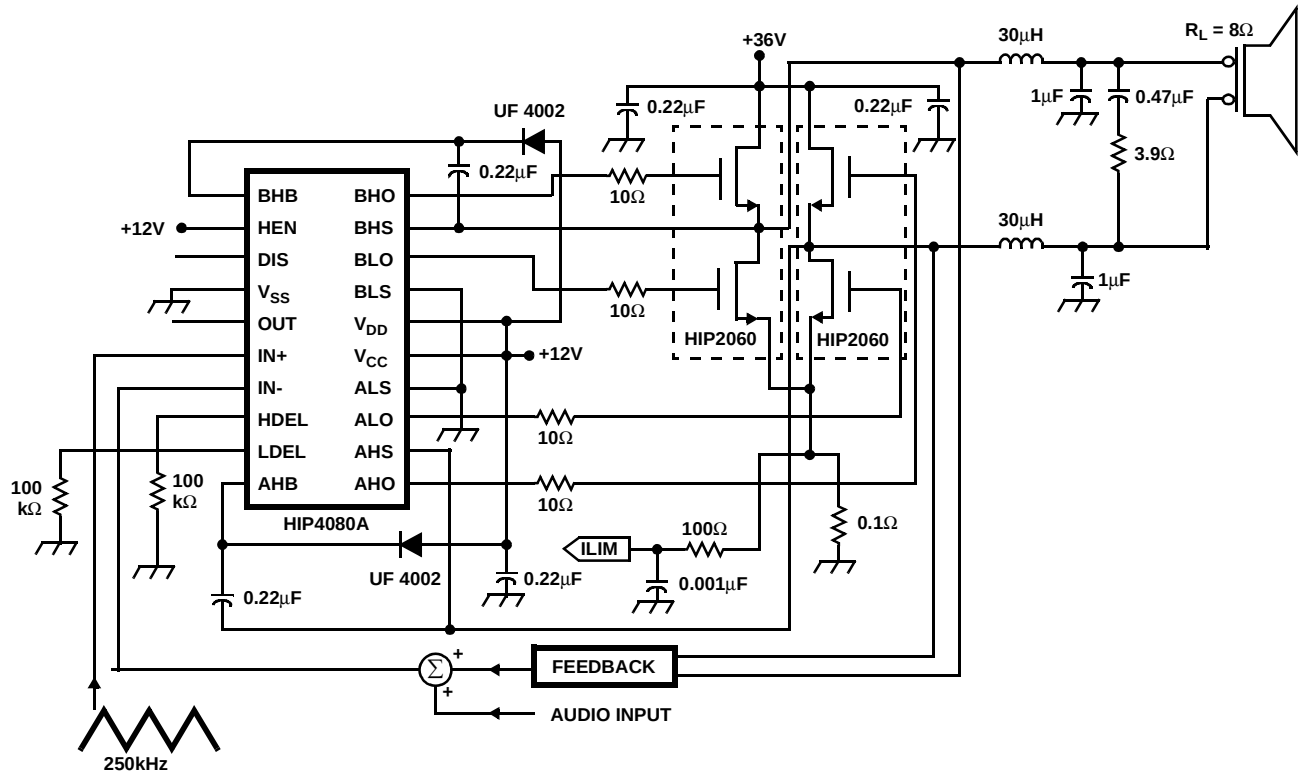

FIGURE 21. CLASS D SWITCHING AUDIO AMPLIFIER APPLICATION CIRCUIT

Application Circuits (Continued)

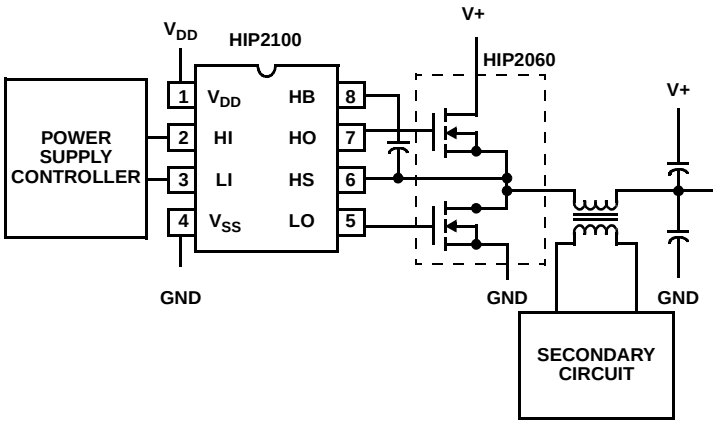

FIGURE 22. HIGH FREQUENCY HALF-BRIDGE DRIVER APPLICATION CIRCUIT

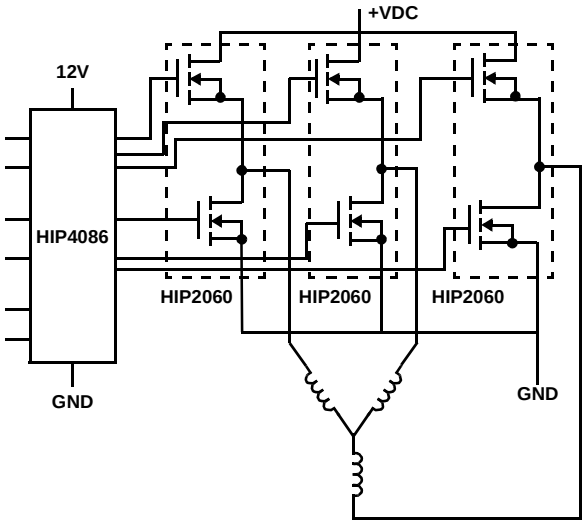

FIGURE 23. THREE PHASE-BRIDGE DRIVER FOR MOTOR CONTROL APPLICATION CIRCUIT