A Complete Analog-to-Digital Converter Operating From a Single 3.3V Power Supply

Application Note | August 1993 | AN9326

Introduction

The current data acquisition marketplace has an ever increasing demand for integrated circuits capable of operating with a single 3.3V power supply. The Intersil HI-5812 12-bit sampling analog-to-digital converter has proven capable of meeting this market demand and can assist system designers with their 3.3V requirements. The Intersil HI-5813, which will be our 3.3V, 12-bit ADC with guaranteed 3.3V parameters, is scheduled to be introduced in the fall of 1993.

Features

The Intersil HI-5812 is a fast, low power, 12-bit successive approximation analog-to-digital converter capable of operating from a single 3.3V to 6V supply. Typical supply current is 1.9mA (when operating with a 5V supply), and the device can operate from either an external clock or from its own internal clock. It is offered over the full industrial temperature range in 24 lead narrow body Plastic DIP, narrow body Ceramic DIP, and wide body Plastic SOIC packages.

Theory of Operation

The HI-5812 uses capacitor charge balancing to approximate the analog input. The heart of the converter is a capacitor network with a common node connected to a comparator and the second terminal of each capacitor is individually switchable to the analog input, $V_{REF}+$, or $V_{REF}-$.

A complete conversion takes 15 clock cycles. The first three clock cycles are used to auto-balance the comparator at the capacitor common node. The switchable terminal of every capacitor in the network is connected to the analog input during this time.

During the fourth clock period, all capacitors are disconnected from the input. The capacitor representing the MSB is then connected to the $V_{REF}+$ terminal and the remaining capacitors to $V_{REF}-$. After the charge balances out, the capacitor common node will indicate whether the input was above 1/2 of (($V_{REF}+$) - ($V_{REF}-$)). At the end of the fourth clock period the comparator output is stored and the MSB capacitor is either connected to $V_{REF}+$ (if the comparator output is high) or connected to $V_{REF}-$. This allows the next comparison to be at either 3/4 or 1/4 of (($V_{REF}+$) - ($V_{REF}-$)). A similar procedure is used during clock periods five through fifteen to test the capacitors representing the remaining bits. At the end of each clock cycle the comparator result is stored and each capacitor either connected to $V_{REF}+$ or $V_{REF}-$.

Typical 3.3V Performance

At room temperature, the HI-5812 will typically exhibit eleven bit linearity under the following operating conditions: (1) V_{DD} = V_{REF} + = 3.3V and (2) maximum clock frequency f_{CLKMAX} = 600kHz (which equates to a conversion time of t_C = 25µs).

Refer to Figure 1 through Figure 10 for typical performance curves. Note that all data shown was taken at room temperature (+25^{o}C).

Power supply current, at reduced supply voltage (3.3V), is typically 500µA and remains relatively independent of the applied external clock frequency (Figure 1.) **Offset and Gain** errors remain below ±2LSBs up to f_{CLK} = 600kHz (Figure 2 and Figure 3). Both **Differential and Integral Linearity** also remain below ±2LSBs with f_{CLK} up to 600kHz or 25µs conversion time (Figure 4 and Figure 5). Typical overall 12-bit performance is achievable with f_{CLK} up to 500kHz or 30µs conversion time.

Figure 6 and Figure 7 are spectral plots of the HI-5812 output with a 1kHz sine wave input and clock frequencies of 500kHz and 600kHz respectively. The plots show that the noise floor is between -90dB and -100dB and all harmonics are below -80dB for both clock frequencies. Figure 8, Figure 9 and Figure 10 illustrate signal-to-noise + distortion (SINAD) vs frequency, total harmonic distortion (THD) vs frequency, and effective number of bits (ENOB) vs frequency respectively. As expected, each of these parameters degrades with increasing clock frequency. In particular, ENOB decreases from 11.1 bits at f_{CLK} = 500kHz to 10.2 bits at f_{CLK} = 750kHz. Figure 11 shows the test circuit used for this 3.3V characterization. conversion time (Figure 4 and Figure 5). Typical overall 12-bit performance is achievable with f_{CLK} up to 500kHz or 30µs conversion time.

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Conclusions

The capacitor charge balancing technique used by the HI-5812 lends itself well to operation at reduced supply voltages. Optimal performance is determined by the clock frequencies applied.

Slower clocks allow for additional conversion time and allows the comparator to meet the higher accuracy requirements imposed by both the reduced headroom and the reduced LSB size. Eleven bit performance can typically be obtained with clock frequencies less than 600kHz (equating to t_C = 25µs) and twelve bit performance can typically be achieved with f_{CLK} = 500kHz (t_C = 30µs).

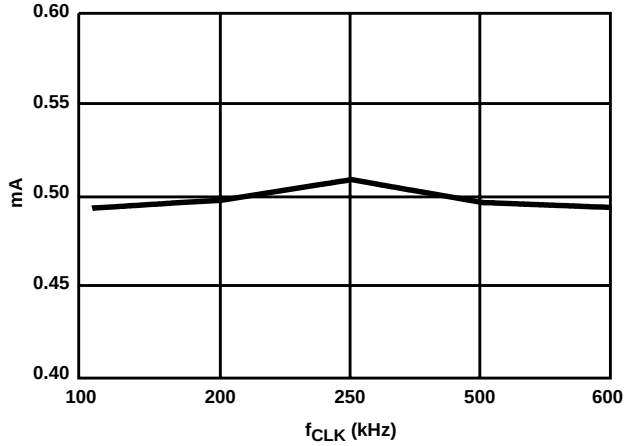

FIGURE 1. DYNAMIC POWER SUPPLY CURRENT vs CLOCK FREQUENCY

$V_{REF} = V_{DD} = 3.3V$

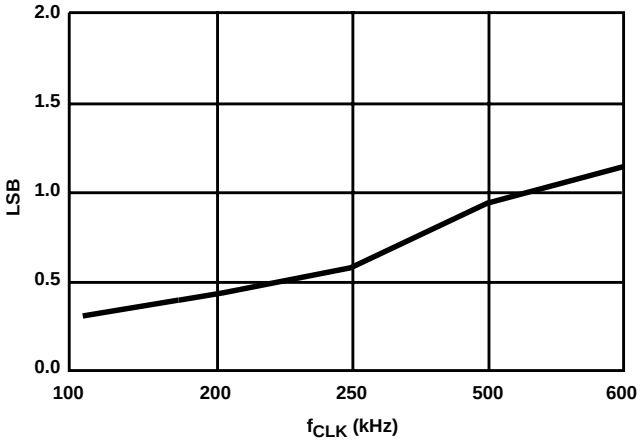

FIGURE 2. OFFSET ERROR (IN LSB) vs CLOCK FREQUENCY

$V_{DD} = V_{REF} = 3.3V$

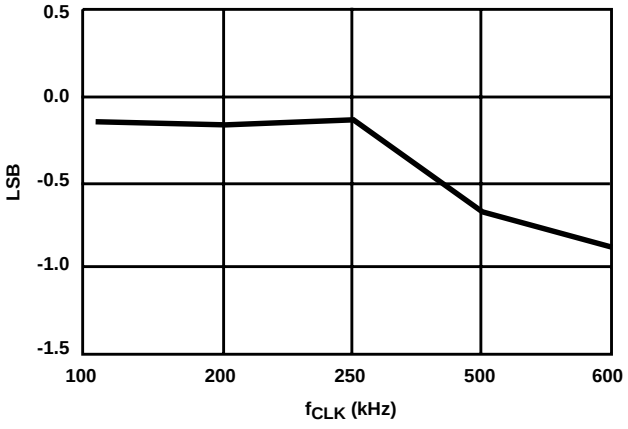

FIGURE 3. GAIN ERROR (IN LSB) vs CLOCK FREQUENCY

$V_{REF} = V_{DD} = 3.3V$

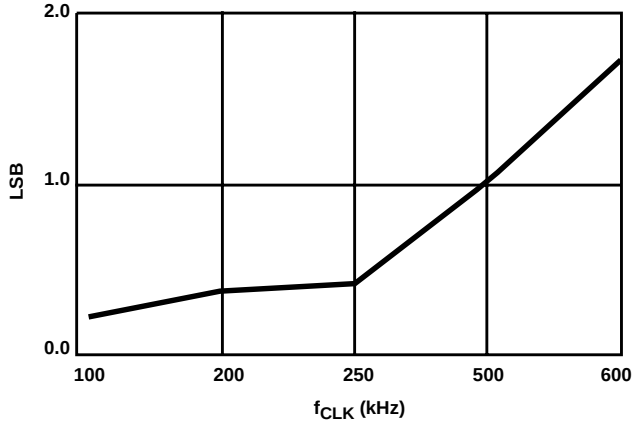

FIGURE 4. WORST CASE DIFFERENTIAL LINEARITY ERROR vs CLOCK FREQUENCY

$V_{REF} = V_{DD} = 3.3V$

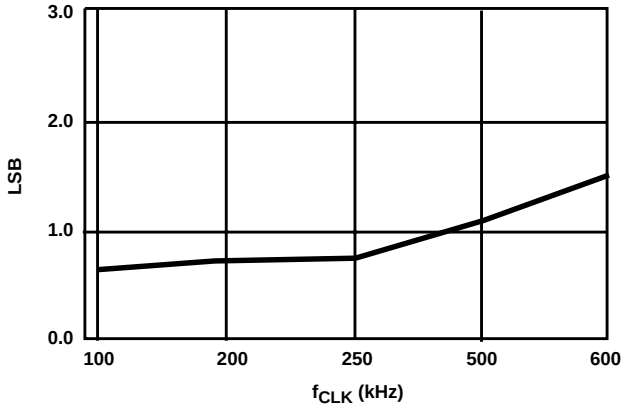

FIGURE 5. INTEGRAL INEARITY ERROR vs CLOCK FREQUENCY

$V_{REF} = V_{DD} = 3.3V$

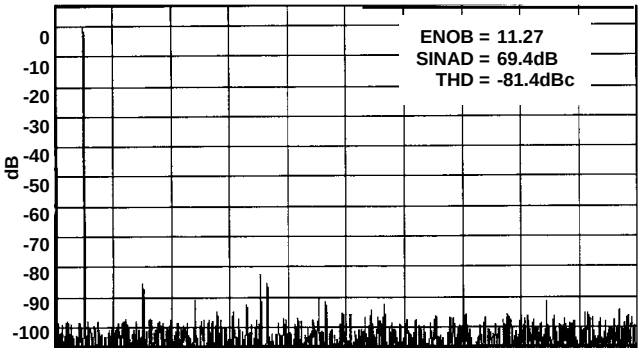

FIGURE 6. SPECTRAL PLOT

(f_{CLK} = 500kHz)

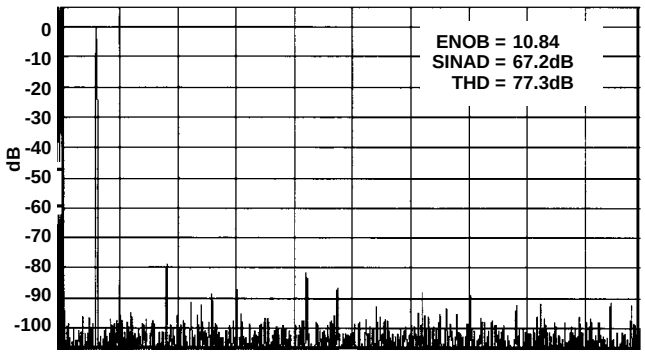

FIGURE 7. SPECTRAL PLOT
(f_{CLK} = 600kHz)

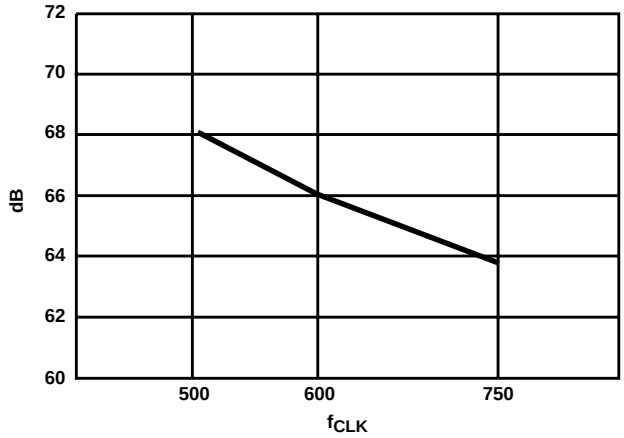

FIGURE 8. TYPICAL SIGNAL TO NOISE + DISTORTION (SINAD)
V_{REF} = V_{DD} = 3.3V, f_{IN} = 1kHz

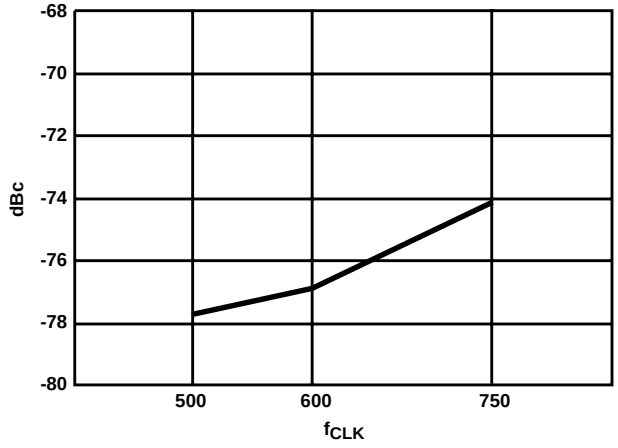

FIGURE 9. TOTAL HARMONIC DISTORTION
V_{REF} = V_{DD} = 3.3V, f_{IN} = 1kHz

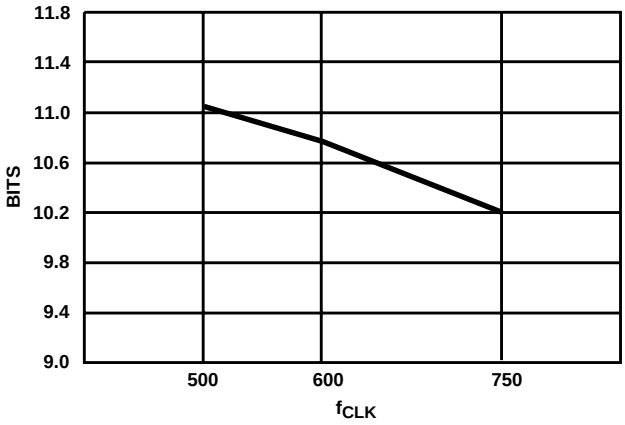

FIGURE 10. EFFECTIVE NUMBER OF BITS
V_{REF} = V_{DD} = 3.3V, f_{IN} = 1kHz

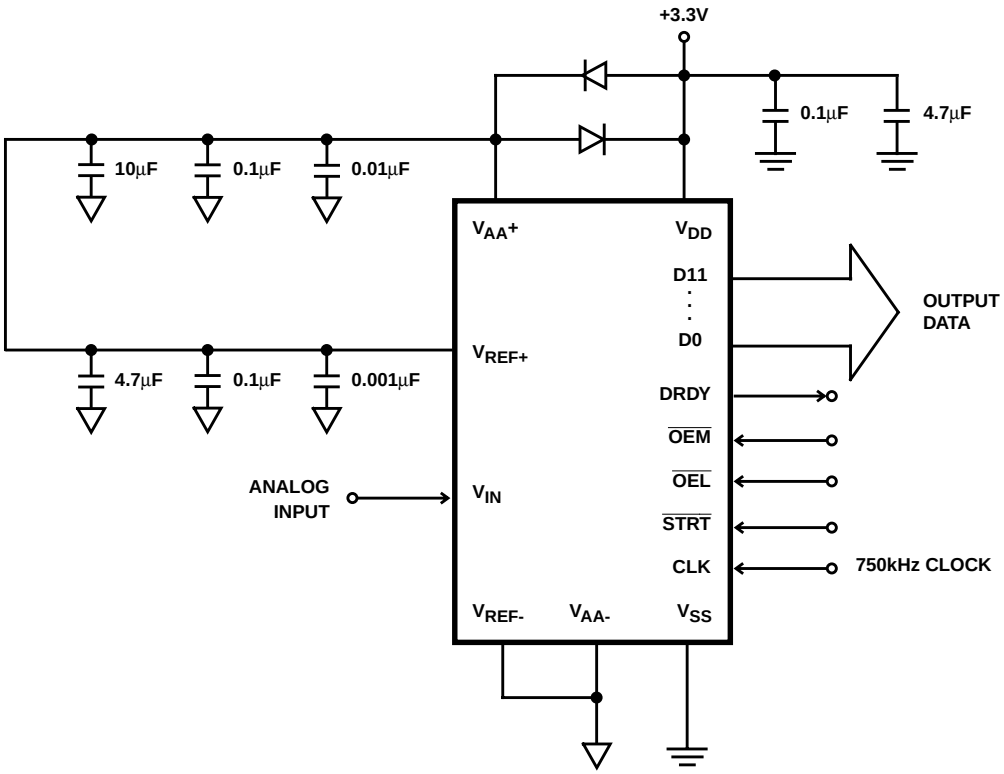

FIGURE 11.