HIP4080, 80V High Frequency H-Bridge Driver

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Introduction

The HIP4080 is a member of the HIP408X family of High Frequency H-Bridge Driver ICs. A simplified application diagram is shown in Figure 1. The HIP4080 H-Bridge driver IC provides the ability to operate from 8VDC to 80VDC busses for driving N-Channel MOSFET H-Bridges, The HIP4080 packaged in either 20 lead DIP or 20 lead SOIC, provides peak gate current drive of 2.5A.

A combination of bootstrap and charge-pumping techniques is used to power the circuitry which drives the upper MOSFETs of the H-Bridge. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to maintain bias voltage on the upper driver sections and MOSFETs. Since voltages on the upper bias supply pin “float” with the source terminals of the upper power switches, the design of this family provides voltage capability for the upper bias supply terminals to 95VDC.

The HIP4080 can drive lamp loads for automotive and industrial applications as shown in Figure 2. When inductive loads are switched, flyback diodes must be placed around the loads to protect the MOSFET switches.

The HIP408X family of devices is fabricated using a proprietary Intersil IC process which allows this family to switch at frequencies of over 500kHz. Therefore, the HIP408X family is ideal for use in voice coil motor, class-D audio amplifier, DC-DC converters and high performance AC, DC and step-motor control applications.

Many applications utilize the full bridge topology. These are voice coil motor drives, stepper and DC brush motors, audio amplifiers and even power supply inverters used in uninterruptable power supplies, just to name a few. Of the above, voice coil motor drives and audio amplifiers can take advantage of the built-in comparator available in the HIP4080. Using the output of the comparator to add some positive feedback, a hysteresis control, so popular with voice coil motor drivers, can be implemented as shown in Figure 3. In the figure, R3 is fed back from the comparator output, OUT, to the positive input of the comparator, IN+. Capacitor, C1, integrates in a direction to satisfy the reference current signal at IN. The IN- input of the comparator sums this current reference with a signal proportional to load current through resistor, R4, which comes from a differential amplifier, A1. A bias voltage of 6V (represents half of the bias voltage and the maximum rail to rail voltage of the comparator and amplifier, A1) biases the comparator’s IN+ terminal through R2 and the amplifier, A1’s, positive summing junction.

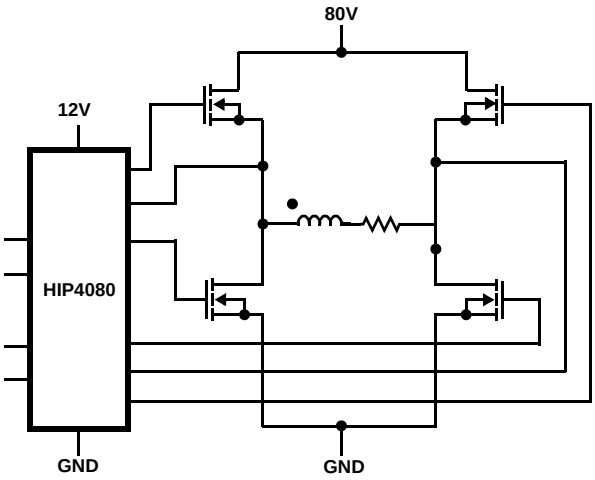


FIGURE 1. HIP4080 SIMPLIFIED APPLICATION DIAGRAM

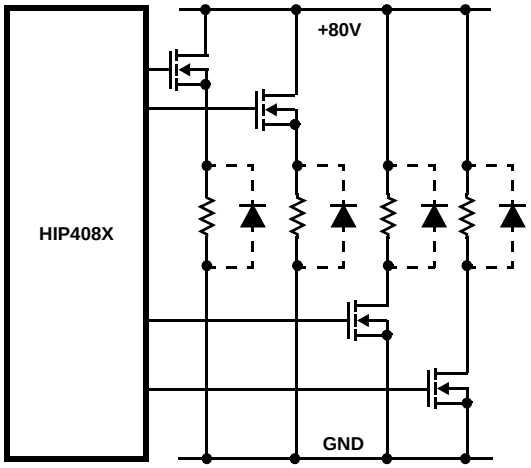


FIGURE 2. HIP4080 AS LAMP SWITCH DRIVER, DUAL HIGH/LOW SWITCHES FOR AUTOMOTIVE AND INDUSTRIAL CONTROLS

When no current is flowing in either direction in the load, the output of A1 is exactly 6V. The reference input, IN, would also have to be 6V to request zero current from the bridge. The bridge would still switch in this case, because of the positive feedback connection of the HIP4080 internal com parator. The frequency of oscillation of the output will be a function of the amount of dc hysteresis gain, R3/R1 and the size of capacitor, C1. As the capacitor, C1, is made larger, the steady-state frequency of the bridge will become smaller. It is beyond the scope of this application note to provide a full analysis. A valuable characteristic of hysteresis control is that as the error becomes smaller (i.e., the reference and

feedback signals match) the frequency increases. Usually this occurs when the load current is small or at a minimum. When the error signal is large, the frequency becomes very small, perhaps even dc. One advantage of this is that when currents are largest, switching losses are a minimum, and when switching losses are largest, the dc current component is small.

To provide accurate dead-time control for the twin purposes of shoot-through avoidance and duty-cycle maximization, two resistors tied to pins HDEL and LDEL provide precise delay matching of upper and lower propagation delays, which are typically only 55ns. The HIP408X family of H-Bridge drivers have enough voltage margin to be applied to all SELV (UL classification for operation at $\leq$ 42.0V) applications and most Automotive applications where “load dump” capability over 65V is required. This capability makes the HIP408X family a more cost-effective solution for driving N-channel power MOSFETs than either discrete solutions or other solutions relying on transformer or opto-coupling gate-drive techniques as shown in Figure 1.

The HIP4080 differs from the HIP4081 regarding the function of pins 2, 5, 6 and 7 of the IC and the truth table which governs the switching function of the two ICs. In the HIP4080, pins 2, 5, 6 and 7 are labeled HEN, OUT, IN+ and IN-, respectively. In the HIP4081, pins 2, 5, 6 and 7 are labeled BHI (B-side high input), BLI (B-side low input), ALI (A-side low input) and AHI (A-side high input), respectively. The HIP4081’s inputs individually control each of the four power MOSFETs, or in pairs (excepting the shoot-through case). The HIP4080 provides an internal comparator and a “HEN...high enable” pin. The comparator can be used to provide a PWM logic signal to switch the appropriate MOSFETs within the H-bridge, and can facilitate “Hysteresis” control to be illustrated later. The HEN pin enables (when HEN is high) or disables (when HEN is low) the upper MOSFETs. With HEN held low, it is possible to switch only the lower H-bridge MOSFETs. The HEN input can also be PWM-switched with the IN+ and IN- inputs used only for direction control, thereby minimizing switching losses.

Description of the HIP4080

The block diagram of the HIP4080 relating to driving the A-side of the H-Bridge is shown in Figure 4. The blocks associated with each side of the H-Bridge are identical, so the B-side is not shown for simplicity.

The two bias voltage terminals on the HIP408X H-Bridge Drivers, V_{CC} and V_{DD} should be tied together. They were separated within the HIP408X IC to avoid possible ground loops internal to the IC. Tying them together and providing a decoupling capacitor from the common tie-point to V_{SS} greatly improves noise immunity.

Input Logic

The HIP4080 accepts inputs which control the output state of the power MOSFET H-bridge and provides a comparator output pin, OUT, which can provide compensation or hysteresis.

The DIS, “Disable,” pin disables gate drive to all H-bridge MOSFETs regardless of the command states of the input pins, IN+, IN– and HEN. The HEN, “High Enable,” pin enables and disables gate drive to the two high side MOSFETs. A high level on the HEN pin “enables” high side gate drive as further determined by the states of the IN+ and IN– comparator input pins, since the IN+ and IN– pins control which diagonal pair of MOSFETs are gated. Upper drive can be “modulated” through use of the HEN pin while drive to diagonally opposing lower MOSFETs is continuous. To simultaneously modulate both upper and lower drivers, HEN is continuously held high while modulating the IN+ and IN– pins.

Modulating only the upper switches can nearly halve the switching losses in both the driver IC and in the lower MOSFETs. The power dissipation saved at high switching frequencies can be significant. Table 1 summarizes the input control logic.

TABLE 1. INPUT LOGIC TRUTH TABLE

IN+ > IN-	DIS	HEN	ALO	AHO	BLO	BHO
X	1	X	0	0	0	0
1	0	1	0	1	1	0
0	0	1	1	0	0	1
1	0	0	0	0	1	0
0	0	0	1	0	0	0

X = DON’T CARE 1 = HIGH/ON 0 = LOW/OFF

The input sensitivity of the DIS and HEN input pins are best described as “enhanced TTL” levels. Inputs which fall below 1.0V or above 2.5V are recognized, respectively, as low level or high level inputs. The IN+ and IN- comparator inputs have a common mode input voltage range of 1.0V to V_{DD} -1.5V, whereas the offset voltage is less than 5mV. For more information on the comparator specifications, see Intersil Data Sheet HIP4080, File Number 3178.

Propagation Delay Control

Propagation delay control is a major feature of the HIP4080. Two identical sub-circuits within the IC delay the commutation of the power MOSFET gate turn-on signals for both sides of the H-bridge. The gate turn-off signals are not delayed. Propagation delays related to the level-translation function (see section on Level-Translation) cause both upper on/off propagation delays to be longer than the lower on/off propagation delays. Four delay sub-circuits are needed to fully balance the H-bridge delays, two for upper delay control and two for lower delay control.

Users can tailor the low side to high side commutation delay times by placing a resistor from the HDEL pin to the V_{SS} pin.

Similarly, a resistor connected from LDEL to V_{SS} controls the high side to low side commutation delay times of the lower power switches. The HDEL resistor controls both upper commutation delays and the LDEL resistor controls the lower commutation delays. Each of the resistors sets a current which is inversely proportional to the created delay. The delay is added to the falling edge of the “off” pulse associated with the MOSFET which is being commutated off. When the delay is complete, the “on” pulse is initiated. This has the effect of “delaying” the commanded on pulse by the amount set by the delay, thereby, creating dead-time.

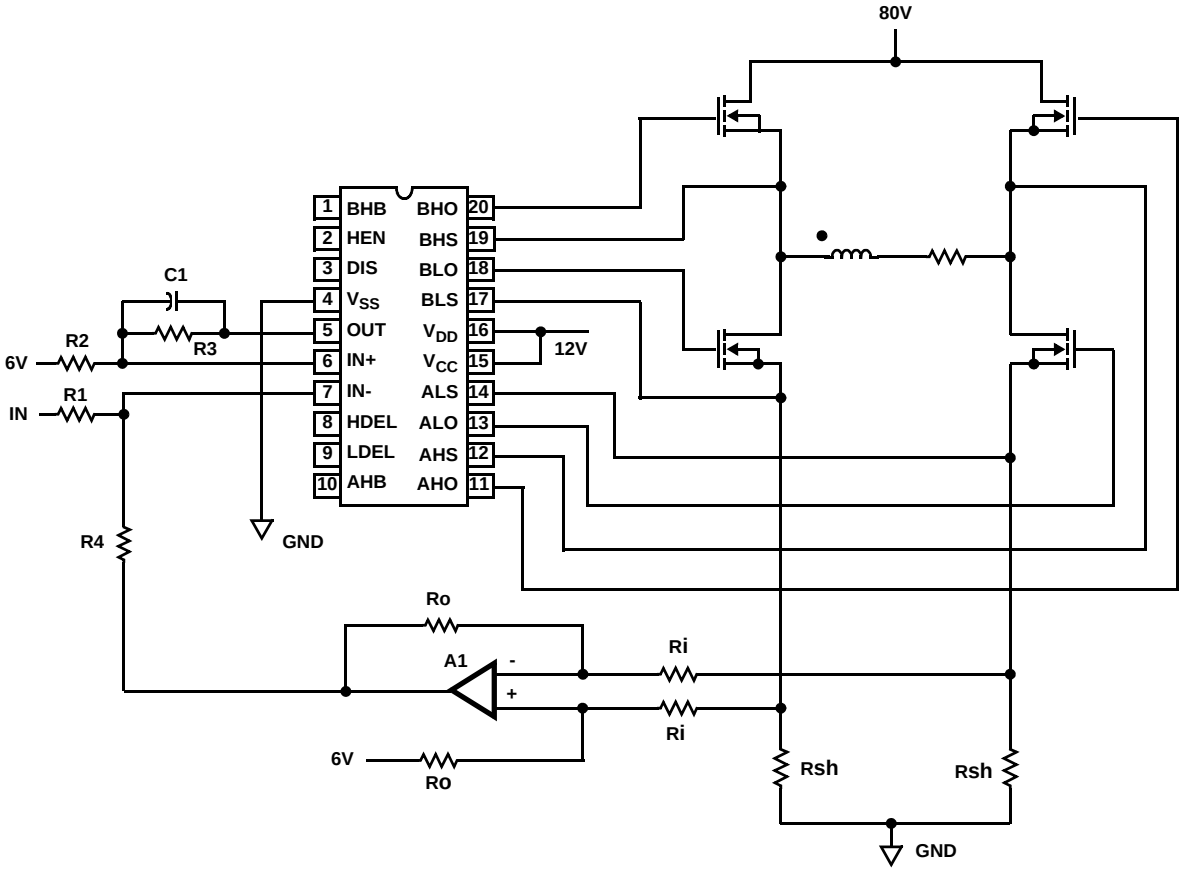


FIGURE 3. HYSTERESIS MODE SWITCHING

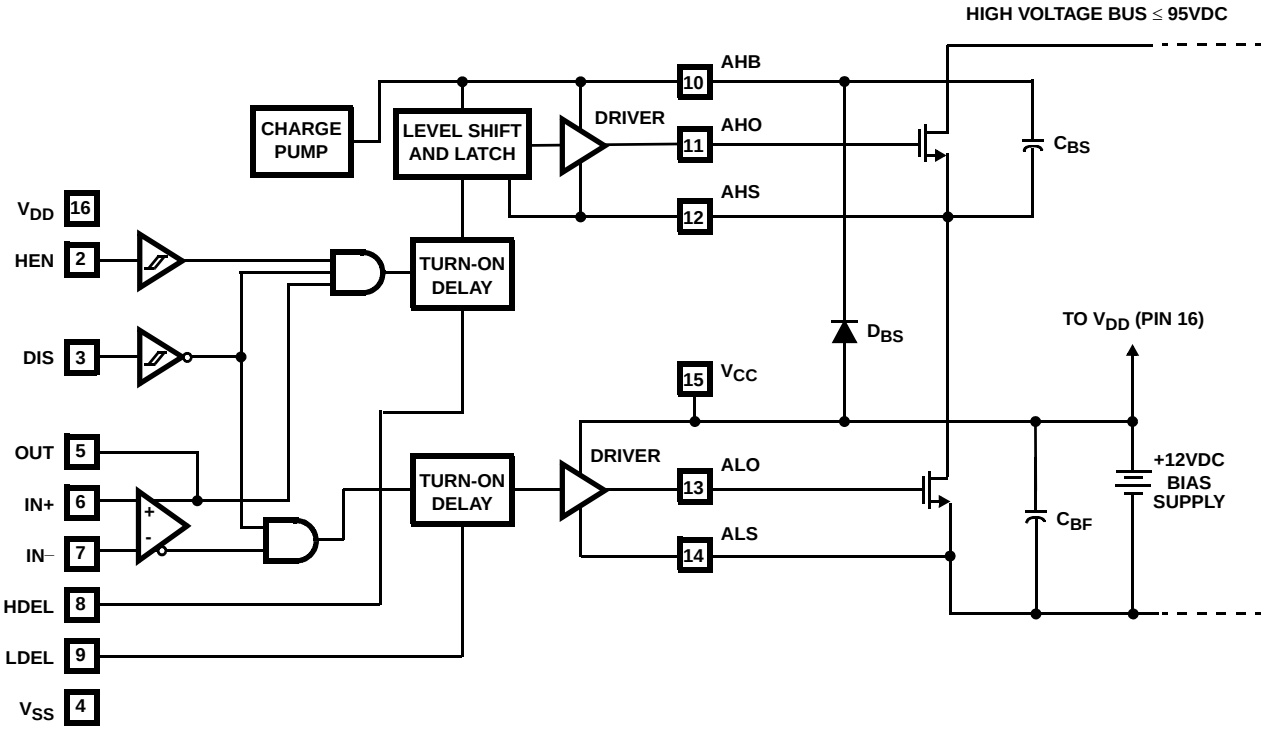


FIGURE 4. HIP4080 BLOCK DIAGRAM (A SIDE ONLY)

Proper choice of resistor values connected from HDEL and LDEL to V_{SS} provides a means for matching the commutation dead times whether commutating high to low or low to high. Values for the resistors ranging from 10kΩ to 200kΩ are recommended. Figure 5 shows the delays obtainable as a function of the resistor values used.

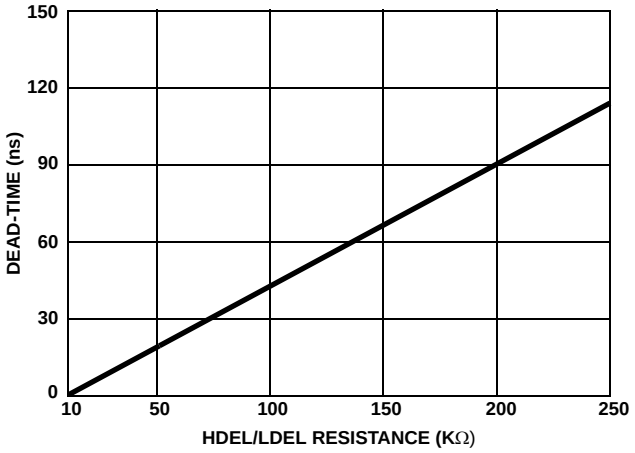


FIGURE 5. MINIMUM DEAD-TIME vs DEL RESISTANCE

Level-Translation

The lower power MOSFET gate drive signals from the propagation delay and control circuits go to amplification circuits which are described in more detail under the section "Driver Circuits". The upper power MOSFET gate drive signals are directed first to the Level-Translation circuits before going to the upper power MOSFET "Driver Circuits".

The Level-Translation circuit communicate "on" and "off" pulses from the Propagation Delay sub-circuit to the upper logic and gate drive sub-circuits which "float" at the potential of the upper power MOSFET source connections. This voltage can be as much as 85V when the bias supply voltage is only 10V (the sum of the bias supply voltage and bus voltages must not exceed 95VDC).

In order to minimize power dissipation in the level-shifter circuit, it is important to minimize the width of the pulses translated because the power dissipation is proportional to the product of switching frequency and pulse energy in joules. The pulse energy in turn is equal to the product of the bus voltage magnitude, translation pulse current and translation pulse duration. To provide a reliable, noise free pulse requires a nominal current pulse magnitude of approximately 3mA. The translated pulses are then "latched" to maintain the "on" or "off" state until another level-translation pulse comes along to set the latch to the opposite state. Very reliable operation can be obtained with pulse widths of approximately 80ns. At a switching frequency of even 1.0MHz, with an 80VDC bus potential, the power developed by the level-translation circuit will be less than 0.08W.

Charge Pump Circuits

There are two charge pump circuits in the HIP4080, one for each of the two upper logic and driver circuits. Each charge pump uses a switched capacitor doubler to provide about 30μA to 50μA of gate load current. The sourcing current charging capability drops off as the floating supply voltage increases. Eventually the gate voltage approaches the level set by an internal zener clamp, which prevents the voltage from exceeding about 15V, the safe gate voltage rating of most commonly available MOSFETs.

Driver Circuits

Each of the four output drivers are comprised of bipolar high speed NPN transistors for both sourcing and sinking gate charge to and from the MOSFET switches. In addition, the sink driver incorporates a parallel-connected N-channel MOSFET to enable the gate of the power switch gate-source voltage to be brought completely to 0V.

The propagation delays through the gate driver sub-circuits while driving 500pF loads is typically less than 10ns. Nevertheless, the gate driver design nearly eliminates all gate driver shoot-through which significantly reduces IC power dissipation.

Application Considerations

To successfully apply the HIP4080 the designer should address the following concerns:

- General Bias Supply Design Issues
- Upper Bias Supply Circuit Design
- Bootstrap Bias Supply Circuit Design

General Bias Supply Design Issues

The bias supply design is simple. The designer must first establish the desired gate voltage for turning on the power switches. For most power MOSFETs, increasing the gate-source voltage beyond 10V yields little reduction in switch drain-source voltage drop.

Overcharging the power switch's gate-source capacitance also delays turn-off, increases MOSFET switching losses and increases the energy to be switched by the gate driver of the HIP4080, which increases the dissipation within the HIP4080. Overcharging the MOSFET gate-source capacitance also can lead to "shoot-through" where both upper and lower MOSFETs in a single bridge leg find themselves on simultaneously, thereby shorting out the high voltage DC bus supply. Values close to 12V are optimum for supplying V_{DD} and V_{CC}, although the HIP4080 will operate up to 15V.

Lower Bias Supply Design

Since most applications use identical MOSFETs for both upper and lower power switches, the bias supply requirements with respect to driving the MOSFET gates will also be identical. If switching frequencies for driving upper and lower MOSFETs differ, two sets of calculations must be done; one for the upper switches and one for the lower switches. The bias current budget for upper and lower switches will be the sum of each calculation.

Always keep in mind that the lower bias supply must supply current to the upper gate drive and logic circuits as well as the lower gate drive circuits and logic circuits. This is due to the fact that the low side bias supplies (V_{CC}/V_{DD}) charge the bootstrap capacitors and the charge pumps, which maintain voltage across the upper power switch's gate-source terminals.

Good layout practice and capacitor bypassing technique avoids transient voltage dips of the bias power supply to the HIP4080. Always place a low ESR (equivalent series resistance) ceramic capacitor adjacent to the IC, connected between the bias terminals V_{CC} and V_{DD} and the common terminal, V_{SS} of the IC. A value in the range of 0.22μF and 0.5μF is usually sufficient.

Minimize the effects of Miller feedback by keeping the source and gate return leads from the MOSFETs to the HIP4080 short. This also reduces ringing, by minimizing the length and the inductance of these connections. Another way to minimize inductance in the gate charge/discharge path, in addition to minimizing path length, is to run the outbound gate lead directly "over" the source return lead. Sometimes the source return leads can be made into a small "ground plane" on the back side of the PC board making it possible to run the outbound gate lead "on top" of the board. This minimizes the "enclosed area" of the loop, thus minimizing inductance in this loop. It also adds some capacitance between gate and source which shunts out some of the Miller feedback effect.

Upper Bias Supply Circuit Design

Before discussing bootstrap circuit design in detail, it is worth mentioning that it is possible to operate the HIP4080 without a bootstrap circuit altogether. Even the bootstrap capacitor, which functions to supply a reservoir of charge for rapidly turning on the MOSFETs, is optional in some cases. In situations where very slow turn-on of the MOSFETs is tolerable, one may consider omitting some or all bootstrap components. Applications such as driving relays or lamp loads, where the MOSFETs are switched infrequently and switching losses are low, may provide opportunities for omitting the boot strap operation. Generally, loads with a lot of resistance and inductance are candidates.

Operating the HIP4080 without a bootstrap diode and/or capacitor will severely slow gate turn-on. Without a bootstrap capacitor, gate current only comes from the internal charge pump. The peak charge pump current is only about 30μA to 50μA. The gate voltage waveform, when operating without a bootstrap capacitor, will appear similar to the dotted line shown in Figure 6.

If a bootstrap capacitor value approximately equal to the equivalent MOSFET gate capacitance is used, the upper bias supply (labeled “bootstrap voltage” in Figure 6) will drop approximately in half when the gate is turned on. The larger the bootstrap capacitance used, the smaller is the instantaneous drop in bootstrap supply voltage when an upper MOSFET is turned on.

Although not recommended, one may employ a bootstrap capacitor without a bootstrap diode. In this case the charge pump is used to charge up a capacitor whose value should be much larger than the equivalent gate-source capacitance of the driven MOSFET. A value of bootstrap capacitance about 10 times greater than the equivalent MOSFET gate-source capacitance is usually sufficient. Provided that sufficient time elapses before turning on the MOSFET again, the bootstrap capacitor will have a chance to recharge to the voltage value that the bootstrap capacitor had prior to turning on the MOSFET. Assuming 2Ω of series resistance is in the bootstrap change path, an output frequency of up to $\frac{1}{5 \times 2\Omega \times C_{BS}}$ should allow sufficient refresh time.

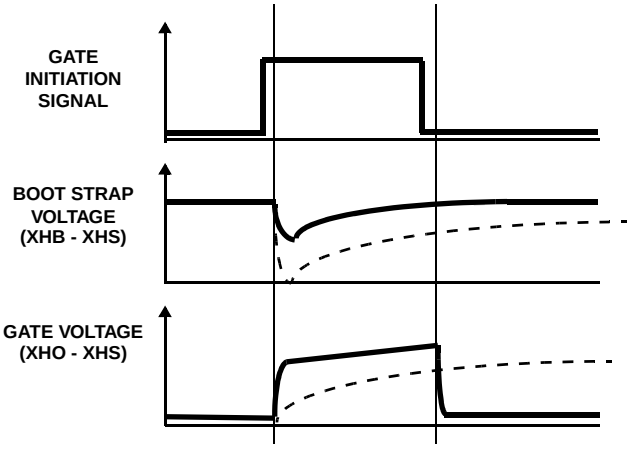


FIGURE 6.

A bootstrap capacitor 10 times larger than the equivalent gate-source capacitance of the driven MOSFET prevents the drop in bootstrap supply voltage from exceeding 10% of the bias supply voltage during turn-on of the MOSFET. When operating without the bootstrap diode the time required to replenish the charge on the bootstrap capacitor will be the same time as it would take to charge up the equivalent gate capacitance from 0V. This is because the charge lost on the bootstrap capacitor is exactly equal to the charge transferred to the gate capacitance during turn-on. Note that the very first time that the bootstrap capacitor is charged up, it takes much longer to do so, since the capacitor must be charged from 0V. With a bootstrap diode, the initial charging of the bootstrap supply is almost instantaneous, since the charge required comes from the low-side bias supply. Therefore, before any upper MOSFETs can initially be gated, time must be allowed for the upper bootstrap supply to reach full voltage. Without a bootstrap diode, this initial “charge” time can be excessive.

If the switching cycle is assumed to begin when an upper MOSFET is gated on, then the bootstrap capacitor will undergo a charge withdrawal when the source driver connects it to the equivalent gate-source capacitance of the MOSFET. After this initial “dump” of charge, the quiescent current drain experienced by the bootstrap supply is infinitesimal. In fact, the quiescent supply current is more than offset by the charge pump current.

The charge pump continuously supplies current to the bootstrap supply and eventually would charge the bootstrap capacitor and the MOSFET gate capacitance back to its initial value prior to the beginning of the switching cycle. The problem is that “eventually” may not be fast enough when the switching frequency is greater than a few hundred Hz.

Bootstrap Bias Supply Circuit Design

For high frequency applications all bootstrap components, both diodes and capacitors, are required. Therefore, one must be familiar with bootstrap capacitor sizing and proper choice of bootstrap diode.

Just after the switch cycle begins and the charge transfer from the bootstrap capacitor to the gate capacitance is complete, the voltage on the bootstrap capacitor is the lowest that it will ever be during the switch cycle. The charge lost on the bootstrap capacitor will be very nearly equal to the charge transferred to the equivalent gate-source capacitance of the MOSFET as shown in Equation 1.

$$Q_G = (V_{BS1} - V_{BS2}) \times C_{BS} \quad \text{(EQ. 1)}$$

where:

V_{BS1}= Bootstrap voltage immediately before turn-on
V_{BS2}= Bootstrap voltage immediately after turn-on
C_{BS} = Bootstrap Capacitance
Q_G **=** Gate charge transferred during turn-on

Were it not for the internal charge pump, the voltage on the bootstrap capacitor and the gate capacitor (because an upper MOSFET is now turned on) would eventually drain down to zero due to bootstrap diode leakage current and the very small supply current associated with the level-shifters and upper gate driver sub-circuits.

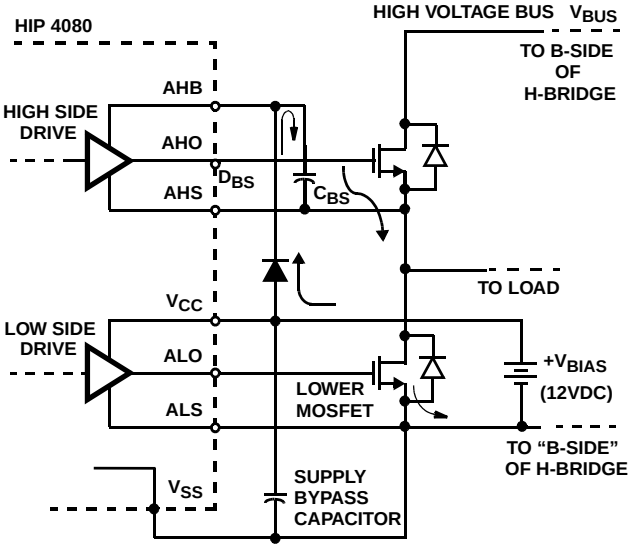
In PWM switch-mode, the switching frequency is equal to the reciprocal of the period between successive turn-on (or turn-off) pulses. Between any two turn-on gate pulses exists one turn-off pulse. Each time a turn-off pulse is issued to an upper MOSFET, the bootstrap capacitor of that MOSFET begins its “refresh” cycle. A refresh cycle ends when the upper MOSFET is turned on again, which varies depending

on the PWM frequency and duty cycle. As the duty cycle approaches 100%, the available “off-time”, t_{OFF} approaches zero. Equation 2 shows the relationship between t_{OFF}, f_{PWM} and the duty cycle.

$$t_{OFF} = (1 - DC)/f_{PWM} \quad \text{(EQ. 2)}$$

As soon as the upper MOSFET is turned off, the voltage on the phase terminal (the source terminal of the upper MOSFET) begins its descent toward the negative rail of the high voltage bus. When the phase terminal voltage becomes less than the V_{CC} voltage, refreshing (charging) of the bootstrap capacitor begins. As long as the phase voltage is below V_{CC} refreshing continues until the bootstrap and V_{CC} voltages are equal.

The off-time of the upper MOSFET is dependent on the gate control input signals, but it can never be shorter than the dead-time delay setting, which is set by the resistors connecting HDEL and LDEL to V_{SS}. If the bootstrap capacitor is not fully charged by the time the upper MOSFET turns on again, incomplete refreshing occurs. The designer must insure that the dead-time setting be consistent with the size of the bootstrap capacitor in order to guarantee complete refreshing. Figure 7 illustrates the circuit path for refreshing the bootstrap capacitor.



NOTE: Only “A-side” of H-bridge is shown for simplicity. Arrows show bootstrap charging path.

FIGURE 7. BOOTSTRAP CAPACITOR CHARGING PATH

The bootstrap charging and discharging paths should be kept short, minimizing the inductance of these loops as mentioned in the section, “Lower Bias Supply Design”.

Bootstrap Circuit Design - An Example

Equation 1 describes the relationship between the gate charge transferred to the MOSFET upon turn-on, the size of the bootstrap capacitor and the change in voltage across the bootstrap capacitor which occurs as a result of turn-on charge transfer.

The effects of reverse leakage current associated with the bootstrap diode and the bias current associated with the upper gate drive circuits also affect bootstrap capacitor sizing. At the instant that the upper MOSFET turns on and its source voltage begins to rapidly rise, the bootstrap diode becomes rapidly reverse biased resulting in a reverse recovery charge which further depletes the charge on the bootstrap capacitor. To completely model the total charge transferred during turn-on of the upper MOSFETs, these effects must be accounted for, as shown in Equation 3.

$$C_{BS} = \frac{Q_G + Q_{RR} + \frac{(I_{DR} + I_{QBS})}{f_{PWM}}}{V_{BS1} - V_{BS2}} \quad \text{(EQ. 3)}$$

where:

I_{DR} = Bootstrap diode reverse leakage current

I_{QBS} = Upper supply quiescent current

Q_{RR} = Bootstrap diode reverse recovered charge

Q_G = Turn-on gate charge transferred

f_{PWM} = PWM operating frequency

V_{BS1} = Bootstrap capacitor voltage just after refresh

V_{BS2} = Bootstrap capacitor voltage just after upper turn on

C_{BS} = Bootstrap capacitance

From a practical standpoint, the bootstrap diode reverse leakage and the upper supply quiescent current are negligible, particularly since the HIP4080’s internal charge pump continuously sources a minimum of about 30µA. This current more than offsets the leakage and supply current components, which are fixed and not a function of the switching frequency. The higher the switching frequency, the lower is the charge effect contributed by these components and their effect on bootstrap capacitor sizing is negligible, as shown in Equation 3. Supply current due to the bootstrap diode recovery charge component increases with switching frequency and generally is not negligible. Hence, the need to use a fast recovery diode. Diode recovery charge information can usually be found in most vendor data sheets.

For example, if we choose a Intersil IRF520R power MOSFET, the data book states a gate charge, Qg, of 12nC typical and 18nC maximum, both at V_{DS} = 12V. Using the maximum value of 18nC the maximum charge we should have to transfer will be less than 18nC.

Suppose a General Instrument UF4002, 100V, fast recovery, 1A, miniature plastic rectifier is used. The data sheet gives a reverse recovery time of 25ns. Since the recovery current waveform is approximately triangular, the recovery charge can be approximated by taking the product of half the peak reverse current magnitude (1A peak) and the recovery time duration (25ns). In this case the recovery charge should be 12.5nC.

Since the internal charge pump offsets any possible diode leakage and upper drive circuit bias currents, these sources of discharge current for the bootstrap capacitor will be ignored. The bootstrap capacitance required for the example above can be calculated as shown in Equation 4, using Equation 2.

$$C_{BS} = \frac{18nC + 12.5nC}{12.0 - 11.0} \quad \text{(EQ. 4)}$$

Therefore, a bootstrap capacitance of 0.033µF will result in less than a 1.0V droop in the voltage across the bootstrap capacitor during the turn-on period of either of the upper MOSFETs. If typical values of gate charge and bootstrap diode recovered charge are used rather than the maximum value, the voltage droop on the bootstrap supply will be only about 0.5V.

Power Dissipation and Thermal Design

One way to model the power dissipated in the HIP4080 is by lumping the losses into static losses and dynamic (switching) losses. The static losses are due to bias current losses for the upper and lower sections of the IC and include the sum of the I_{CC} and I_{DD} currents when the IC is not switching. The quiescent current is approximately 9mA. Therefore, with a 12V bias supply, the static power dissipation in the IC is slightly over 100mW.

The dynamic losses associated with switching the power MOSFETs are much more significant and can be divided into the following categories:

- Low Voltage Gate Drive (charge transfer)
- High Voltage Level-shifter (V-I) losses
- High Voltage Level-shifter (charge transfer)

In practice, the high voltage level-shifter and charge transfer losses are small compared to the gate drive charge transfer losses.

The more significant low voltage gate drive charge transfer losses are caused by the movement of charge in and out of the equivalent gate-source capacitor of each of the 4 MOSFETs comprising the H-bridge. The loss is a function of PWM (switching) frequency, the applied bias voltage, the equivalent gate-source capacitance and a minute amount of CMOS gate charge internal to the HIP4080. The low voltage charge transfer losses are given by Equation 5.

$$P_{SWLO} = f_{PWM} \times (Q_G + Q_{IC}) \times V_{BIAS} \quad \text{(EQ. 5)}$$

The high voltage level-shifter power dissipation is much more difficult to evaluate, although the equation which defines it is simple as shown in Equation 6. The difficulty arises from the fact that the level-shift current pulses, I_{ON} and I_{OFF}, are not perfectly in phase with the voltage at the upper MOSFET source terminals, V_{SHIFT} due to propagation delays within the IC. These time-dependent source voltages (or “phase” voltages) are further dependent on the gate capacitance of the driven MOSFETs and the type of load (resistive, capacitive or inductive) which determines how rapidly the MOSFETs turn on. For example, the level-shifter I_{ON} and I_{OFF} pulses may come and go and be latched by the upper logic circuits before the phase voltage even moves. As a result, little level-shift power dissipation may result from the I_{ON} pulse, whereas the I_{OFF} pulse may have a significant power dissipation associated with it, since the phase voltage generally remains high throughout the duration of the I_{OFF} pulse.

$$P_{SHIFT} = \frac{1}{T}\int_{O}^{T}(I_{ON}(t) + I_{OFF}(t)) \times V_{SHIFT}(t) \times dt \quad \text{(EQ. 6)}$$

Lastly, there is power dissipated within the IC due to charge transfer in and out of the capacitance between the upper driver circuits and V_{SS}. Since it is a charge transfer phenomena, it closely resembles the form of Equation 5, except that the capacitance is much smaller than the equivalent gate-source capacitances associated with power MOSFETs. On the other hand, the voltages associated with the level-shifting function are much higher than the voltage changes experienced at the gate of the MOSFETs. The relationship is shown in Equation 7.

$$P_{TUB} = C_{TUB} \times V_{SHIFT}^2 \times f_{PWM} \quad \text{(EQ. 7)}$$

The power associated with each of the two high voltage tubs in the HIP4080 derived from Equation 7 is quite small, due to the extremely small capacitance associated with these tubs. A “tub” is the isolation area which surrounds and isolates the high side circuits from the ground referenced circuits of the IC. The important point for users is that the power dissipated is linearly related to switching frequency and the square of the applied bus voltage.

The tub capacitance in Equation 7 varies with applied voltage, V_{SHIFT}, making its solution difficult, and the phase shift of the I_{ON} and I_{OFF} pulses with respect to the phase voltage, V_{SHIFT}, in Equation 6 are difficult to measure. Even the Q_{IC} in Equation 5 is not easy to measure. Hence the use of Equation 5 through Equation 7 to calculate total power dissipation is at best difficult. The equations do, however, allow users to understand the significance that MOSFET choice, switching frequency and bus voltage play in determining power dissipation. This knowledge can lead to corrective action when power dissipation becomes excessive.

Fortunately, there is an easy method which can be used to **measure** the components of power dissipation rather than **calculating** them, except for the tiny “tub capacitance” component.

Power Dissipation, the Easy Way

The average power dissipation associated with the IC and the gate of the connected MOSFETs can easily be measured using a signal generator, an averaging millimeter and a voltmeter.

Low Voltage Power Dissipation

Two sets of measurements are required. The first set uses the circuit of Figure 8 and evaluates all of the low voltage power dissipation components. These components include the MOSFET gate charge and internal CMOS charge transfer losses shown in Equation 5 as well as the quiescent bias current losses associated with the IC. The losses are calculated very simply by calculating the product of the bias voltage and current measurements as performed using the circuit shown in Figure 8. For measurement purposes, the phase terminals (AHS and BHS) for both A and B phases are both tied to the chip common, V_{SS} terminal, along with the lower source terminals, ALS and BLS. Capacitors equal to the equivalent gate-source capacitance of the MOSFETs are connected from each gate terminal to V_{SS}. The value of the capacitance chosen comes from the MOSFET manufacturers data sheet. Notice that the MOSFET data sheet usually gives the value in units of charge (usually nano-coulombs) for different drain-source voltages. Choose the drain-source voltage closest to the particular dc bus voltage of interest**.**

Simply substituting the actual MOSFETs for the capacitors, C_L, doesn't yield the correct average current because the Miller capacitance will not be accounted for. This is because the drains don't switch using the test circuit shown in Figure 8. Also the gate capacitance of the devices you are using may not represent the maximum values which only the data sheet will provide.

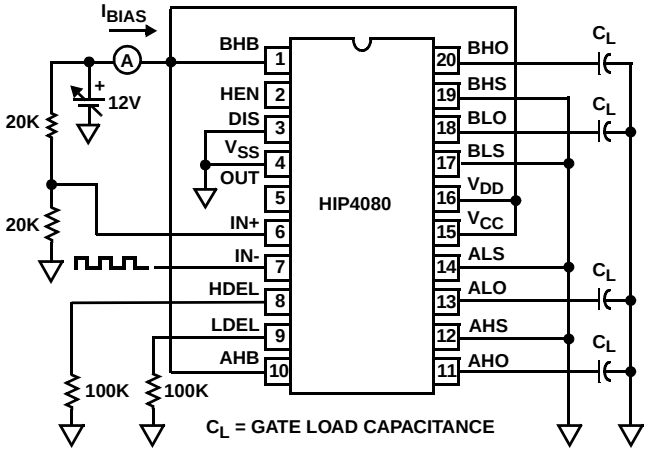


FIGURE 8. LOW VOLTAGE POWER DISSIPATION TEST CIRCUIT

The low voltage charge transfer switching currents are shown in Figure 9. Figure 9 does not include the quiescent bias current component, which is the bias current which flows in the IC when switching is disabled. The quiescent bias current component is approximately 10mA. Therefore the quiescent power loss at 12V would be 120mW. Note that the bias current at a given switching frequency grows almost proportionally to the load capacitance, and the current is directly proportional to switching frequency, as previously suggested by Equation 5.

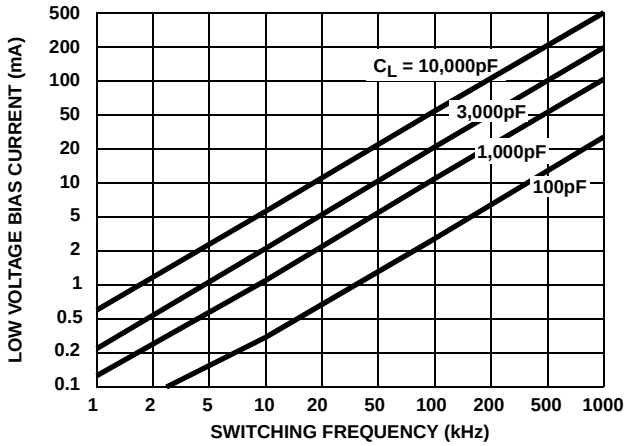


FIGURE 9. LOW VOLTAGE BIAS CURRENT vs FREQUENCY AND LOAD CAPACITANCE

High Voltage Power Dissipation

The high voltage power dissipation component is largely comprised of the high voltage level-shifter component as described by Equation 6. All of the difficulties associated with the time variance of the I_{ON} and I_{OFF} pulses and the level shift voltage, V_{SHIFT}, under the integrand in Equation 6 are avoided. For completeness, the total loss must include a small leakage current component, although the latter is usually smaller compared to the level-shifter component. The high voltage power loss calculation is the product of the high voltage bus voltage level, V_{BUS}, and the average high voltage bus current, I_{BUS}, as measured by the circuit shown

in Figure 10. Averaging meters should be used to make the measurements.

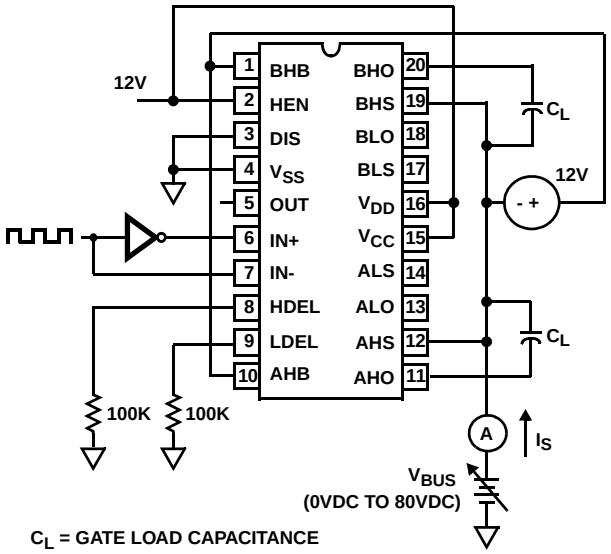


FIGURE 10. HIGH VOLTAGE LEVEL-SHIFT CURRENT TEST CIRCUIT

Figure 11 shows that the high voltage level-shift current varies directly with switching frequency. This result should not be surprising, since Equation 6 can be rearranged to show the current as a function of frequency, which is the reciprocal of the switching period, 1/T. The test circuit of Figure 10 measures quiescent leakage current as well as the switching component. Notice that the current increases somewhat with applied bus voltage. This is due to the finite output resistance of the level-shift transistors in the IC.

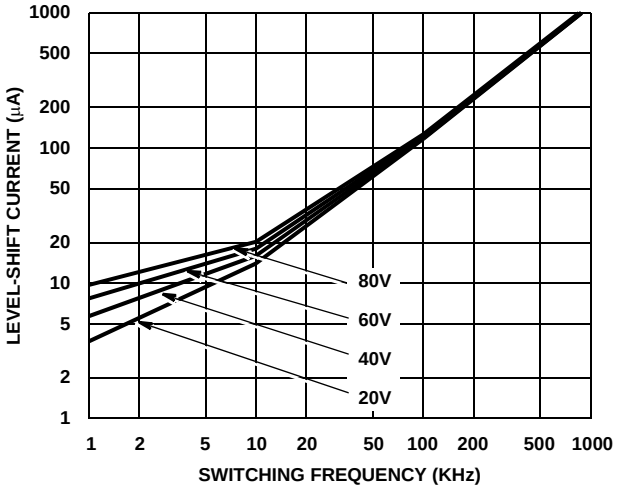


FIGURE 11. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

Layout Issues

In fast switching, high frequency systems, poor layout can result in problems. It is crucial to consider PCB layout. The HIP4080 pinout configuration encourages tight layout by placing the gate drive output terminals strategically along the right side of the chip (pin 1 is in the upper left-hand corner). This provides for short gate and source return leads connecting the IC with the power MOSFETs.

Minimize the series inductance in the gate drive loop by running the lead going out to the gate of the MOSFETs from the IC over the top of the return lead from the MOSFET sources back to the IC by using a double-sided PCB if possible. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The benefit is that the gate drive currents and voltages are much less prone to ringing which can similarly modulate the drain current of the MOSFET. The following table summarizes some of the layout problems which can occur and the corrective action to take.

Layout Problems and Effects

The Bootstrap circuit path should also be short to minimize series inductance that may cause the voltage on the bootstrap capacitor to ring, slowing down refresh or causing an overvoltage on the bootstrap bias supply.

A compact power circuit layout (short circuit path between upper/lower power switches) minimizes ringing on the phase lead(s) keeping BHS and AHS voltages from ringing excessively below the V_{SS} terminal which can cause excessive charge extraction from the substrate and possible malfunction of the IC.

Excessive gate lead lengths can cause gate voltage ringing and subsequent modulation of the drain current, thereby amplifying the Miller Effect.

PROBLEM	EFFECT
Bootstrap circuit path too long	Inductance may cause voltage on bootstrap capacitor to ring, slowing down refresh and/or causing an overvoltage on the bootstrap bias supply.
Lack of tight power circuit layout (long circuit path between upper/lower power switches)	Can cause ringing on the phase lead(s) causing BHS and AHS to ring excessively below the V_{SS} terminal causing excessive charge extraction from the substrate and possible malfunction of the IC.
Excessive gate lead lengths	Can cause gate voltage ringing and subsequent modulation of the drain current and impairs the effectiveness of the sink driver from minimizing the miller effect when an opposing switch is being rapidly turned on.

Quick Help Table

The quick help table has been included to help locate solutions to problems you may have in applying the HIP4080.

PROBLEM	EFFECT
Low chip bias voltages (V_{CC} and V_{DD})	May cause power MOSFETs to exhibit excessive R_{DSON}, possibly overheating them. Below about 6V, the IC may not function properly.
High chip bias voltages (V_{CC} and V_{DD})	At V_{DD} voltages above about 12V, The charge pump limiter will begin to operate, in turn drawing heavier V_{DD} current. Above 16V, Breakdown may occur.
Bootstrap capacitor(s) too small	May cause insufficient or soft charge delivery to MOSFETs at turn-on causing MOSFET overheating. Charge pump will pump charge, but possibly not quickly enough to avoid excessive switching losses.
Bootstrap capacitor(s) too large	Dead time may need to be increased in order to allow sufficient bootstrap refresh time. The alternative is to decrease bootstrap capacitance.
R_{GATE} too small	Smaller values of R_{GATE} reduces turn-on/off times and may cause excessive emi problems. Incorporating a series gate resistor with an anti-parallel diode can solve EMI problem and add to the dead time, reducing shoot-through tendency.
R_{GATE} too large	Increases switching losses and MOSFET heating. If anti-parallel diode mentioned above is in backwards, turn-off time is increased, but turn-on time is not, possibly causing a shoot-through fault.
Dead time too small	Reduces “refresh” time as well as dead time, with increased shoot-through tendency. Try increasing HDEL and LDEL resistors (don't exceed 1mΩ.)
HIP4080 IC gets too hot	Reduce bus voltage, switching frequency, choose a MOSFET with lower gate capacitance or reduce bias voltage (if it is not below 10V to 12V). Shed some of the low voltage gate switching losses in the HIP4080 by placing a small amount of series resistance in the leads going to the MOSFET gates, thereby transferring some of the IC losses to the resistors.
Lower MOSFETs turn on, but upper MOSFETs don't	Check that the HEN terminal is not tied low inadvertently.

Application Demonstration PC Board

Intersil has developed a demonstration PC board to allow fast prototyping of numerous types of applications. The board was also tailored to be used to aid in characterizing the HIP4080 and HIP4081 devices under actual operating conditions.

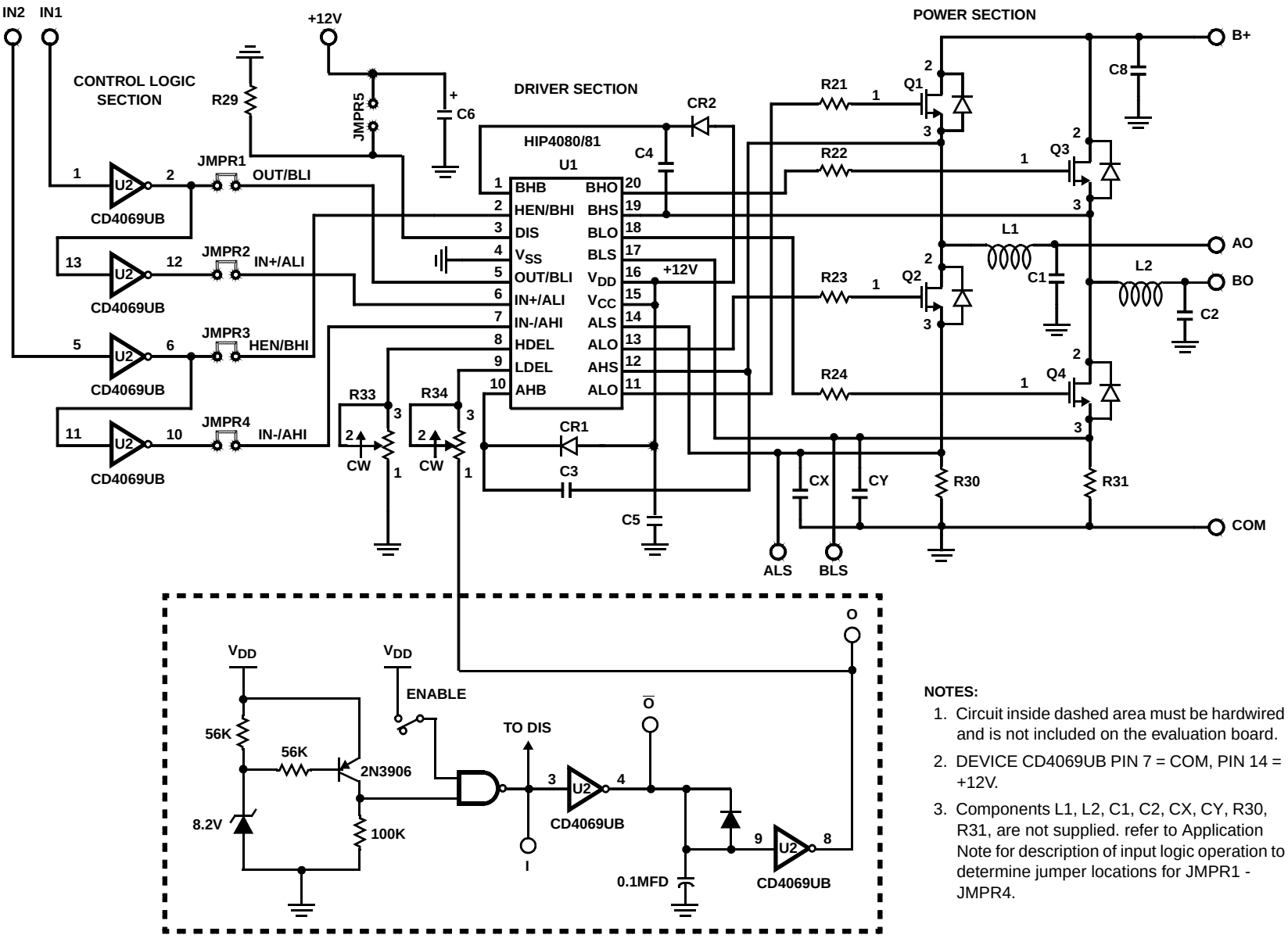
Figure 12 and Figure 13 show the schematic and the silkscreen indicating component placement, respectively, for the HIP4080/1 demo board. Note that the board can be used to evaluate either the HIP4080 or the HIP4081, simply by changing a few jumpers.

The PC board incorporates a CD4069UB to “buffer” inputs to the HIP4080 on input terminals IN1 and IN2. Normally the polarities of IN1 and IN2 should be opposite in polarity to obtain proper H-Bridge operation. If all 4 MOSFETs are to be PWM-ed, then JMPR3 should be removed (or opened). Also the OUT terminal of the IC should not be driven, so insure JMPR1 is open. Specific recommendations for working with the HIP4081 will be discussed in the corresponding section of the application note for the HIP4081. JMPR5 should always be removed in order to implement the power up reset circuit described in data sheet HIP4080, File Number 3178. Resistors R27 and R28 as well as capacitor, C7 are not required.

Consistent with good design practice, the +12V bias supply is bypassed by capacitors C6 and C5 (at the IC terminals directly). Capacitor C6 is a 4.7μF tantalum, designed to bypass the whole PCB, whereas C5 is a 0.22μF, designed to bypass the HIP4080. The bootstrap capacitors, C3 and C4, and the high voltage bus bypass capacitors are 0.1μF, 100V ceramic. Ceramic is used here because of the low inductance required of these capacitors in the application. The bootstrap diodes are 1A, fast recovery (t_{RR} = 200ns), 100V, to minimize the charge loss from the bootstrap capacitors when the diodes become reverse-biased.

The MOSFETs supplied with the demo board is a Intersil IRF520, 100V, 9A device. Since it has a gate charge of approximately 12nC, 10Ω gate resistors, R21 through R24, have been employed to deliberately slow down turn-on and turn-off of these switches. Finally, R33 and R34 provide adjustment of the dead-time. These are 500kΩ normally set for 100kΩ, which will result in a dead-time of approximately 50ns. Resistors, R30 and R31 are shunt resistors (0.1Ω, 2W, 2%, wirewound) used to provide a current-limiting signal, if desired. These may be replaced with wire jumpers if not required.

Finally, space has been provided for filter reactors, L1 and L2, and filter capacitors, C1 and C2, to provide filtering of PWM switching components from appearing at output terminals AO and BO. To facilitate placement of user-defined ICs, such as op-amps, comparators, etc., space for 3 fourteen pin standard width ICs has been reserved at the far left side of the demo board. The output terminations of the 3 optional locations are wired to holes which can be used to mount application-specific components, easing the process for building up working amplifiers for motor controls and audio amplifiers.



NOTES:

1. Circuit inside dashed area must be hardwired and is not included on the evaluation board.
2. DEVICE CD4069UB PIN 7 = COM, PIN 14 = +12V.
3. Components L1, L2, C1, C2, CX, CY, R30, R31, are not supplied. refer to Application Note for description of input logic operation to determine jumper locations for JMPR1 - JMPR4.

FIGURE 12. HIP4080 EVALUATION PC BOARD SCHEMATIC

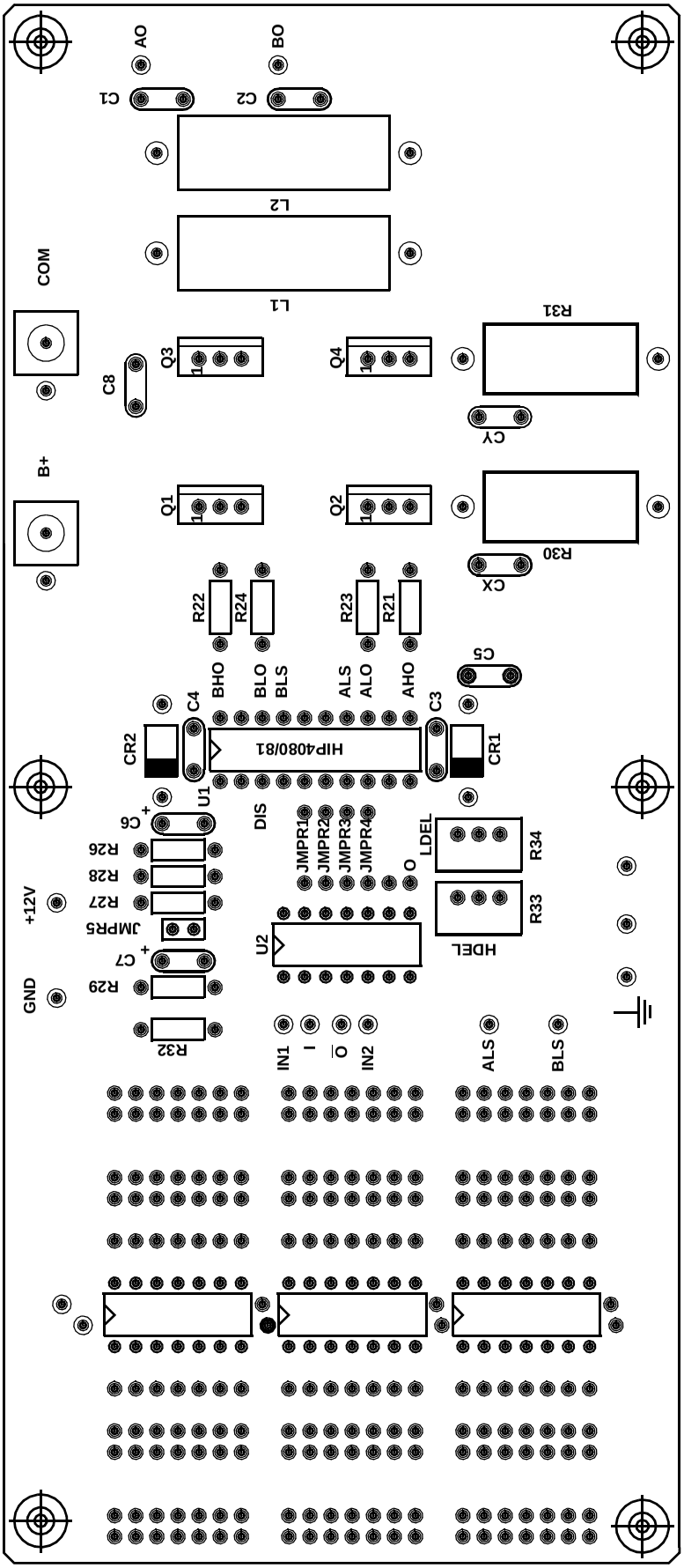


FIGURE 12. EVALUATION BOARD SILKSCREEN

Supplemental Information for HIP4080 and HIP4081 Power-up Application

The HIP4080 and HIP4081 H-Bridge Driver ICs require external circuitry to assure reliable start-up conditions of the upper drivers. If not addressed in the application, the H-bridge power MOSFETs may be exposed to shoot-through current, possibly leading to MOSFET failure. Following the instructions below will result in reliable start-up.

HIP4081

The HIP4081 has four inputs, one for each output. Outputs ALO and BLO are directly controlled by input ALI and BLI. By holding ALI and BLI low during start-up no shoot-through conditions can occur. To set the latches to the upper drivers such that the driver outputs, AHO and BHO, are off, the DIS pin must be toggled from low to high after power is applied. This is accomplished with a simple resistor divider, as shown below in Figure 14. As the V_{DD}/V_{CC} supply ramps from zero up, the DIS voltage is below its input threshold of 1.7V due to the R1/R2 resistor divider. When V_{DD}/V_{CC} exceeds approximately 9V to 10V, DIS becomes greater than the input threshold and the chip disables all outputs. It is critical that ALI and BLI be held low prior to DIS reaching its threshold level of 1.7V while V_{DD}/V_{CC} is ramping up, so that shoot through is avoided. After power is up the chip can be enabled by the ENABLE signal which pulls the DIS pin low.

HIP4080

The HIP4080 does not have an input protocol like the HIP4081 that keeps both lower power MOSFETs off other than through the DIS pin. IN+ and IN- are inputs to a comparator that control the bridge in such a way that only one of the lower power devices is on at a time, assuming DIS is low. However, keeping both lower MOSFETs off can be accomplished by controlling the lower turn-on delay pin, LDEL, while the chip is enabled, as shown in Figure 15. Pulling LDEL to V_{DD} will indefinitely delay the lower turn-on delays through the input comparator and will keep the lower MOSFETs off. With the lower MOSFETs off and the chip enabled, i.e., DIS = low, IN+ or IN- can be switched through a full cycle, properly setting the upper driver outputs. Once this is accomplished, LDEL is released to its normal operating point. It is critical that IN+/IN- switch a full cycle while LDEL is held high, to avoid shoot-through. This start-up procedure can be initiated by the supply voltage and/or the chip enable command by the circuit in Figure 15.

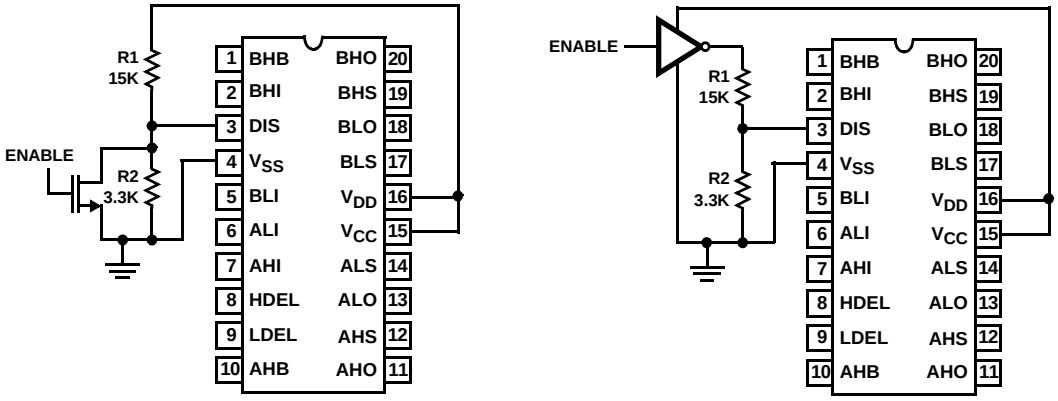


FIGURE 13.

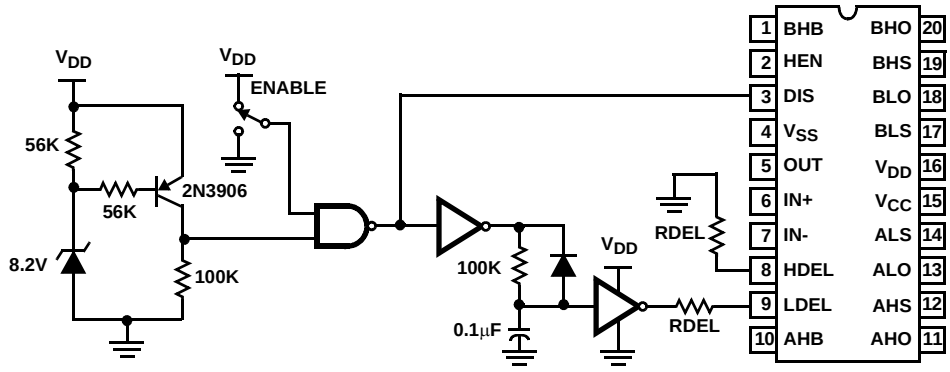
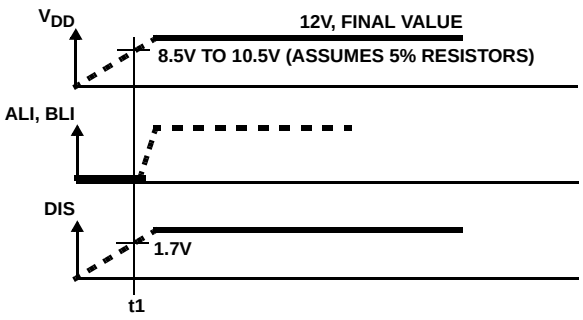


FIGURE 14.

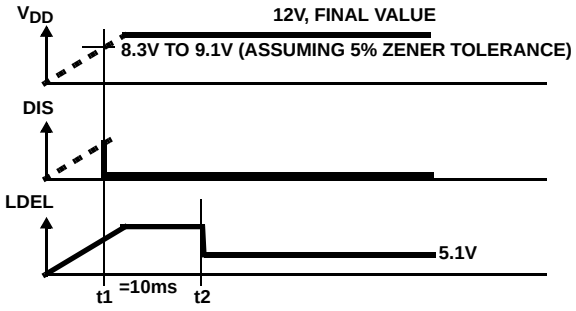
Timing Diagrams



NOTE:

1. ALI and/or BLI may be high after t1, whereupon the ENABLE pin may also be brought high.

FIGURE 15.



NOTE:

1. Between t1 and t2 the IN+ and IN- inputs must cause the OUT pin to go through one complete cycle (transition order is not important). If the ENABLE pin is low after the undervoltage circuit is satisfied, the ENABLE pin will initiate the 10ms time delay during which the IN+ and IN- pins must cycle at least once.

FIGURE 16.