HA5020 Operational Amplifier Feedback Resistor Selection

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Optimum AC performance of current feedback amplifiers in general and of the HA-5020 in particular depends upon careful selection of the feedback resistor, R_F. The benefit of higher usable bandwidth (compared with conventional voltage feedback amplifiers) and the ability to control the frequency response (by choosing the value of R_F) carries an expense in that the design process becomes more complicated. This is particularly true if an intuitive knowledge of how the device will behave in the end application is lacking. The purpose of this App Note is to provide a conceptual foundation on which this intuitive knowledge can be built.

The choice of the optimum resistor value depends upon design goals for the application subject to conditions of closed loop gain, source impedance, and load. As a point of reference, typical curves are provided in the data sheet that show how the frequency response is affected by closed loop gain, feedback resistor value, and load resistance. Source impedance, if it is large, becomes a factor only in conjunction with capacitance at the inputs. The data sheet curves are all generated with a 50Ω source impedance.

To illustrate how one might approach the problem of selecting a feedback resistor based on closed loop gain, consider the simple model of Figure 1. Between the inputs is a unity gain voltage buffer with non-zero output impedance indicated by R_I. The transimpedance gain, R_Z, is a function of frequency having a high DC value that forces I_ε to zero. The model's behavior is influenced by external elements consisting of a feedback network (R_F and R_G), source and load impedances (R_S and R_L), and stray capacitance at the amplifier's inputs (C_S).

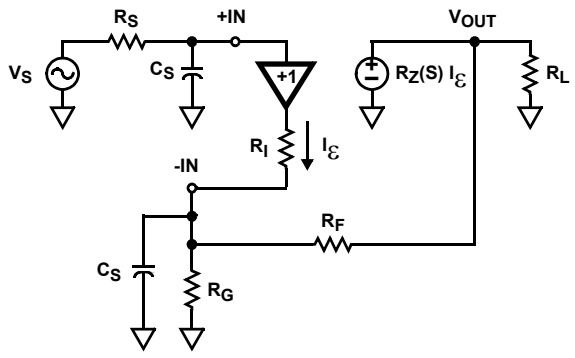

FIGURE 1. SIMPLE CURRENT FEEDBACK AMPLIFIER MODEL

Derivation of the transfer function will confirm that the non-zero inverting input impedance, R_I, causes the circuit's bandwidth to degrade as the closed loop gain increases, while stray capacitance at the negative input gives rise to gain peaking particularly at low gains (intuitively, C_S is in parallel with R_G causing the gain as determined by the feedback network to increase with frequency).

Gain peaking due to capacitance at the inverting input is most easily dealt with by placing a resistor in series with the positive input. If we assume that the stray capacitance at the positive input equals the stray at the negative input, we can choose R_S equal to the parallel combination of R_F and R_G. This introduces a pole at the positive input which cancels the zero at the negative input, thereby eliminating the gain peak. Note that any remaining gain peaking is a result of excessive phase shift around the loop. Excess phase shift around the loop can be reduced by increasing R_F.

Bandwidth degradation due to non-zero inverting input resistance is also easy to deal with as long as the product of the closed loop gain and the inverting input resistance does not exceed the optimum value for R_F in unity gain. By solving the transfer function for constant bandwidth, we arrive at the following equations for R_F and R_G:

$$R_F = R_{FO} - A_{CL} * R_I \quad \text{(EQ. 1)}$$

$$R_I = R_F / (A_{CL} - 1) \quad \text{(EQ. 2)}$$

Where,

R_{FO} is the optimum value for unity gain (1000Ω),

R_I is the inverting input impedance (75Ω), and

A_{CL} is the desired closed loop gain.

A comparison between actual measured results in Figures 2 and 3 provides graphic reinforcement for the utility of these equations. Figure 2 illustrates the failure to consider stray input capacitance and inverting input resistance, while Figure 3 incorporates the lessons learned from analyzing our simple model.

In Figure 2, a family of closed loop gain curves was obtained on a representative unit using R_S = 50Ω and constant R_F ($R_F = R_{FO}$ = 1000Ω). The measured stray capacitance at either input was 2pF. The results in Figure 3 were obtained from the same unit, except that (within the constraints of available standard resistor values) R_F and R_G were chosen according to the equations above and R_S was chosen to be equal to the parallel combination of R_F and R_G.

One limitation of the above model is that it does not include the effects of the load. In general if R_L is 400Ω or above, the response is independent of the load. If R_L is less than 400Ω, the response becomes more damped and the bandwidth degrades. Here again the bandwidth degradation can be compensated for by lowering the value of R_F.

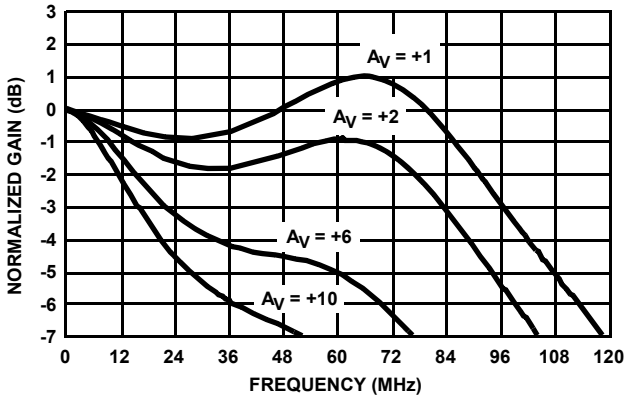

FIGURE 2. FREQUENCY RESPONSE vs CLOSED LOOP GAIN USING FIXED R_F = 1kΩ, R_S = 50Ω, R_L = 402Ω

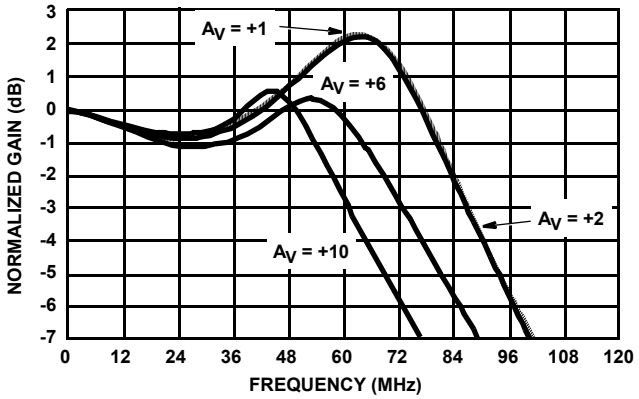

FIGURE 3. FREQUENCY RESPONSE vs CLOSED LOOP GAIN R_F = 1000-A_V(75Ω), R_S = R_F || R_G, R_L = 402Ω

TABLE 1. RESISTOR VALUES FOR FIGURE 2

A_V	R_F (Ω)	R_G (Ω)	R_S (Ω)	BW (MHz)	PEAKING (dB)
+1	1K	-	50	97	1
+2	1K	1K	50	84	<0
+6	1K	200	50	22	<0
+10	1K	110	50	16	<0

TABLE 2. RESISTOR VALUES FOR FIGURE 3

A_V	R_F (Ω)	R_G (Ω)	R_S (Ω)	BW (MHz)	PEAKING (dB)
+1	909	-	909	87	2
+2	825	825	422	87	2
+6	562	110	90.9	74	0.5
+10	237	26.1	23.7	62	0.5

NOTE: R_F = 1000-A_V(75Ω), R_S = R_F || R_G, R_L = 402Ω

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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