Introduction

Table 1 shows the wide range of high-speed ADC's available from Intersil. Maintaining the accuracy of these converters in a high-speed environment can be quite a challenge. This note will point out considerations for board layout, grounding, power management, and suggest various support circuits.

Board Layout, Ground and Power Considerations

The cost of multilayer boards has decreased to the point where they are now commonly used with high-speed mixed signal circuits. This technology enables the use of solid ground and power planes which will result in the lowest impedance possible while minimizing any shared impedances. Figure 1 illustrates the sequencing of the layers used on the HI1276 evaluation board. The dimensions called out were those required to achieve 50Ω microstrip for the signal lines.

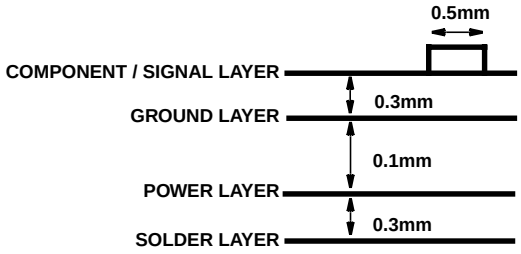


FIGURE 1. HI1276 EVALUATION BOARD LAYERS

There are many board layout techniques that can be used on a mixed signal board to keep digital noise from corrupting the analog signal path. The ground layer should be separated into an analog and a digital ground with an eighth of an inch spacing between them to minimize coupling.Analog components should be separated from the digital components. This is simplified if the converter has separate analog and digital supply and ground pins making it fairly obvious where to locate the components in relation to the ADC.

TABLE 1. Intersil HIGH-SPEED CONVERTERS

TABLE	BITS	CONVERSION SPEED	LOGIC LEVELS	INPUT BANDWIDTH	TECHNOLOGY
CA3304	4	25 MSPS	CMOS	13MHz	CMOS Flash
CA3306	6	18 MSPS	CMOS	9MHz	CMOS Flash
HI5701	6	30 MSPS	CMOS/TTL	20MHz	CMOS Flash
CA3318	8	15 MSPS	CMOS	2.5MHz	CMOS Flash
HI5700	8	20 MSPS	CMOS/TTL	18MHz	CMOS Flash
HI1175	8	20 MSPS	CMOS	18MHz	CMOS Two-Step
HI1176	8	20 MSPS	CMOS	18MHz	CMOS Two-Step
HI1386	8	75 MSPS	ECL	150MHz	BIPOLAR Flash
HI1396	8	125 MSPS	ECL	200MHz	BIPOLAR Flash
HI1166	8	250 MSPS	ECL	200MHz	BIPOLAR Flash
HI1276	8	500 MSPS	ECL	300MHz	BIPOLAR Flash
HI5800	12	3 MSPS	TTL	20MHz	BICMOS Two-Step

Position the components and signal lines over their corresponding analog or digital ground plane. This will minimize inductive loops, and thereby reduce ringing and magnetic coupling into sensitive analog areas. It also results in a certain measure of high frequency decoupling on the supply lines. Route all controlled impedance signal lines on the component layer minimizing the number of through holes. The holes will make it difficult to maintain a controlled impedance and will tend to generate additional noise on the board. Additional power or noncontrolled impedance signal lines could be run on the solder side. Pay particular attention to the analog input and reference traces to the ADC. Route them so as to minimize capacitive coupling from any digital lines. Unexpected frequency components in a spectrum plot for the ADC might be caused by digital noise coupling onto the analog traces. It is especially critical for the ECL converters with multiple V_{IN} pins to equalize the line lengths to these pins.

The analog and digital grounds should only be tied together in one place. The choices are under the ADC, at the edge of the board, or back at the supplies. When the system has a single ADC then the best place is usually under the ADC. A wise decision in the prototype phase of a design is to allow for all three choices so the optimum scheme can be determined. **Do not** tie the grounds together back at the supplies and under the ADC. This will create a ground loop and generate additional noise. If the system has multiple ADC's, then treat each one as an analog part, and group it close to the other analog components. Tie the grounds together either at the edge of the board or back at the supplies.

Avoid mounting high-speed converters in IC sockets. Their parasitic resistance, inductance, and capacitance will usually degrade the performance of the part. Instead use "Pin Sockets" Amp Part No. 5-330808-3.

All the parts in Table 1, except the CA3304 and CA3318, have evaluation boards available. Copies of the layout are provided with the documentation that comes with the board, and it is suggested that it be used in a system design to get the best performance from the part.

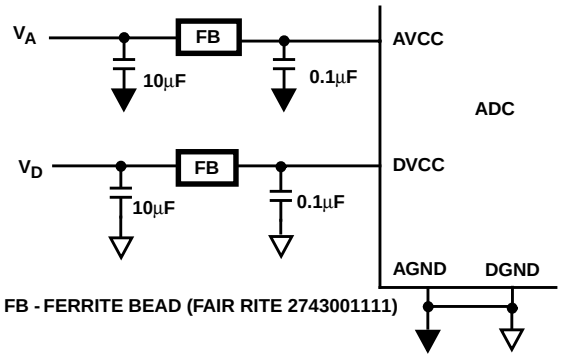


FIGURE 2. SUGGESTED POWER SCHEME

Again, in the interest of keeping digital noise out of the analog signal path, the ADC should have separate analog and digital supplies. Figure 2 shows a suggested scheme for bypassing the supplies. Each supply is bypassed to its respective ground. A 10µF tantalum cap is usually placed at the edge of the board to keep any low frequency noise from getting on the board. Since a bulk capacitor will look inductive at higher frequencies, an additional 0.1µF chip cap is placed at the ADC supply pins. The ferrite bead performs two functions. First, it will damp the resonant circuit formed by the 10µF cap, the parasitic inductance of the trace to the power pin of the ADC, and the 0.1µF cap. And, if system cost constraints do not allow separating the analog and digital supplies, then the bead will keep the digital noise off the analog supply.

The HI1175 could latchup if at power up there is a time skew between the analog and digital supplies. Therefore, do not separate these supplies or insert a ferrite bead between them, but instead tie both to the +5V analog supply.

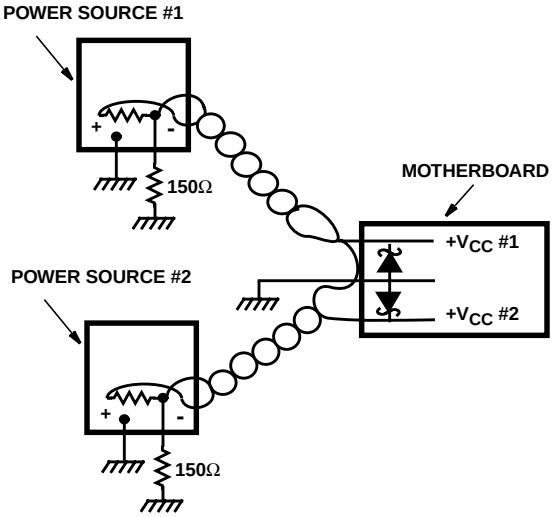


FIGURE 3. REMOTE POWER SUPPLY CONNECTIONS

Figure 3 is a suggested scheme for bringing power to a motherboard with remote power supplies. The analog and digital grounds are tied together at the edge of the board along with earth ground. Allow for a large number of ground connections to the board to minimize voltage drops across the backplane. Notice the use of twisted pair lines to minimize the inductance of the supply lines. The 150Ω resistor ensures that the power supplies have a reference to earth ground at all times and is large enough to prevent ground-loop currents.

Try to avoid using switching power supplies whenever possible. The large spikes, 100mV or more at about 100kHz, found on these supplies have frequency components that can extend into many megahertz. Since the PSRR of the ADC will tend to rolloff significantly from its DC value, there can be a reduction in the overall signal to noise ratio (SNR) of the converter. If it is necessary to use a switching power supply, then filter its output with commercially available DC power filters. A linear regulator could also be used to provide a certain amount of isolation on an analog supply.

References

A number of factors must be considered when designing a reference for a converter. Accuracy must be maintained over the temperature range of the ADC, and the noise it generates must not degrade the SNR of the converter. The reference voltage terminals for a flash converter are typically subjected to internal transient currents during conversion. Therefore, it is important to drive the ADC reference pin from a low impedance source and to decouple thoroughly between the $V_{REF}+$ and $V_{REF}-$ pins. The reference must also be able to drive the low impedance of the reference ladder (as low as 75Ω for the ECL flash converters).

Figure 4 is a reference circuit capable of producing a positive and a negative reference voltage of about 4V that has a 40ppm/^{o}C drift over temperature. The positive side of the reference could be used with the CMOS converters, while the negative side could be used with the ECL parts. The feedforward and feedback resistors of the op-amps would be scaled for the required reference voltage.The HI1166 and HI1276 have the provision for bypassing the Rs parasitic resistance using the sense pins (V_{RTS} and V_{RBS}). All the other flashes do not have this option, so they would close the feedback loop at the converter reference input pin.

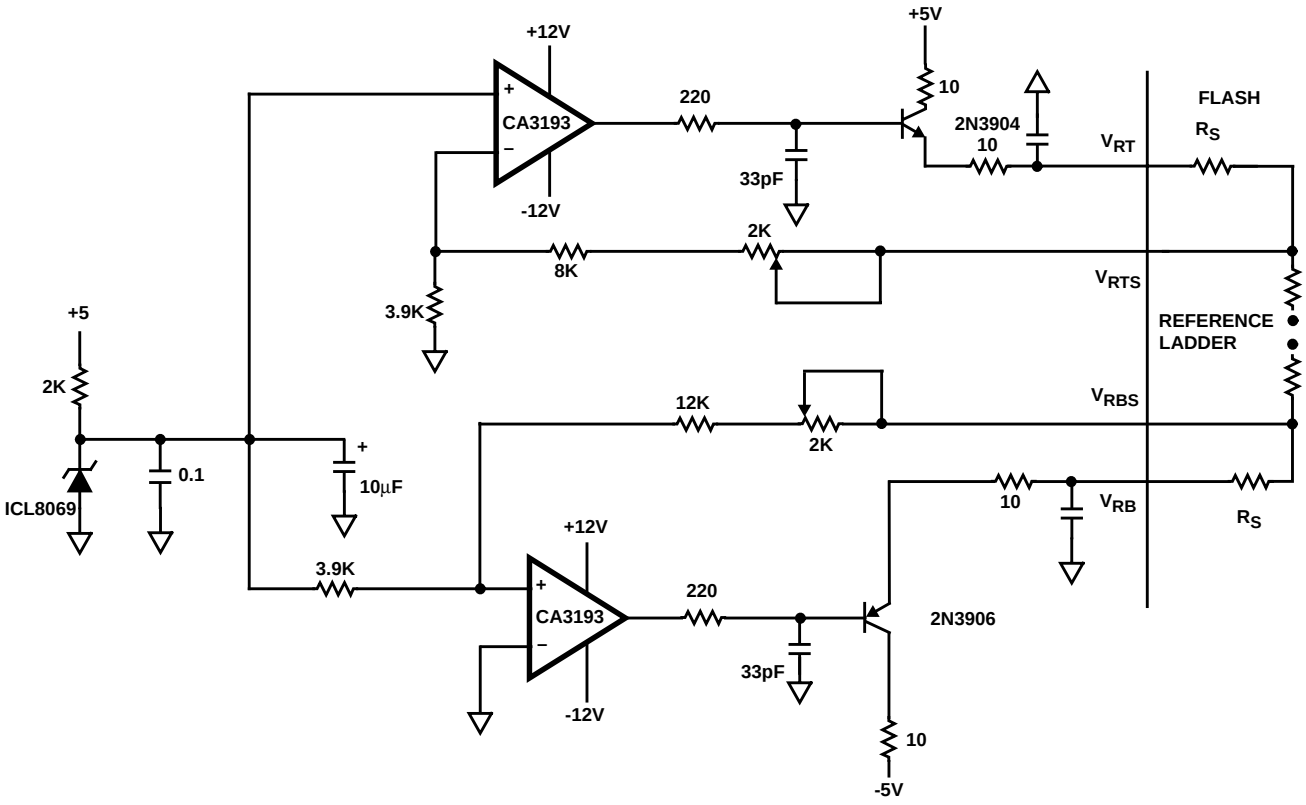


FIGURE 4. FLASH REFERENCE CIRCUIT

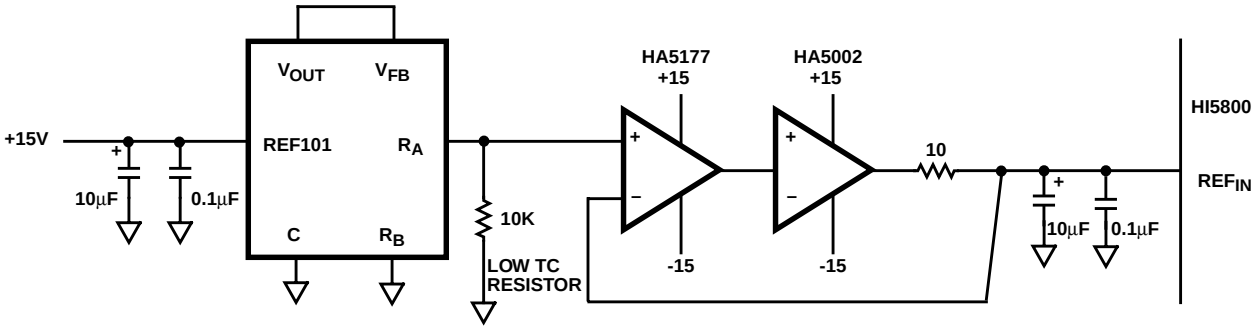


FIGURE 5. HI5800 REFERENCE CIRCUIT

The CA3306 has an internal 6.2V zener that can be used to generate the reference voltage for the part. However, this technique is not recommended for converters with greater than 6 bits of resolution, because of the noise generated by the zener diode. For these parts, a bandgap reference such as the ICL8069 should be used.

The internal reference for the HI1175 and HI1176 are resistors to +5V and ground that in combination with the reference ladder sets V_{RT} to 2.6V and V_{RB} to 0.6V. These voltages are specified at a nominal supply and will be very sensitive to the actual supply voltage used in a system. Bypass the V_{RT} and V_{RB} pins heavily in order to ensure that power supply noise does not get into the converter reference.

The HI5800 12 bit sampling converter has an internal 2.5V 20ppm/^{O}C reference. If a user decides to provide an external reference, then they will be faced with various problems. The drift of the reference over temperature must be low, and it also must be capable of driving the 200Ω input impedance seen at the REF_{IN} pin of the HI5800. Figure 5 is a recommended circuit for doing this that is capable of 2ppm/^{O}C drift over temperature. Notice that in this case a REF101 is used to supply the reference voltage capable of 12 bit performance. A slightly cheaper REF102 can be used if a larger T_C can be tolerated.

Analog Input Buffers

In general, the analog input to an ADC needs to be amplified or buffered for the following reasons: to adjust gain and offset, to sink any spurious clock kickback generated during the conversion process, to drive the ADC's input capacitance, or to maintain circuit bandwidth.

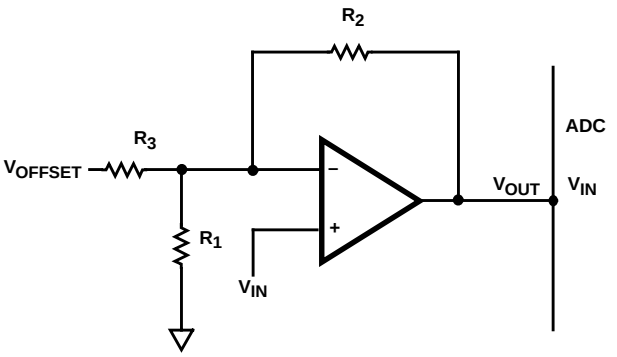


FIGURE 6. NON INVERTING AMPLIFIER

Figure 6 is an example of a high input impedance noninverting amplifier that will level shift an input to an offset determined by V_{OFFSET}. The gain can be calculated from:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1 || R_3}\right) \times V_{IN} - \left(\frac{R_1}{R_1 + R_3}\right) \times V_{OFFSET}$$

$$R_1 || R_3 = \frac{R_1 \times R_3}{R_1 + R_3}$$

Figure 7 is an example of an amplifier that will also offset the input depending on V_{OFFSET}; but, in this case, the input will be inverted and the input impedance is equal to the value of R1. The equation for the circuit gain is:

$$V_{OUT} = \left(-\frac{R_2}{R_1}\right) \times V_{IN} - \left(\frac{R_2}{R_3}\right) \times V_{OFFSET}$$

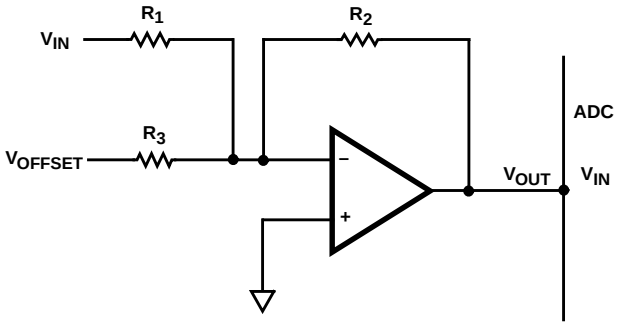


FIGURE 7. INVERTING AMPLIFIER

These circuits could be used to level shift unipolar inputs to the ±2.5V range of the HI5800 or translate them up to the levels required by the HI1175 and HI1176.

Several factors need to be considered when selecting an amplifier to drive an ADC. First, the DC performance of the amplifier must match the desired system accuracy. Refer to references 1, 2, and 3 for an excellent discussion of the differences between voltage and current feedback op-amps and the DC accuracy that can be expected of them.

TABLE 2. BANDWIDTH APPROXIMATIONS

INPUT SIGNAL	APPROXIMATE BANDWIDTH REQUIRED
Pulsating DC	Rate Of Change (V/s)/1V
Sinusoidal	1/Period
Complex Periodic	20/Fundamental Period
Single Event	1/Pulse Width

Table 2 shows some of the first-pass approximations of the required bandwidth for a given type of input signal. The nyquist criterion would then set the minimum sampling rate at twice the bandwidth.

There are a number of reasons why the bandwidth of the input circuitry to the ADC is usually much wider than these approximations. All applications will suffer a loss of dynamic range as the input to the ADC approaches the -3dB bandwidth. In CCD or muxed input applications (pulsating DC) a wide bandwidth system will settle faster to a new input and recover quicker from an overrange. Signal distortion of baseband (sinusoidal) or pulse signals (complex periodic) will be avoided if the input is operating over a flat portion of the system frequency response and has a zero phase shift over its entire frequency range. A more realistic goal is a phase shift that is proportional to frequency. That is, the second har-

monic should be delayed twice as much as the fundamental, the third three times as much, and so on. When this occurs, all the frequency components will end up having the same amount of time delay resulting in a signal that is only delayed slightly in time and can easily be adjusted for.

For a single pole system, the attenuation factor and phase shift at a particular frequency relative to the f_{-3dB} can be calculated from:

$$A(f) = \frac{1}{\sqrt{1+\left(\frac{f}{f_{-3dB}}\right)^2}} \quad (1) \text{ and } \quad \Theta(f) = \operatorname{atan}\left(\frac{f}{f_{-3dB}}\right) \quad (2).$$

Taking these error terms into account, the complete equation for a sinewave including the effects of the system would now be:

$$V(t) = \frac{A}{\sqrt{1+\left(\frac{f}{f_{-3dB}}\right)^2}} \times \sin\left(\omega t + \operatorname{atan}\left(\frac{f}{f_{-3dB}}\right)\right)$$

.

Once the phase shift has been calculated the corresponding time delay at frequency f will be:

$$T_D = \frac{\Theta(f)}{360 \times f}$$

.

In equation 1, when f equals 4MHz (video) and the attenuation A(f) is one 8 bit lsb (0.4%), the required small signal bandwidth f_{3dB} would be 40MHz. The corresponding phase shift at 4MHz would be 5.7^o and the time delay is 4ns. Consult the datasheet for a particular op-amp to find out if it will provide the desired gain flatness and phase response over the required bandwidth. Keep in mind the signal levels required for a full scale swing to the ADC and at what level the bandwidth for the op-amp is specified. There are many ways to spec the bandwidth of a converter, but the important point is its accuracy at the desired operating frequencies.

Figure 8 is a model for the analog input circuit for a typical flash converter. The inductance L includes the lead inductance of the part and the inductance due to the V_{IN} trace on the board. Resistor R includes the output resistance of the op-amp.

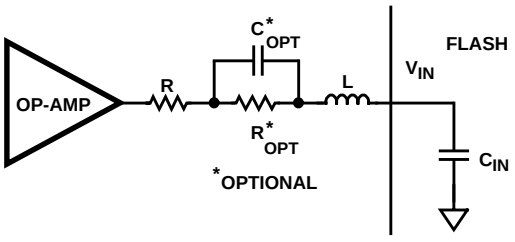


FIGURE 8. FLASH INPUT CIRCUIT

The circuitry driving the analog input of one of the 8 bit ECL flashes must drive 255 bipolar comparators. Each comparator will have a parasitic capacitance formed by a reverse biased p-n semiconductor junction. The capacitance will be a nonlinear function of voltage and temperature. Normally, the ADC analog input would present a total capacitive load (C_{IN}) which would also vary depending on the state of the comparators internal to the converter. However, the design used in the Intersil ECL converters has minimized this effect and the resulting kickback on the analog input.

The circuit in Figure 8 can be optimized for a particular ECL flash and board layout by the proper selection of resistor R. Too low a value for R will cause peaking in the frequency response and too high a value will result in a loss of bandwidth. The process to select the correct value for R will involve plotting the bandwidth for the total system at a number of different values of R. In some cases additional bandwidth can be gained by adding Ropt and Copt but it will require a more complicated selection process. A user should refer to the evaluation board available for a particular ADC for a suggested layout, op-amp, and component values.

The input capacitance (C_{IN}) for a CMOS flash depends on the state of the convert clock signal. For example, the analog input capacitance of the HI5700 is typically 60pF during the sample phase and 15pF during the auto-balance phase. The charging current for these capacitors will generate a current pulse that is present at the input at the beginning of every sample and auto-balance period. The peak current transient is dependent upon the applied voltage, input capacitance during sample phase, and the driving source impedance. Ideally, the input to the ADC should settle fast enough in one sample period so the accuracy of the conversion is not degraded. These transients can be quite large for the CMOS converters and is the primary reason why a wide bandwidth buffer is always recommended to drive the analog input to these parts.

The circuit depicted in Figure 8 can be tuned for the best settling time for a particular CMOS ADC by the proper choice of R and will occur when:

$$R = 2 \times \sqrt{\left(\frac{L}{C}\right)}$$

.

Since the values for R and L are hard to quantify, the calculated value will probably have to be adjusted a few ohms one way or the other in an actual system before an optimum value is found. An R of 27Ω was determined to be appropriate for a HA5020 driving a HI5700 mounted on its evaluation board. The HA5020 is a good choice for an op-amp to use with the family of CMOS converters.

The settling time for the above circuit, neglecting L, can be calculated from $T_S = 0.69 \times N \times R \times C$. N is the desired resolution. This equation applies only to CMOS converters with switched capacitor inputs. If the flash is the 8 bit HI5700, and R is equal to 27Ω, then the settling time would come out to 9ns, well within the sample time of the HI5700 running at a 20MHz encode rate.

An op-amp with adequate slew rate, full power bandwidth (FPBW), and drive current should be selected to drive an ADC. The minimum required slew rate can be calculated from: $SR_{MIN} = 2 \times \pi \times V_{PEAK} \times FPBW$. An HI1276 500

MSPS converter with a 2V reference would have a Vpeak equal to 1V and the required FPBW would equal 250MHz (nyquist). The minimum slew rate needed from the op-amp would then be 1571V/µs.

The minimum required output drive current is a function of the maximum slew rate, termination load impedance, and feedback current, if any. Given the required slew rate, the minimum output current needed from an amplifier just to charge the HI1276 input capacitance load of 20pF, is found by:

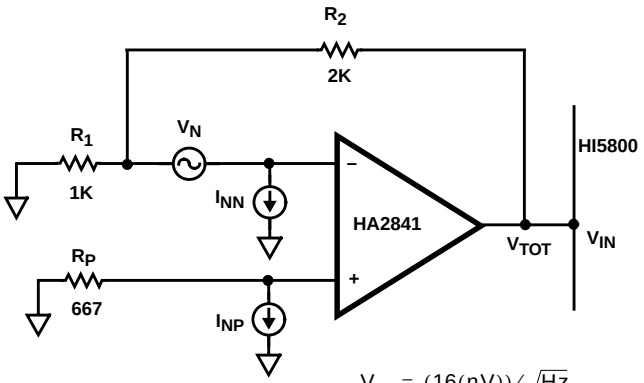
$$SR_{MIN} = \frac{OutputCurrent}{CapacitorLoad} = \frac{I}{C}$$

$$I_{MIN} = SR_{MIN} \times C = (1571 \times 10^{6}) \times (20 \times 10^{-12}) = 31mA$$

The HFA1100 is one of a family of high-speed op-amp and buffers that have sufficient slew rate and output current to drive the analog input of the Intersil family of ECL converters.

The overall system performance at a particular frequency will not be degraded if the harmonic distortion of input circuit to an ADC is less than that of the converter. Given that the dynamic range for a perfect 8 bit converter is 50dB, for a 0.5dB reduction in the overall system distortion, the amplifiers contribution must be less than 58dB. A 3dB reduction would result if the harmonic distortion of both the ADC and amplifier were equal. Sometimes it is difficult to get from the amplifier's data sheet a clear picture of what distortion to expect at the particular levels and frequencies the user will be operating. The gain flatness spec can also be used to give an indication of the op-amp linearity. For example, for 8 bit accuracy the op-amp should have a gain flatness of 0.2dB out to the frequency of interest.

An amplifier circuit driving an ADC must also minimize the total RMS noise voltage that it generates or it will reduce the system SNR. The objective is to keep this noise less than q/ ($\sqrt{12}$) (q is the LSB size), which is the theoretical RMS quantization noise of the ADC.



$V_N = (16(nV))/\sqrt{Hz}$

$I_{NN} = I_{NP} = (2pA)/\sqrt{Hz}$

$F_{BW} = 20MHz$

FIGURE 9. OP-AMP NOISE MODEL

Figure 9 is a HA-2841 op-amp driving an HI5800 with the voltage noise (V_N) and current noise (I_N) sources modeled. The equation for the total rms noise over the bandwidth of interest is:

$$V_{TOT} = \sqrt{1.57 \times F_{BW}} \times \sqrt{\left((V_N)^2 \times \left(1 + \frac{R_2}{R_1}\right)^2 + (R_2)^2 \times (I_{NN})^2 + (R_P)^2 \times (I_{NP})^2 \times \left(1 + \frac{R_2}{R_1}\right)^2\right)}$$

Where:

V_{TOT} is the total rms noise voltage at the input to the ADC.

R_1 is the feedforward resistor.

R_2 is the feedback resistor.

R_P is the noninverting input resistor.

V_N is input voltage noise spectral density.

I_{NN} is the inverting input current noise spectral density.

I_{NP} is the noninverting input current noise spectral density.

f_{BW} is the bandwidth over which the noise is to be integrated.

Note that I_{NN} and I_{NP} are equal in the case of voltage feedback op-amps but will not be for current feedback op-amps. If the small signal bandwidth is not given for the converter, then use its full power bandwidth for f_{BW}. For the values given in the figure, V_{TOT} is found to be equal to 180µV. This is about a factor of two less than the 352µV of quantization noise for a HI5800 12 bit ADC with a 5V range. Keep in mind that the amount of quantization noise is inherent to any ADC given its lsb size. Overall the HA2841 a good choice for driving the HI5800.

The circuits in CCD or muxed input applications must process large signal pulse type waveforms. In order to get the highest throughput possible, they must slew and settle quickly so, as depicted in Figure 10, the ADC can then accurately digitize the analog information.

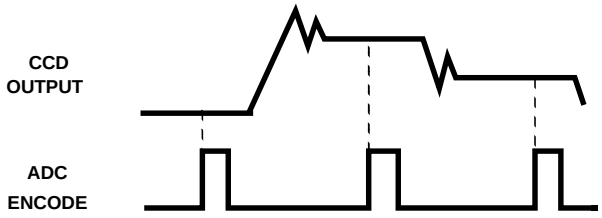


FIGURE 10. TIME DIVISION MULTIPLEXED SIGNAL

Op-amp settling time is made up of two parts. Initially the signal must slew until it enters a region where small signal analysis takes over. For a single pole frequency response, the error will then decay with a time constant determined by the small signal bandwidth of the op-amp. The settling time in an actual system is very much a function of the circuit parasitics and the overall frequency response of the circuit. As such, it is difficult to calculate an accurate number beforehand. Reference 2 has a more thorough discussion of settling time and the calculations involved. The extremely fast

settling time of the HFA family of op-amps (11ns to 0.1%) make these parts very useful in these types of applications.

Additional large signal time domain converter specifications such as overvoltage recovery time and transient response time become important in these applications. Transient response is a difficult test to perform especially to the 12 bit level. However, as in the case of the HI5800, if the converter is tested close to nyquist then its input will see full scale swings on alternate samples giving an indication of the overall settling time of the part.

This note has tried to give some of the important considerations when selecting an op-amp to drive a high-speed ADC. It is advisable to breadboard up an application circuit on an evaluation board provided by Intersil for a particular ADC and verify the performance with the converter.

Increased Accuracy

Adjustments can be made to the converter offset, gain, and linearity in applications where accuracy is of upmost importance. The triming of an HI5700 will be used here as an example. However, the techniques are the same for all the CMOS and ECL flashes as long as the relationship of the output codes to the input voltage is noted.

Offset correction is trimmed first and is usually done in the preamp driving the ADC (Figure 6 and Figure 7). Another method to produce the desired offset is to adjust the lowside the low side of the reference (V_{REF-} for the HI5700). Whatever method is used, a voltage 0.5 LSB up from the desired V_{REF-} is applied to the input and the offset is trimmed until the code 0 to 1 transition occurs.

Gain correction is trimmed next. It can also be done in the preamp circuit, but a better choice is in the reference circuit by adjusting the fullscale reference voltage to the ADC (V_{REF+} for the HI5700). The 2k pots in the reference circuit of Figure 4 can be used for this purpose. A voltage 1.5 LSB down from the desired V_{REF+} is applied to the input and the gain is trimmed until the code 254 to 255 transition occurs.

Linearity errors in a flash converter can many times result in a bowed transfer curve rather than a straight line through the endpoints. If taps on the reference ladder are provided, the user can make external adjustments to reduce this nonlinearity and improve the AC performance. Figure 11 illustrates a transfer curve with these kinds of errors before and after adjustment of a midpoint tap.

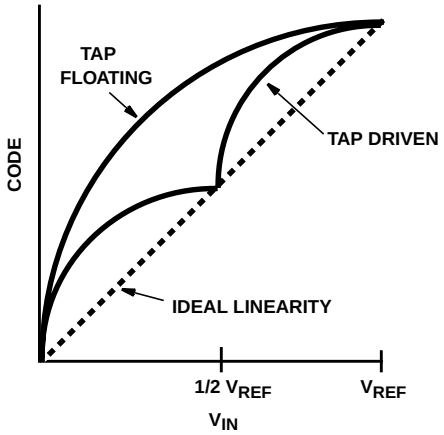


FIGURE 11. LINEARITY ADJUSTMENT

Figure 12 is a circuit that might be used to drive the midpoint tap of a flash. The op-amp will isolate the resistors R from the ladder impedance allowing improved performance over temperature. The values of these resistors are not critical as long as they match well and do not load down the reference source. If the resistors do not match to 0.5% then it might be necessary to replace them with a potentiometer and adjust the tap voltage to one-half the voltage between V_{REF+} and V_{REF-}. This adjustment should be made after the offset and gain errors have been trimmed. The capacitor value shown is that recommended for the HI5700. Consult the datasheet for the value suggested for a particular flash converter. If the flash has the 1/4 and 3/4 taps available, as in the case of the HI5700 and the CA3318, the resistor string can be modified to generate the required tap reference voltages and the appropriate buffers added to drive the taps.

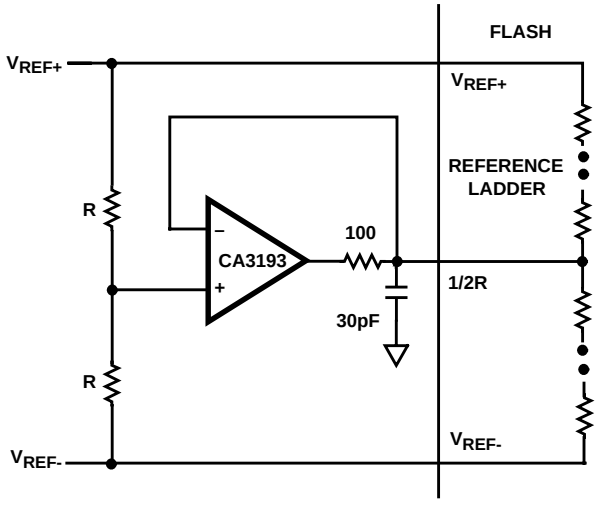


FIGURE 12. DRIVING THE REFERENCE TAP

Linearity adjustment can improve the performance of the HI5700 and CA3318. This technique is not useful for the ECL flash converters because they already have linearity correction on the chip and therefore have excellent INL numbers to begin with.

Another use for the ladder taps is to implement a nonlinear

transfer characteristic for the converter. A companding ADC will reduce the midscale voltage from its normal value to increase the SNR for low level signals.

Digital Inputs and Outputs

Table 1 shows that the Intersil family of high-speed converters has a wide range of logic families. Consult the datasheet to make sure the input and output logic levels and clock speeds are compatible with the accompanying logic. In order to minimize noise, use the slowest logic family that will still work.

There are a number of reasons for placing a data latch or buffer in close proximity to a converter. First, it could drive the large load capacitance normally seen on a digital buss, which can cause large digital power supply transient currents. For example, if all bits of an 8 bit TTL converter change simultaneously and the rise/fall time of the outputs are 5ns and the load capacitance is 15pF, the resulting transient current is 120mA. If the supply has a significant impedance, the resulting noise may not be adequately rejected by the PSRR of the ADC. In order to get the required isolation the supplies for the buffer must be separate from the supplies on the converter. A ferrite bead, in some cases, might be sufficient to provide the required isolation between the supplies.

The buffer or latch could also be used to isolate the ADC from a busy data buss. Depending on the design and layout of a converter a significant parasitic coupling may exist between the digital outputs and the analog circuitry. A buffer or latch would shield the converter from the buss noise and avoid the resulting reduction in SNR.

The rise and fall times of the digital logic for the ECL flash converters will approach 1ns. This will infer a corresponding interface bandwidth of 350MHz. In order to attain these speeds a 50Ω system is used and usually requires microstrip or stripline techniques in the board layout.

The HI1386 and HI1396 have single ended digital outputs. Place buffers close to the part to minimize line lengths and ringing. The HI1166 and HI1276 have differential digital outputs for the best noise rejection at the high data rates. Refer to references 4, 5, and 6 for additional information on high-speed board design.

It is possible to run the ECL family of high-speed flashes parts off a single +5V supply instead of the normal -5.2V supply. This will not effect the performance of the part but, as shown in Figure 13, the analog input levels and digital output levels will be changed. If an op-amp from the HFA family of parts is used to drive the input, then its supply voltages will have to be skewed to get the output swings required. The digital output levels can be translated to TTL levels by using a positive ECL logic family (PECL) provided by Motorola.

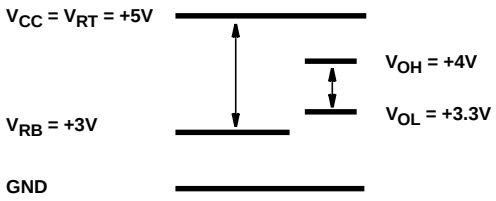


FIGURE 13. POSITIVE ECL LEVELS

Reference 7 and Reference 8 have more information on using this logic family.

When running the ECL parts at the normal -5.2V supply the ECL logic levels can be translated to TTL levels using parts provided by Motorola and Texas Instruments. TI provides a wide range of parts that includes buffers, transceivers, and latches. Reference 7 and Reference 9 have a complete listing of the parts available from these vendors.

Extraneous digital noise should be kept out of the convert clock source in order to minimize the timing jitter on this line and the resulting reduction of the signal to noise ratio (SNR) of the ADC. Given a 250MHz input frequency to an HI1276 and an rms jitter (t_A) of 2ps on the clock source, the SNR that can be expected only due to the effects of timing jitter can be found from:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times F_{IN} \times t_A}\right)$$

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times 250 \times 10^{6} \times 2 \times 10^{-12}}\right) = 50dB$$

It is not a trivial task to design a clock source with 2ps of jitter and in this case it might be beneficial to use a highly stable discrete bipolar sinewave crystal oscillator with heavy filtering to remove as much wideband and narrowband noise as possible. Figure 14 is a circuit that can be used to convert a sinewave from the clock source to the ECL levels required by the converter.

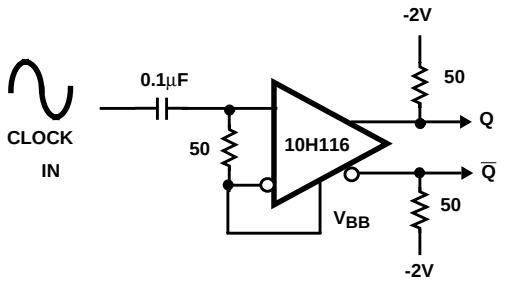


FIGURE 14. CLOCK CIRCUIT

In the interest of keeping out any digital noise, the convert clock source should be treated as an analog circuit and as such grouped with the other analog components. Be careful not to let this clock couple into the other analog circuitry.

Many times an application requires that a high sample rate ECL converter be interfaced to slower TTL DSP or buffer memories. Figure 15 is a circuit that can be used to demux

the ECL digital data out of a converter effectively cutting the output data rate in half. This reduction in data rate can be extended by adding additional latches and the appropriate timing signals.

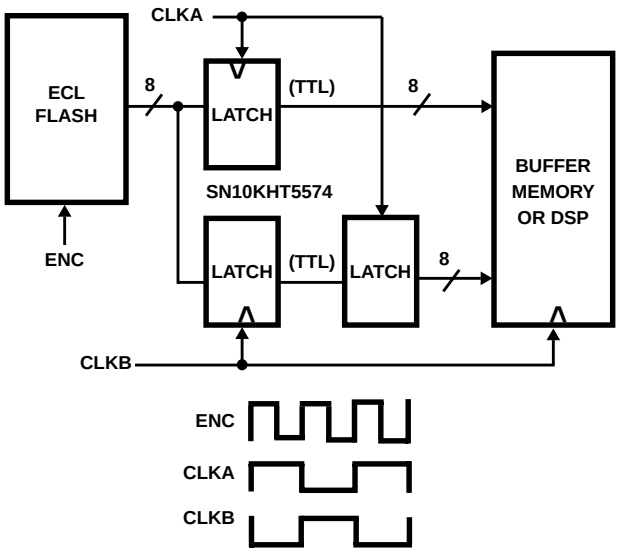


FIGURE 15. DATA DEMUX CIRCUIT

Antialiasing Filters

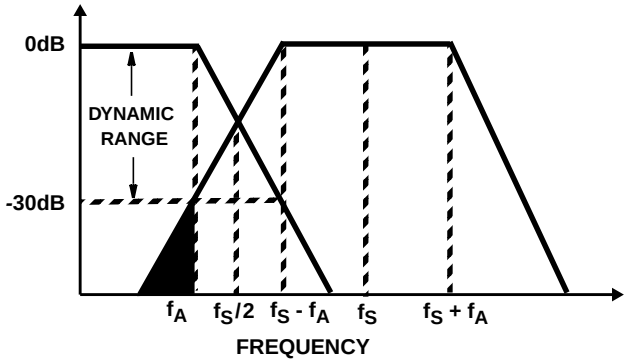


FIGURE 16. ALIASING EFFECTS

Figure 16 shows the effect of sampling a bandlimited signal at less than nyquist ($f_S/2$). The shaded area are signals at frequencies that were not in the original information but have been aliased into the baseband and will now limit the overall dynamic range of this system to 30dB. If this was intended to be a 12 bit system, then the dynamic range is significantly less then the desired 74dB. An antialiasing lowpass filter would be used to modify the rolloff from fa to $f_S/2$ so that the aliased signals would now be below 74dB in the baseband. Several considerations need to be taken into account when designing the filter. The designer must know the required passband flatness, the rolloff rate of the transition band, the final attenuation, and the phase characteristics. The lower the sampling rate, the steeper the rolloff has to be, the more poles required by the filter, and the greater the complexity of the filter design.

There are a number of types of lowpass antialiasing filters and each one has certain characteristics. A Butterworth filter has the flattest response near dc and has a moderately fast rolloff. This filter emphasizes constant amplitude versus constant phase shift therefore, the pulse response would have overshoot. A Chebyshev filter has a rapid attenuation above the cutoff frequency with some passband ripple. It has a squarer amplitude response than the Butterworth but less desirable phase and time delay. The Cauer (Elliptical) filter surpasses other filter designs for critical amplitude applications. It's very sharp rolloff rate with some ripple has the squarest possible amplitude response with poor phase and transient response. The Bessel filter has an optimized phase response over a wide input frequency. The passband response is not as flat as the Butterworth and it has a moderate attenuation rate. This filter is most useful for pulse applications since it avoids overshoot/undershoot. Reference 10 gives an excellent discussion of these and other considerations in choosing an antialiasing filter.

Passive filters are usually recommended for higher frequency filters (>200kHz). They will have impedances of around 50Ω to 100Ω. If the signal source can drive the filter, and the ADC has a high input impedance, then place these filters directly ahead of the converter so the output noise of any buffer circuit will also be band limited.

Active filters are useful below 200kHz. Keep in mind the considerations that have already been pointed out when selecting an op-amp to use with this type of filter.

HI5800 Step Input Applications

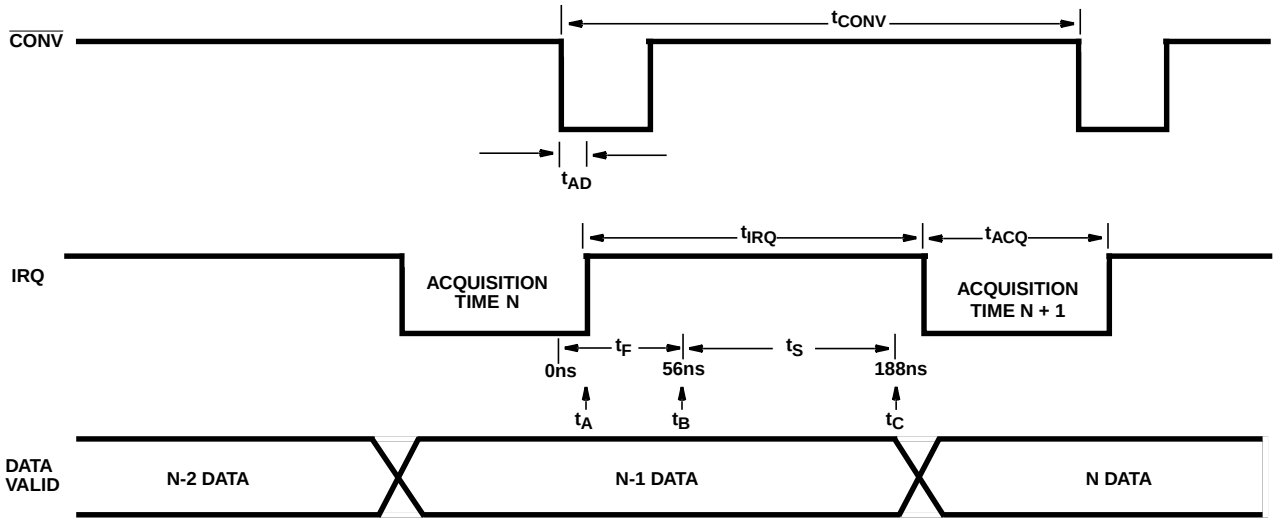
In order to get the best performance in muxed or CCD applications that use an HI5800, the step input to the converter should be timed correctly. As shown Figure 17, the overall digital system should be quiet during the time the HI5800 is doing its final pass to 12 bit accuracy (t_B to t_C). The preferred time to switch the input is between t_A and t_B because it allows about 200ns for the input to settle to 12 bits prior to the HI5800 sample-and-hold acquisition time. If the input is switched at t_C, then the overall conversion time of the HI5800 has to be extended to let the input to settle and still allow for the acquisition time of the sample-and-hold. Consult the HI5800 datasheet for the exact timing values.

It is difficult to find muxes that will settle to 0.01% accuracy in less than 200ns. The HI-508 is a 8 channel single ended mux that will settle to 0.01% in typically 600ns. The acquisition time of the HI5800 would have to be extended by 400ns to accommodate the mux settling time which would decrease the system throughput rate to 1.3MHz.

If the user wants higher throughput, they will have to settle for fewer channels. The HI-201HS is a four channel mux which will settle to 0.1% (10 bits) in typically 180ns. Another choice is the HA-2444. It is a selectable four channel operational amplifier with a settling time of 120ns to 0.1%. If very high switching speeds are required, then DMOS switches can be used. Siliconix provides a series of high-speed DMOS switches in the DG6XX series that will switch in about 25ns and can be driven by standard TTL logic. Since 12 bit settling times are highly dependent on the board layout and

$t_{AD} = t_A$ = APERTURE DELAY (~20ns)
t_{IRQ} = IRQ HIGH TIME (~200ns)
t_{ACQ} = SAMPLE AND HOLD ACQUISITION TIME (~130ns)

t_{CONV} = CONVERSION TIME (~333ns)
t_F = FIRST PASS (~56ns)
t_S = SECOND PASS (TO 12 BITS ~133ns)



numerous other factors, it is unlikely the user will be able to calculate an exact number for the throughput of a particular system from data sheet information.

Input Clamping

There are various reasons for clamping the input to a converter. In muxed input application the converter might be subject to frequent over range conditions as the mux switches from channel to channel. A clamp circuit that limits the input to small overranges would protect the converter and also significantly reduce the amount of time it would take the ADC to recover from the overrange. The analog input to the converter could also be severely overdriven if the supplies to an input buffer come up before the supplies to the ADC. The obvious solution to this problem is to power the input circuitry off the same supplies as the ADC. However, many flashes can operate at input levels that are above the maximum output voltage capability of an op-amp operated at the same rails that power the converter. Therefore, the input op-amp must operate off different supplies and the situation exists for power sequencing problems. The HI1175 is susceptible to this effect, and therefore it is recommended the input be diode clamped to V_{DD} and GND.

FIGURE 17. HI5800 TIMING

Figure 18 is a circuit that might be used to clamp the input to the voltages set on V+ and V-. These voltages could be the rails of the converter or the reference circuit in Figure 4 could be used to generate the required voltages. Resistor R should be calculated to limit the current to a safe level through the clamp diodes and the analog input of the flash. As discussed in the op-amp, section the value of this resistor should be kept as small as possible to maximize circuit performance. The diodes will add a voltage dependent capacitance at the input to the flash which will put an additional load on the op-amp drive requirements.

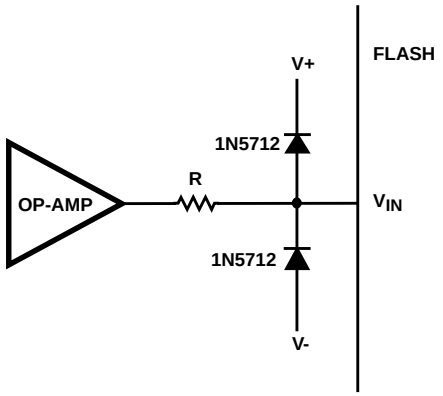


FIGURE 18. INPUT CLAMP CIRCUIT

The analog input to the HI5800 can be clamped to 2.5V It should **NOT** be clamped to the supply rails because these levels on the input will damage the part. The positive clamp voltage can be derived from the HI5800 +2.5V reference output but it should be buffered by an op-amp because the ADC

reference is not designed to sink large clamp currents. Another op-amp can be used to invert the +2.5V to generate the negative clamp voltage.

An elegant solution to the clamp problem for the ECL converters is to use an HFA1130 clamped amp. This op-amp has the electrical characteristics of the HFA1100 with the addition of two pins, V_H and V_L, which can be used to set the level at which the output is clamped. The clamp pins are a high impedance so they can be driven by simple resistive divider circuit or a DAC.

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