Introduction

Computers and telecom equipment are steadily becoming more complex, providing ever higher levels of performance. Simultaneously, the selling price for this equipment is being driven ever lower by market competition. Integral to all of this equipment is a power conversion system which converts the incoming unregulated power from the utility, or other source, to the multiple regulated voltages required by the equipment. In present designs the power subsystem constitutes a significant part of the equipment cost and volume.

The development of a unique power converter(s) for each new system is a substantial cost item in the equipment development. Frequently the equipment will have a variety of configurations with differing power requirements. To save development cost only a single design is often used to cover a range of loads. The result is that many users have to pay for capability not needed in their particular configuration.

One means to reduce power subsystem over capacity and cost is to use a distributed power system where the power processing functions are distributed within the system and more power processing capacity is added as required when more capability is installed. A typical distributed system will have a central power processor which converts the raw input power into a regulated DC bus. The central power processor is relatively simple but it does provide for line isolation and the safety requirements for the system. The central processor may be modular to allow for power scaling as the loads change. Each board or group of boards within the equipment has a small power processor which converts the DC bus to the voltages required by that particular section of the equipment. In general these board level converters are quite simple and efficient. Frequently no DC isolation is required at the board level which further simplifies the converters.

The use of multiple small power converters allows a custom system to be designed using high volume, low cost, standardized modules. In a complex system there can be substantial cost savings.

Board space is always at a premium and the localized power converters take up space. In general height is severely constrained and the power converter has a low profile geometry which tends to increase the board area required. In order to minimize the area required, the switching frequency (fs) of the converter is pushed as high as possible. The latest generation of systems [1] use converters with fs in the low MHz.

In addition to minimizing board area there are other requirements placed on these converters. [2] The components must be small enough for automated insertion and be low cost. All of this has to be achieved without seriously reducing conversion efficiency. Poor efficiency would increase the size and cost of the input converter and create thermal problems within the unit.

Overall these “simple” converters represent a significant design challenge.

Converter Circuits For MHz Switching

Many possible circuit topologies exist which could be used. They fall into three general categories: switchmode, resonant and quasi-resonant. At the power levels typical of board mounted converters (1 to 100W) single switch topologies are usually preferred for their lower cost. Examples of typical single switch, PWM converters are shown in Figure 1. A comparison of the switch, diode and capacitor voltages for these circuits is given in Table 1. In general circuits with the switch referenced to the ground node are preferred to simplify the switch drive circuits. The boost, Cuk and SEPIC circuits are non-isolated circuits with ground referenced switches. The flyback and forward converters provide isolation as well as multiple outputs with a single, ground referenced switch. The price paid for using an isolating transformer is higher cost and the increasing difficulty of designing a high performance transformer as the frequency is raised. The simpler non-isolated topologies are usually preferred in a distributed system unless there are compelling reasons to provide isolation.

TABLE 1. COMPONENT VOLTAGE STRESS FOR VARIOUS TOPOLOGIES

CIRCUIT	V_{SWITCH}	V_{DIODE}	$V_{COUPLING}$
Buck	V_I	V_I	N/A
Forward	$V_I/(1-D)$	$V_O/(1-D)$	N/A
Boost	V_O	V_O	N/A
Flyback	$V_I/(1-D)$	V_O/D	N/A
Buck-Boost	$V_I + V_O$	$V_I + V_O$	N/A
SEPIC	$V_I + V_O$	$V_I + V_O$	V_I
Cuk	$V_I + V_O$	$V_I + V_O$	$V_I + V_O$

NOTE: V_I = Input Voltage, V_O = Output Voltage, D = Duty Cycle

The boost, Cuk and SEPIC circuits each have different characteristics. The boost has a non-pulsating input current and a pulsating output current. It can only make voltages higher than the input bus. The Cuk converter has non-pulsating input and output currents and it can generate voltages either greater or less than the input voltage. The non-isolated Cuk converter inverts the sign of the input voltage. For the normal case of a positive DC bus, the Cuk converter will only produce negative voltages. The SEPIC converter is non-inverting and can generate voltages either above or below the input. The input current is non-pulsating but the output current is pulsating. Non-pulsating input and output currents are desirable to minimize EMI and reduce the need for additional filter elements.

The circuits in Figure 1 are considered “conventional” in that they have been widely used for many years. These topologies have first order input to output voltage transfer functions $M = V_O/V_I$, such as D, 1/(1-D) or D/(1-D). Recent work by Maksimovic [3, 4, 5] has shown that single switch quadratic and even higher order topologies exist. Three circuit examples are given in Figure 2. Quadratic circuits are particularly useful when large input to

output voltage ratios are needed or a large variation in input voltage is present.

When implemented with discrete components the high frequency performance of switchmode circuits is limited by the parasitic inductance and capacitance normally present. This is due to the very fast voltage and current transitions required for efficient power conversion. One way to get around these problems is to modify the circuit such that it exploits the parasitic elements as part of normal operation. A boost version of a zero voltage switching quasi-resonant converter (ZVS-QRC) is shown in Figure 3. This is a typical example of this class of circuit. Many others exist [6, 7, 8, 9] and most switchmode topologies can be implemented as ZVS-QRC. This circuit operates quasi-resonant; i.e. during a portion of the switching cycle the waveforms are sinusoidal like a resonant converter and during other portions of the switching cycle the waveforms are essentially straight line segments like a non-resonant switchmode converter.

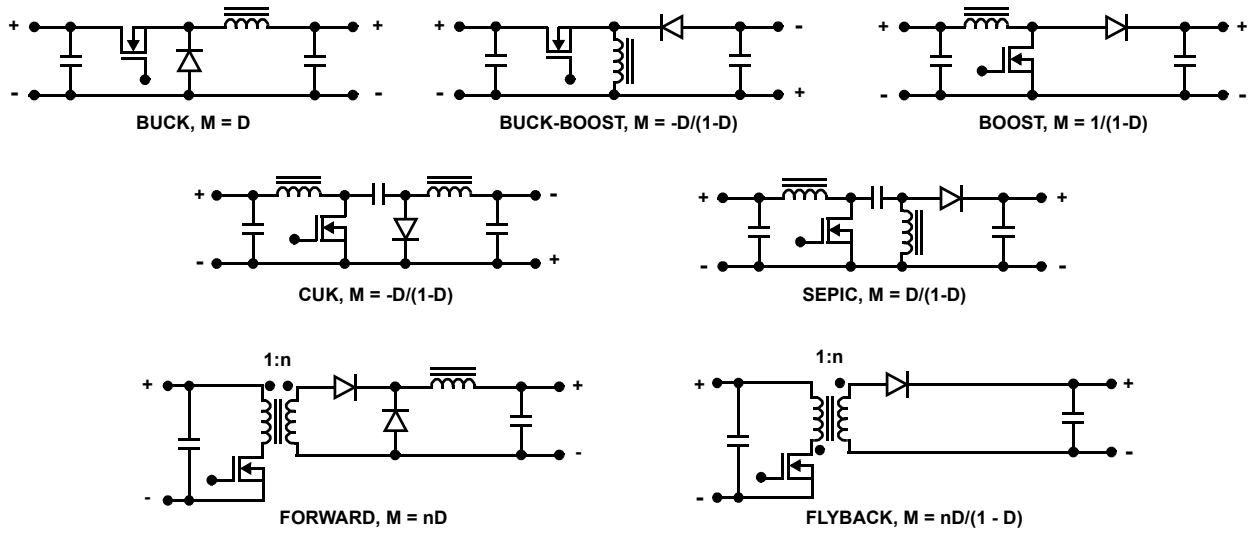


FIGURE 1. CONVERTER CIRCUITS, $M = V_O/V_I$

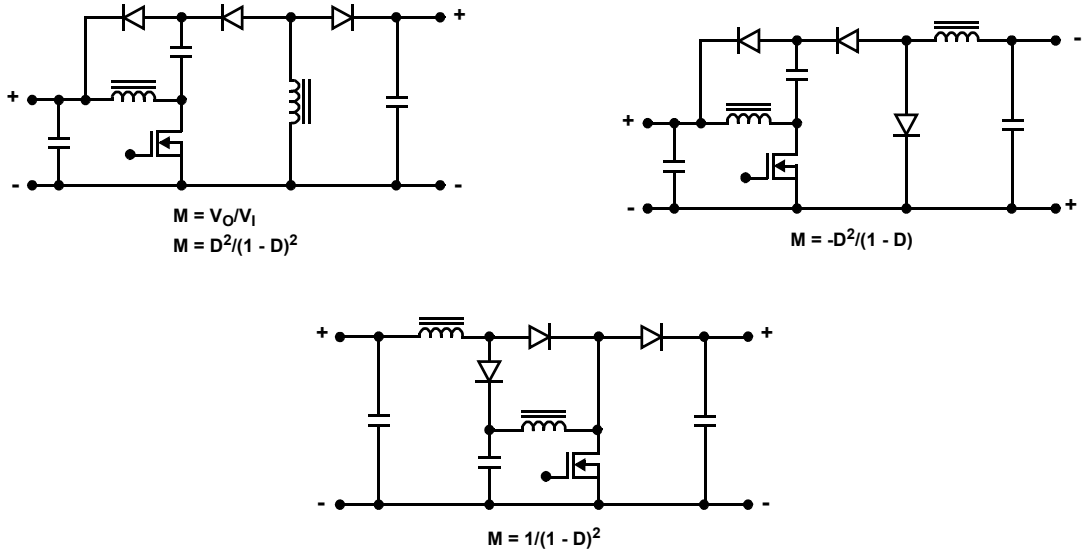


FIGURE 2. QUADRATIC CONVERTERS

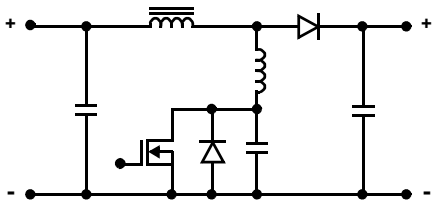
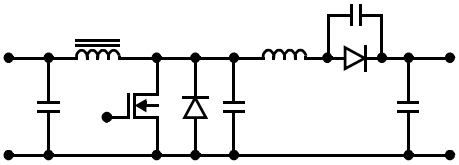


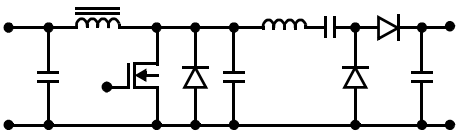
FIGURE 3. ZVS-QRC BOOST CONVERTER

The primary advantage of this topology is that the switch turns on and off while the voltage across the switch is zero. This translates to essentially zero switching loss and very low stress during switching transitions. The inherent junction capacitance of the switch is utilized as an active component as well as the series package inductance. This enables the switch to operate efficiently at very high frequencies (10MHz+). A price has to be paid for this performance. The converter can only be controlled by varying frequencies (fs). This is a relatively simple control scheme to implement but sometimes leads to EMI problems, particularly if the range of variation of fs is large. If fixed frequency operation is desired another switch must be added to the circuit. An additional disadvantage is that the switch voltage will be much higher than the input or output voltages. Peak switch voltages of 3 to 5 times the input voltage are typical. There are also restrictions on the acceptable load ranges and the switching frequency range can be large under some conditions.

Some improvement in performance can be obtained by operating the converter in a ZVS-multiresonant mode [10, 11]. Two examples are given in Figure 4. In this topology both the switch and the diode operate with low switching stress. This circuit does however, still have many of the disadvantages of the ZVS-QRC.



ZVS-MRC BOOST



CLASS E

FIGURE 4. MULTI-RESONANT CONVERTERS

Because of their disadvantages this family of converters is not usually employed until the operating frequency is so high that more conventional approaches cannot be used.

Many resonant converters can also be used for very high fs but in general they require more than a single switch and are not normally advantageous for low power levels (<100W).

Using Switchmode Circuits at MHz Frequencies

One of the primary motivations for developing resonant and quasi-resonant topologies has been to overcome the problems associated with switchmode converters when they are operated with high fs. While these approaches have been helpful, in general some price must be paid. This often takes the form of higher conduction losses, higher voltage stress, more numerous and larger components, loss of PWM control and limited load and input voltage ranges.

If the problems associated with high frequency operation can be overcome then switchmode circuits are advantageous. The limitations of switchmode converters for MHz operation stem primary from the difficulty of switching rapidly enough and the effect of parasitic components on the circuit behavior. An example of the parasitics present in a typical power stage is shown in Figure 5.

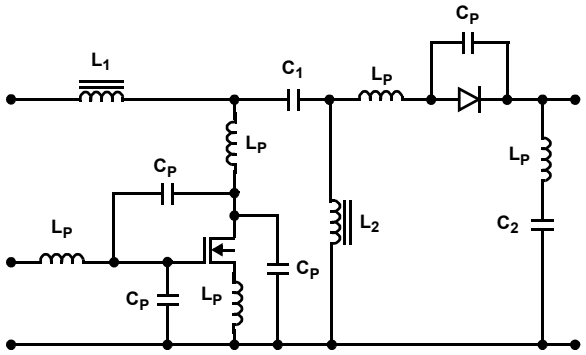


FIGURE 5. TYPICAL PARASITIC COMPONENTS

MOSFETs are inherently fast switching devices. If the input capacitance can be charged quickly enough they are capable of sub-nanosecond switching. However, in discrete or even hybrid circuits, the parasitic inductance in the gate and source connections limits the charge rate, increasing the switching transition time. The parasitic inductance and capacitance associated with the drain circuit causes voltage and current ringing which can over stress the switch and associated components, increase the switching loss and create VHF radiated and conducted EMI.

For power levels typically used in distributed power systems, a power IC manufactured with the Intersil PASIC [12] (Power Applications Specific Integrated Circuit) process is an excellent way to minimize the parasitic elements that limit circuit performance and increase the level of integration. Other advantages of the PASIC technology is that the IC design can provide on-chip temperature monitoring and high speed, on-chip, current sensing. Moreover, on chip gate drivers help reduce and confine gate drive current and parasitic capacitance associated with external power transistors. Because the switch and its drive circuitry can be integrated onto a very small area, nanosecond switching times are readily achieved. For volume production the IC has the advantage of much smaller size and lower cost than discrete equivalents.

Some external power components will still be needed, but they can be arranged to minimize parasitics. In the SEPIC converter shown in Figure 5, C_1 would be a chip ceramic capacitor and D_1 would be a surface mounted Schottky diode. Both of these components would be placed immediately adjacent to the IC. Efficient and economical 1MHz designs using this concept are presently in volume production.

It is possible to have floating or “high side” switches in the PASIC process for use with the buck topology shown in Figure 1. However, by using the SEPIC topology, the power DMOS transistor source may be returned to ground. This results in much simplified and efficient gate driving circuits. Moreover, a shorted or open power transistor is not detrimental to the load in the SEPIC topology. Because of the load coupling capacitor and the switch being returned to ground in the SEPIC topology, a shorted or open power transistor will not place the full high voltage input voltage on the load as in the buck topology. Besides the SEPIC topology, there is a host of topologies that may be implemented with a grounded source device, among them is the boost, forward, flyback, Cuk, and quadratic topologies.

The SEPIC Converter

The boost, Cuk, flyback and forward converters are well known to power supply designers and information on their design is widely available [13, 14 and 15]. The SEPIC topology has however, not been widely used. The following information is provided to familiarize designers with this circuit and its characteristics.

The name SEPIC is an acronym for Single-Ended Primary Inductance Converter. The circuit was first developed at AT&T Bell laboratories [16] in the mid 1970s. The intent of the developers was to create a new topology with properties not available in contemporary topologies. Of particular interest is the ability to buck or boost the input voltage without inverting voltage polarity.

A typical SEPIC circuit is shown in Figure 6A. This circuit has three dynamic energy storage elements, L_1, L_2 and C_1. The behavior of any switchmode circuit is strongly dependent on the continuity of the currents in the inductors and the voltages on the capacitors. A number of different operating modes are possible depending whether the inductor currents and capacitor voltages are continuous or discontinuous. As shown in Table 2, there are six possible inductor current operating modes. The -C entries are for conditions where one inductor current goes to zero before the other causing that inductor current to reverse direction. The inductor current is still continuous but the circuit behavior is different. The -D entries are for conditions where one inductor current goes negative and then a state exists where the two inductor currents are constant. The modes shown in Table 2 assume the voltage on C_1 is constant (small ripple). An additional set of modes is possible if the voltage on C_1 is discontinuous. While all modes are possible, the usual operating mode is to have the voltage on C_1 continuous and either both L_1 and L_2 in continuous conduction or both L_1 and L_2 in discontinuous conduction. These two modes will be the only ones for which the circuit behavior will be derived in this applications note and will be referred to as the CCM and DCM modes, respectively. There is a brief discussion of four other modes which may be encountered.

FIGURE 6. SEPIC CONVERTER

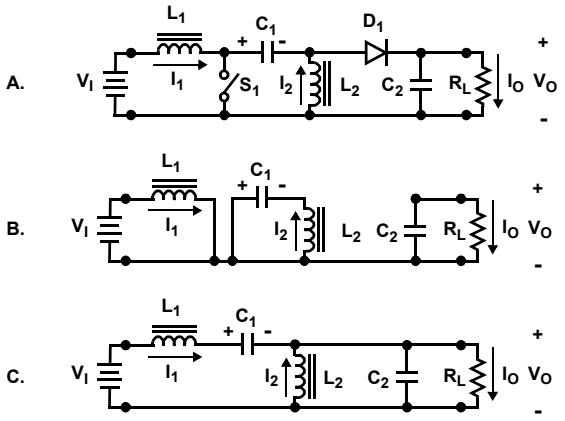


Table 2. SEPIC Operating Modes (C_1 and C_2 have small ripple)

INDUCTOR	CONDUCTION MODE					
L_1	D	C	C	-C	C	-D
L_2	D	C	-C	C	-D	C

CCM Circuit Operation

For this analysis it is assumed that both C_1 and C_2 are sufficiently large that the voltage ripple across them is small. By tracing the DC path from V_I through C_1, L_1, L_2 and back to V_I we see that $V_{C1} = V_I$. By inspection it can be seen that $V_{C2} = V_O$.

When S_1 is on, D_1 is off and when S_1 is off, D_1 is on. This means there are two circuit states during each switching cycle. The two states are shown in Figures 6B and 6C.

When S_1 is closed, L_1 is directly across V_I and I_1 is increasing. Energy is being stored in L_1. C_1 is connected across L_2 and I_2 is increasing. The energy in C_1 is being transferred to L_2. I_O is being maintained by C_2.

When S_1 is opened, the energy in L_1 is discharged into C_1 and C_2. The energy in L_2 is discharged into C_2. For CCM operation some energy remains in L_1 and L_2 (I_1 and $I_2 \neq 0$). At the end of the switching sequence S_1 is again closed and the cycle repeated.

To make the following discussion easier to follow, the details of the circuit analysis have been omitted. The equation derivations can be found in the appendix.

The ratio of the output voltage to the input voltage and the duty cycle are defined as:

$$M \equiv \frac{V_O}{V_I} \qquad \text{Equation 1}$$

$$D \equiv \frac{t_{ON}}{T} \qquad \text{Equation 2}$$

Where t_{ON} is the on time of S_1 and T = 1/fs, the switching period.

D as a function of M is:

$$D = \frac{M}{M+1} \qquad \text{Equation 3}$$

And M as a function of D is:

$$M = \frac{D}{1-D} \qquad \text{Equation 4}$$

A graph of Equation 4 is given in Figure 7 with comparisons to the buck, boost, Cuk and buck-boost converters. The large signal input-to-output voltage ratio for the SEPIC is identical to the Cuk and buck boost circuits except that there is no polarity inversion. V_O may be either less than or greater than V_I depending on D.

TABLE 3. SEPIC CCM VOLTAGES AND CURRENTS

M	V_O/V_I
D	$\frac{M}{M+1}$
M	$\frac{D}{1-D}$
$(I_1)_{RMS}$	MI_O
V_{L1}	V_O, $M \geq 1$ and V_O/M, $M \leq 1$
V_{S1}	$\left[\frac{M+1}{M}\right]V_O = V_O + V_I$
$(I_{S1})_{AVG}$	MI_O
$(I_{S1})_{RMS}$	$I_O\sqrt{M^2+M}$
V_{C1}	$V_O/M = V_I$
$(I_{C1})_{RMS}$	$I_O\sqrt{M}$
V_{L2}	V_O, $M \geq 1$ and $V_O/M = V_I$, $M \leq 1$
$(I_2)_{RMS}$	I_O
V_{D1}	$\left[\frac{M+1}{M}\right]V_O = V_O + V_I$
$(I_{D1})_{AVG}$	I_O
$(I_{D1})_{RMS}$	$I_O\sqrt{M+1}$
V_{C2}	V_O
$(I_{C2})_{RMS}$	$I_O\sqrt{M}$

Expressions for the voltages and currents in other circuit elements as a function of M, V_O and I_O are given in Table 3. Note that the expressions for the peak value for V_{L1} and V_{L2} depend on whether M > 1 or M < 1. The expressions in Table 3 assume that L_1 and L_2 are large with only small current ripple. For the case where the inductors are operating close the CCM-DCM boundary, the current waveforms will be triangular rather than rectangular and the RMS values will be approximately 15% higher.

The boundary between CCM and DCM modes will depend on several variables. For a given load resistance ($R_L=V_O/I_O$), fs and M, the values for the critical inductances of L_1 and L_2 are:

$$L_{1C} = \left[\frac{1}{2fs(M^2+M)}\right]R_L \qquad \text{Equation 5}$$

$$L_{2C} = \left[\frac{1}{2fs(M+1)}\right]R_L \qquad \text{Equation 6}$$

If the inductor values are higher than critical, then the converter will operate in CCM. If the values for the inductors are less than critical then the converter will operate in DCM.

The ratio of L_{2C} to L_{1C} is:

$$\frac{L_{2C}}{L_{1C}} = M \qquad \text{Equation 7}$$

A very important point here is that the currents in L_1 and L_2 go to zero simultaneously only if $L_2/L_1 = M$! If V_O is held constant and V_I is varied then the CCM-DCM transition will occur at some other point and will involve an intermediate mode.

In distributed power systems V_I is the DC bus and is normally relatively well regulated so the M varies only over a small range. In that type of an application, a smooth transition from both inductors in CCM to both in DCM will be possible. If L_2/L_1 does not equal M then the circuit behavior will be quite different.

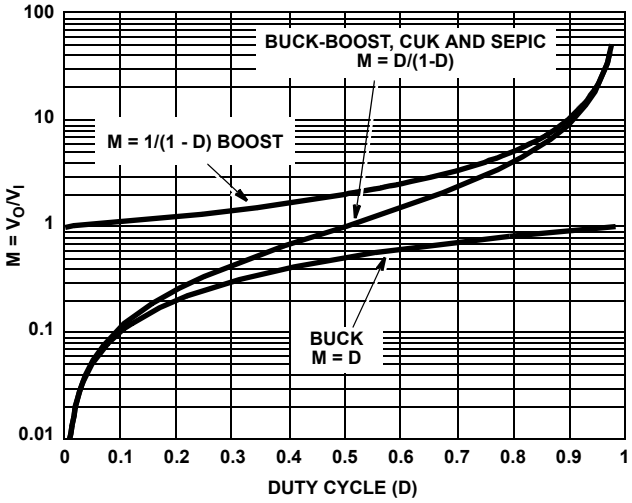


FIGURE 7. VOLTAGE TRANSFER AS FUNCTION OF DUTY CYCLE FOR VARIOUS TOPOLOGIES

If I_2 reaches zero before I_1, D_1 will still be conducting because of the current in L_1. This means there will be a voltage across L_2 which reverses I_2. This leads to two additional operating modes. Current waveforms for the case where $I_1(T) > -I_2(T)$ are shown in Figure 8. This mode corresponds to the C, -C state in Table 2. Figure 9 shows the waveforms for the case where $I_1 = -I_2$ at $t < T$. In this mode, when $I_1 = -I_2$, D_1 drops out of conduction and a new operating state is introduced as shown.

During this state (t_2 to T) the inductor currents are constant (ideally) because the voltage across C_1 cancels the input voltage. The conduction mode shown in Figure 8 is a continuous conduction mode but different from the continuous conduction mode where the current is unidirectional in both inductors. In the mode shown in Figure 9 the inductor currents are continuous but because of the period of time where di/dt = 0 (t_2 to T) the circuit will operate in a discontinuous mode. This mode corresponds to the C, -D mode in Table 2.

Both of these modes, C, -C and C, -D, have different characteristics from those mentioned in the previous discussion of continuous mode operation. The conditions where the current in L_1 reaches zero before the current in L_2 will be similar.

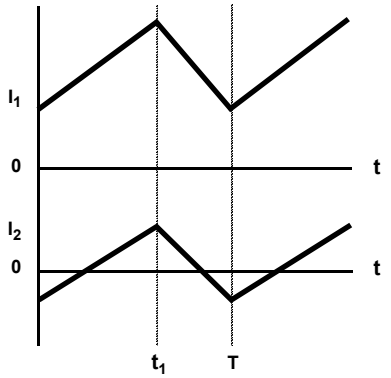


FIGURE 8. INDUCTOR CURRENTS FOR $I_1 > -I_2$ AT t = T

CCM Circuit Example

The following numerical example is provided to give a feeling for the component sizes and stresses in a typical application for the SEPIC converter.

Let:

$V_I = 35V$
$V_O = 12V$
$P_O = 50W$
fs = 1MHz

From this it can be seen that:

$I_O = 4.2A$
$R_L = 2.88\Omega$
M = 0.34

From Equations 5 and 6:

$L_{1C} = 3.2\mu H$
$L_{2C} = 1.1\mu H$

To operate well within CCM and minimize the RMS currents let:

$L_1 = 5\mu H$
$L_2 = 1.7\mu H$

These inductors could be a single layer, wound on small powdered iron or NiZn ferrite cores. From the equations in Table 3:

$V_{S1} = 47V$
$(I_{S1})_{RMS} = 2.8A$ RMS

A MOSFET with $BV_{DSS} = 60V$ would be appropriate for S_1.

$V_{D1} = 47V$
$(I_{D1})_{AVG} = 4.2A$

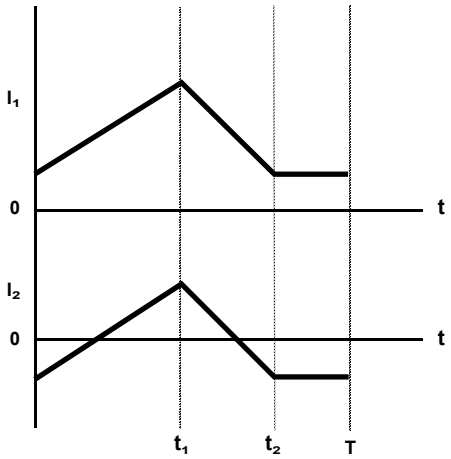
A 60V Schottky diode could be used for D_1.

$V_{C1} = 35V$
$(I_{C1})_{RMS} = 2.4A$ RMS

For C_1 a 50V, 0.47 to 1μF, multilayer, ceramic chip capacitor would be appropriate.

$V_{C2} = 12V$
$(I_{C2})_{RMS} = 2.4A$ RMS

For C_2 a 25V, 1μF, ceramic chip capacitor would be appropriate.



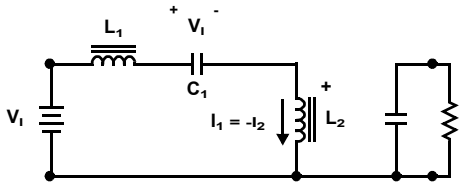


FIGURE 9. INDUCTOR CURRENTS AT $I_1 = I_2$ FOR t < T

DCM Circuit Operation

The following discussion assumes that $L_2/L_1 = M$ and that both inductors go into discontinuous conduction simultaneously. Operation in the DCM mode adds an additional circuit state as shown in Figure 10. At t = 0, the point at which S_1 is turned on, I_1 and $I_2 = 0$. The current in both inductors will rise until S_1 turns off (Figure 10A) and the energy in the inductors is discharged into the output (Figure 10B). When the inductor currents reach zero, D_1 stops conducting and the final state is assumed (Figure 10C). No current flows in the inductors because the voltage on C_1 cancels V_I.The expressions for D and M are:

$$D = \sqrt{2\tau_L\left[\frac{M^3}{M+1}\right]} \qquad \text{Equation 8}$$

Where:

$$\tau_L = \frac{fsL_1}{R_L} \qquad \text{Equation 9}$$

Equation 8 is only valid for D < 1. This sets an upper limit on τ_L of:

$$(\tau_L)_{MAX} = \frac{M+1}{2M^3} \qquad \text{Equation 10}$$

Values of τ_L greater than this limit mean that the converter is operating in CCM for the particular value of M.

Graphs of Equation 8 are given in Figures 11 and 12. These graphs illustrate the effect of varying load on the output voltage for M > 1 and M < 1.

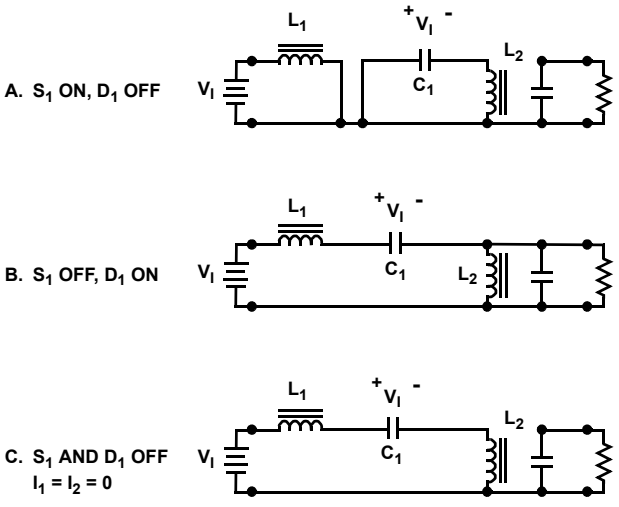


FIGURE 10. SEPIC DCM CIRCUIT STATES $L_2/L_1 = M$

Coupled Inductor Operation

Referring to Figure 6, when S_1 is closed, the voltage across both L_1 and L_2 is equal to V_I. Figure 6B shows that for the remainder of the switching cycle the voltage across L_1 and L_2 is equal to V_O. Because these two voltages are equal and in phase, L_1 and L_2 may be integrated into a single magnetic structure with only one magnetic path, this is referred to as a coupled inductor. A coupled inductor version of the SEPIC topology [14] is shown in Figure 13. This topology has several advantages. The leakage inductance of the coupled inductor can be arranged to effect zero current ripple on the input with finite value of L. Because the turns ratio between the windings is 1:1, there cannot be two different values for L_1 and L_2. This does not lead to multiple modes however. Because they are wound on a common core, both windings are either conducting or not depending on whether there is energy in the core or not. The circuit operates either CCM or DCM.

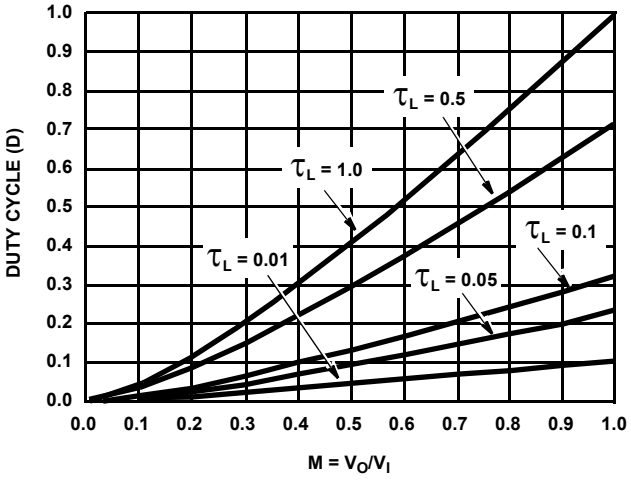


FIGURE 11. SEPIC CONVERTER IN THE DCM MODE FOR A FAMILY OF LOAD PARAMETERS, τ, WITH THE VOLTAGE TRANSFER RATIO, M < 1

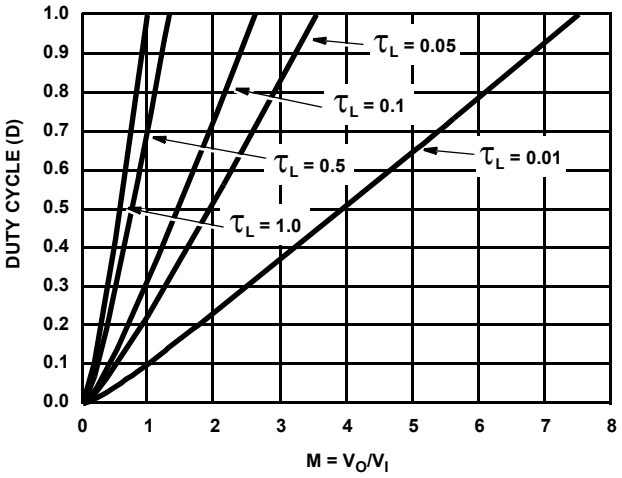


FIGURE 12. SEPIC CONVERTER IN THE DCM MODE FOR A FAMILY OF LOAD PARAMETERS, τ, WITH THE VOLTAGE TRANSFER RATIO, M < 8

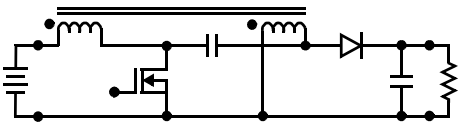


FIGURE 13. COUPLED INDUCTOR SEPIC

References

[1] Wittlinger, H.A.; Hodgins, Robert G.; Cassani, John C.; Hurd, Jonathan J. and Thomas, David R. *Sophisticated Control IC Enhances 1MHz Current Controlled Regulator Performance*, High Frequency Power Conversion (HFPC) conference proceedings, May 1992, pp. 167-173

[2] Smith, Craig D. and Cassani, *Distributed Power Systems Via ASICs Using SMT*, Surface Mount Technology, October 1990

[3] Maksimovic, D., *Synthesis of PWM and Quasi-Resonant DC-to-DC Power Converters*, California Institute of Technology Ph.D. thesis, Division of Engineering and Applied Science, January 1989

[4] Maksimovic and Cuk, *Switching Converters With Wide DC Conversion Range*, High Frequency Power Conversion (HFPC) conference record, May 1989

[5] Maksimovic and Cuk, *General Properties and Synthesis of PWM DC-to-DC Converters*, IEEE Power Electronics Specialists Conference (PESC) record, June 1989

[6] Liu, Oraganti and Lee, *Resonant Switches - Topologies and Characteristics*, IEEE PESC record, 1985, pp. 106-116

[7] Zheng, Chen and Lee, *Variations Of Quasi-Resonant DC-DC Converter Topologies*, IEEE PESC record, 1986, pp. 381-392

[8] Ngo, K., *Generalization of Resonant Switch and Quasi-Resonant DC-DC Converters*, IEEE PESC record, 1987, pp. 395-403

[9] Maksimovic and Cuk, *Constant-Frequency Control of Quasi-Resonant Converters*, HFPC record, May 1989

[10] Tabisz, and Lee, *Zero-Voltage-Switching Multiresonant Techniques - A Novel Approach to Improve Performance of High-Frequency Quasi-Resonant Converters*, IEEE PESC record, 1988, pp. 917

[11] Sokal and Sokal, *Class E - A New Class of High Efficiency Tuned Single-Ended Switching Power Amplifiers*, IEEE Journal of Solid-State Circuits, June 1975, pp. 168-176

[12] Mansmann, Jeff; Shafer, Peter and Wildi, Eric, *Maximizing the Impact of Power IC's Via a Time-to-Market CAD Driven Power ASIC Strategy*, Applied Power and Electronics Conference and Exposition (APEC) proceedings, February 1992, pp. 23-27

[13] Severns and Bloom, *Modern DC-to-DC Switchmode Power Converter Circuits*, Van Nostrand Reinhold, 1985

[14] Sum, K., *Switch Mode Power Conversion - Basic Theory and Design*, Marcel Dekker, In., 1984

[15] Pressman, A., *Switching and Linear Power Supply, Power Converter Design*, Hayden Book Co., 1977

[16] Massey, R.P. and Snyder, *E.C., High Voltage Single-Ended DC-DC Converter*, IEEE Power Electronics Specialists Conference (PESC) record, 1977, pp. 156-159

[17] Clarke, P., *A New Switched-Mode Power Conversion Topology Provides Inherently Stable Response*, POWERCON 10 proceedings, March 1983, pp. E2-1 through E2-7

Appendix

SEPIC Equation Derivations for CCM and DCM Operation CCM Operation

The following calculations are referenced to Figure 6.

For C_1 and C_2 large: $V_{C1} = V_I$ and $V_{C2} = V_O$

When S_1 is closed: $V_{L1} = V_{L2} = V_I$

When S_1 is open: $V_{L1} = V_{L2} = -V_O$

By conservation of flux in the inductors:

$$V_I t_{ON} = V_O (T - t_{ON}) \quad \text{(A1)}$$

For $D = t_{ON}/T$ and $M = V_O/V_I$ Equation A1 reduces to:

$$M = D/(1 - D) \quad \text{(A2)}$$

Equation A2 can be inverted:

$$D = M/(M + 1) \quad \text{(A3)}$$

Assuming that L_1 and L_2 are sufficiently large that the current ripple is small and substituting A3

$$I_O = (I_1 + I_2)(1 - D) = (I_1 + I_2)(1/(M + 1)) \quad \text{(A4)}$$

For Power In = Power Out: (A5)

$$V_I I_1 = V_O I_O,\ M = V_O/V_I = I_1/I_O$$

Combining Equations A4 and A5:

$$I_2 = I_O \quad \text{(A6)}$$

S_1 Voltage and Current

For S_1 open:

$$V_{S1} = V_{C1} + V_O = V_I + V_O \quad \text{(A7)}$$

Restating in terms of M and V_O:

$$V_{S1} = (1 + 1/M)V_O \quad \text{(A8)}$$

For S_1 closed:

$$(I_{S1})_{RMS} = (I_1 + I_2)\sqrt{D} \quad \text{(A9)}$$

Which reduces to:

$$(I_{S1})_{RMS} = I_O\sqrt{(M + M^2)} \quad \text{(A10)}$$

D1 Voltage and Current

By inspection:

$$(I_{D1})_{AVG} = I_O \quad \text{(A11)}$$

When S_1 is closed:

$$V_{D1} = V_I + V_O = (1 + 1/M)V_O \quad \text{(A12)}$$

Note the switch and diode have the same peak voltage.

Inductor Currents

$(I_1)_{RMS} = I_1 = MI_O$ (A13)

$(I_2)_{RMS} = I_O$ (A14)

This assumes small current ripple. If smaller inductors are used such that the inductor currents are nearly triangular (near the DCM-CCM boundary) the RMS current values will be approximately 15% higher.

Capacitor Currents

$$(I_{C1})_{RMS} = \sqrt{I_1^2(1-D) + I_2^2} \quad \text{(A15)}$$

Which reduces to: $(I_{C1})_{RMS} = I_O\sqrt{M}$ (A16)

$$(I_{C2})_{RMS} = \sqrt{I_O^2 D + (I_1 + I_2 - I_O)^2} \quad \text{(A17)}$$

Which reduces to: $(I_{C2})_{RMS} = I_O\sqrt{M}$ (A18)

Values for the Critical Inductances of L_1 and L_2

For a given current, the critical inductance is the value for the inductor that allows the current to just reach zero at the end of the switching cycle. This is a special case of CCM.

L_1 Critical

The input current will be triangular. I_{1P} = peak value of the current:

$I_{1P} = 2I_{1AVG} = 2MI_O$ (A19)

$I_{1P} = V_I t_{ON}/L1$ (A20)

$t_{ON} = DT$ (A21)

$fs = 1/T$ (A22)

Combining Equations A19 - A22:

$L_{1C} = [1/2fsM(M + 1)]R_L$ (A23)

A similar calculation for L_2 yields:

$L_{2C} = R_L/(2fs(M + 1))$ (A24)

DCM Analysis

For this analysis it will be assumed that:

$L_{2C}/L_{1C} = M$ (A25)

This means I_1 and I_2 go to zero simultaneously. The circuit states shown in Figure 10 will be used for this analysis.

$t_1 = t_{ON}$ = on time of S_1

t_2 = the current fall time in the inductors

From conservation of flux in L_1 and L_2:

$V_I t_1 = V_O t_2$ (A26)

From conservation of charge in C_1 (A27)

$I_{1AVG} t_2 = I_{2AVG} t_1$

From conservation of power: (A28)

$V_I I_{1AVG} = V_O I_O$

Derivation of Expressions for M and D

$I_{1P} = V_I t_1/L_1$ (A29)

$$I_{1AVG} = I_{1P}\left[\frac{t_1 + t_2}{2T}\right] \quad \text{(A30)}$$

$$D = \sqrt{\left[\frac{2fsL_1}{R_L}\right]\left[\frac{M^3}{M+1}\right]}$$

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(Rev.4.0-1 November 2017)

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