RS-485 Transceivers

RS-485 Transceivers in J1708 Physical Layer Applications of Heavy Duty Vehicles

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Abstract

In 1986 the Society of Automotive Engineers (SAE) issued the recommended practice J1708, which defines a bidirectional, multi-master network that enables the communication between Electronic Control Units (ECUs) in heavy duty vehicles. The standard specifies a data rate of 9.6kbps and was intended to be replaced by the much faster (250kbps) Controller Area Network (CAN) a decade later.

Still, J1708 remains alive and well, not only in refurbished networks of older vehicles, but also as a diagnostic bus in modern heavy duty vehicles. Here it coexists with CAN, which is predominantly used for the exchange of high-speed data (Figure 1).

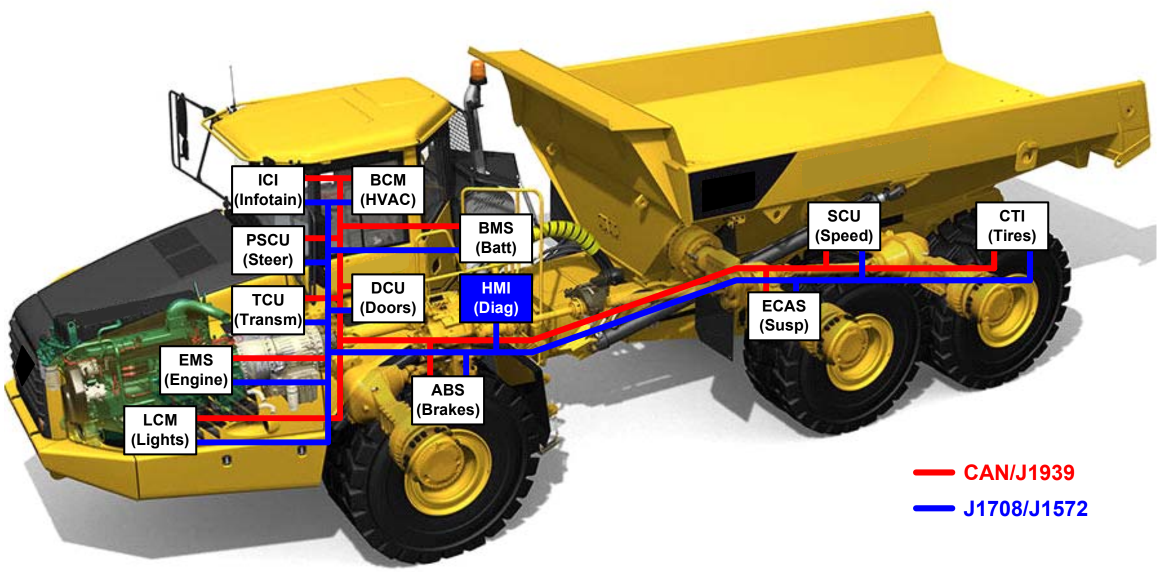

Figure 1. Electronic Control Unit Network in Heavy Duty Vehicles

This application note gives an overview of the hardware design aspects of a J1708 network. It explains the configuration and operating mode of RS-485 transceivers in J1708 applications, and introduces a highly robust bus node design that is immune to overvoltages of ±60V_{DC} and ±80V transients, while operating over a wide common-mode voltage range of ±20V.

Contents

1. Network Parameters

SAE J1708 defines a serial communication link for the exchange of data between standalone microcomputer-based modules, known as Electronic Control Units (ECUs), in heavy duty vehicle applications.

The topology of a J1708 network is that of a common or global bus, supporting a minimum of 20 bus nodes. The transmission medium is an 18-gauge twisted-pair cable. Although there is no restriction in cable length between nodes, the total length of the data link (A+B+C+D+E+F) shall not exceed 40m. The applied data rate is 9.6kbps, which translates into a bit time of (t_B = 104.17µs).

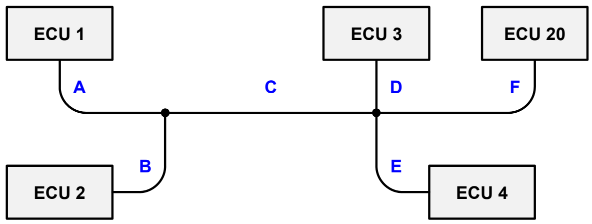

Figure 2. J1708 Network Topology

2. Bus Node Interface Circuit

Each bus node interface consists of an RS-485 transceiver and a resistor-capacitor network, known as the load (Figure 3). Thus, J1708 networks do not have bus termination resistors as referenced in EIA-485.

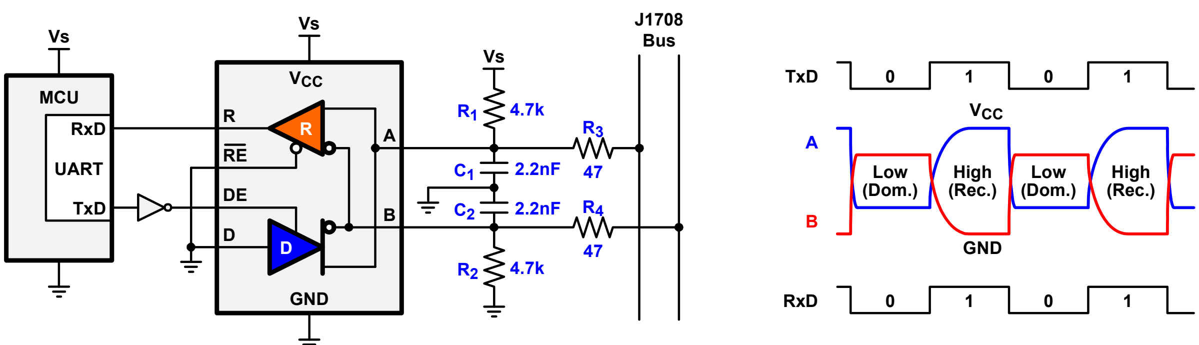

Figure 3. Bus Node Interface Circuit

The receiver stage within the RS-485 transceiver is always enabled through the fixed connection of the receiver enable pin ($\overline{RE}$) to local ground. This allows for monitoring the data traffic on the bus, as well as the detection of bus collisions.

The driver is configured to operate in the dominant/recessive mode. Its data input (D) is fixed to ground while its enable pin (DE) is used as the new data input. A high at DE enables the driver, driving the low potential at D onto the bus. A low at DE disabled the driver, making its outputs high-impedance. In this case, bus line A is pulled up towards Vs through R_1, and bus line B is pulled down to ground using R_2. This condition constitutes a bus-high. To ensure the UART output and the differential output of the driver have the same signal polarity, a logic inverter is inserted between TxD and DE.

Because the actively driven low-state always overwrites a passively generated high-state on the bus, the low becomes the dominant, and the high becomes the recessive bus state. This operating mode enables bus nodes to detect idle lines and bus contentions, both of which are important conditions, used for synchronizing the network, prioritizing bus access, and aborting transmissions.

The remaining components of the load circuits serve as low-pass filters. R_3 and R_4 in combination with C_1 and C_2 form a 1.6MHz receive low-pass filter for EMI suppression. The driver output impedance together with C_1 and C_2 form a 6MHz transmit low-pass filter for EMI and transient suppression.

3. Data Formats

A J1708 message consists of three types of characters:

(1) **Message Identification character (MID):** Used to identify the transmitter sending the information, and to establish message priority and collision detection.

(2) **Data characters:** Used to convey the intelligence of a message to the receiver, such as data type, size, and scaling factor.

(3) **Checksum:** Required to prevent invalid data from being used.

The message length can range from a minimum of 2 up to a maximum of 21 characters, including the checksum (Figure 4).

Each character consists of 10 bits: one start bit (logic low level), eight data bits, and 1 stop bit (logic high-level). This conversion is consistent with the standard UART transmission scheme, 8-N-1 (8 data bits, no parity, 1 stop bit), with the data bits being transmitted Least Significant Bit (LSB) first.

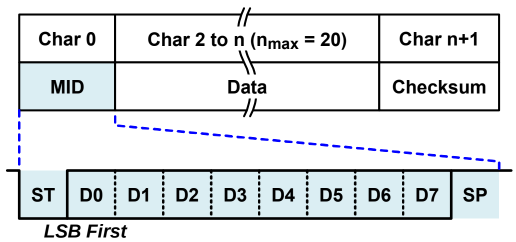

Figure 4. J1708 Message and Character Formats

4. Message Priority and Bus Access Time

Each message is assigned a priority between one and eight by the module manufacturer's defining application document. Classes of message priorities and their assignments as specified in J1708 are listed in Table 1.

Table 1. Priority Classes

Priority	Message Assignment
1 2	Messages requiring immediate bus access
3 4	Messages preventing mechanical damage
5 6	Messages controlling economy and efficiency
7 8	All other messages

Before a transceiver attempts to access the bus, it must have detected an idle-line condition, which consists of 10 consecutive high bits. After that, the transceiver must continue to wait until its priority delay (P_D) has passed. This delay is transceiver specific as it depends on the message priority. P_D is calculated using Equation 1:

(EQ. 1) $$P_D = P \cdot 2 \cdot t_B$$

where P is the message priority and t_B the bit time of 104.17µs.

The sum of idle-line duration (t_I) and priority delay is known as the bus access time (t_A).

(EQ. 2) $$t_A = t_I + P_D$$

Thus, the bus access time is the time a transceiver must wait, after being synchronized or returning from a collision detection, before trying to access the bus again. Table 2 lists the resulting priority delays and bus access times in numbers of bits (multiples of t_B). As can be seen, messages of higher priorities have shorter bus access times than low-priority messages.

Table 2. Priority Delays and Access Times

Priority	P_D (Bits)	t_A (Bits)
1	2	12
2	4	14
3	6	16
4	8	18
5	10	20
6	12	22
7	14	24
8	16	26

5. Collision Detection and Bus Access

If two or more nodes gain bus access at the same time, data collision is inevitable. Figure 5 presents a collision example between a transmission and a diagnostics ECU.

ECU	MID	D0	D1	D2	D3	D4	D5	D6	D7	P	P_D (Bits)
Transmission	24	0	0	0	1	1	0	0	0	2	4
Diagnostics	48	0	0	0	0	1	1	0	0	3	6

↑ 1st (D3) ↑ 2nd (D5)
Collision

Figure 5. Collision Detection between Electronic Control Units

Both ECUs drive their MIDs onto the bus, which are instantaneously verified through the corresponding receivers. At the fourth MID bit (D3) the transmission ECU detects a collision as it transmits a 1 onto the bus, but reads back a 0 instead, which occurred due to the diagnostics ECU pulling the bus low. Both ECUs continue transmitting, the diagnostics ECU because it did not detect a collision, and the transmission ECU because it entered the collision-retry procedure.

Then, at bit D5 a second collision occurs. This time the diagnostics ECU detects the collision and enters the collision-retry procedure. Because of the detected collisions, both ECUs relinquish the bus after sending the first character (MID), only to reengage into a new, subsequent bus access attempt (Figure 6 on page 5).

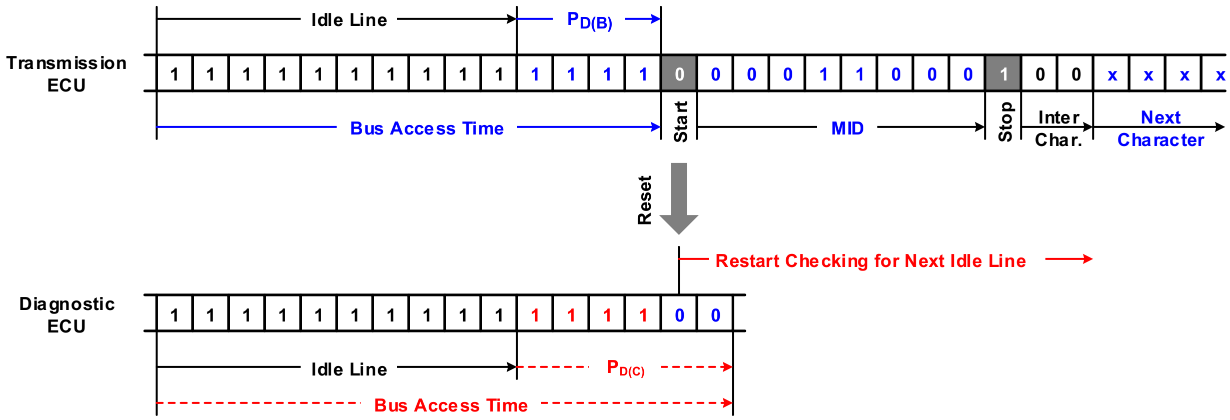

Figure 6. Simultaneous Bus Access Attempts of ECUs

Both ECUs begin checking the bus for an idle-line condition. Because the transmission ECU has the higher priority (see Figure 5 on page 4), its priority delay is only 4 bit times and thus, shorter than the 6 bit PD of the diagnostics ECU.

After passing a total bus access time of 14 bits (t_I + P_D), the transmission ECU begins transmitting its entire message. At the same time, the diagnostics ECU, still waiting for two more high bits to receive, is reset by the low-level start bit from the transmission ECU. The diagnostics ECU must now restart checking for the next idle-line condition before trying to regain bus access. The next idle-line however, can only occur after the transmission ECU has completed sending its entire message (for example, 2 to 21 characters).

6. Fault-Protected Bus Node Solution

Today's modern microcontrollers, such as the Renesas RL78 family of MCUs, provide the programmable inversion of an embedded UART output in form of a /TxD signal (Figure 7). This eliminates the need for an external inverter gate or a modified RS-485 transceiver with inverted DE input, and ensures that designers can chose from a wide variety of standard RS-485 transceivers.

The transceiver of choice for J1708 applications is the ISL32455E. This is due to many customers requiring high immunity to overvoltages (DC and transients), as well as reliable data transmission over a significantly wider Common-Mode Voltage Range (CMVR) than specified in EIA-485.

The ISL32455E has bus I/O stages with high, symmetric stand-off capability of up to ±60V, thus providing protection against high DC potentials and transient voltages within that range (Figure 8 on page 6).

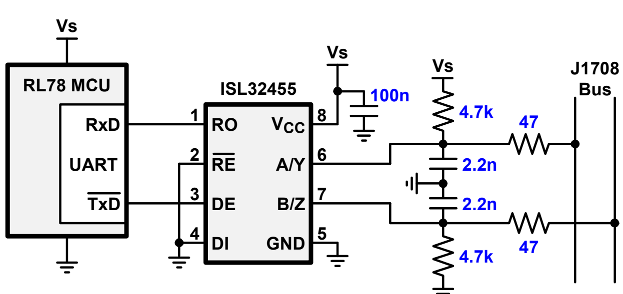

Figure 7. Robust J1708 Interface with ISL32455

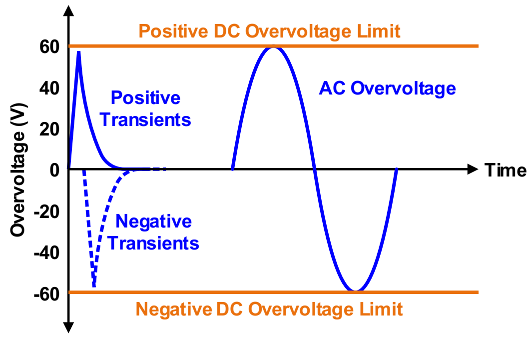

Figure 8. Stand-off Voltage Range of ISL32455E

The transceiver also supports a wide CMVR of up to ±20V. To limit the power consumption of the active driver during a fault event, while maintaining reliable operation across the wide CMVR, its internal current limiter has a dual fold-back characteristic (Figure 9).

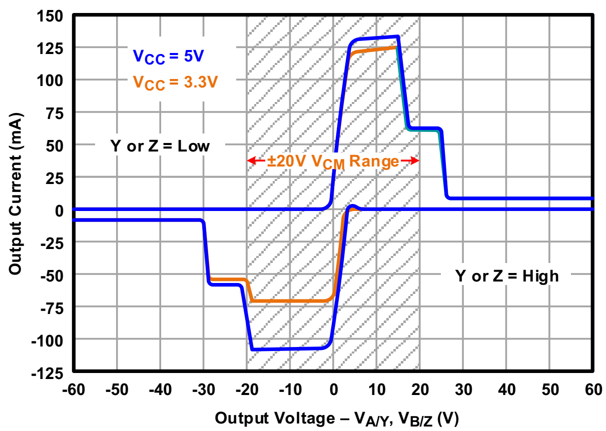

Figure 9. Dual Fold-Back Characteristic of the Current Limiter

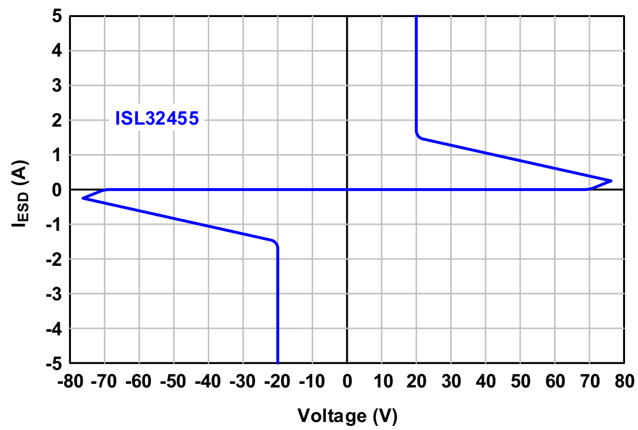

Figure 10. V-I Characteristic of the On-Chip ESD Protection

Here the first fold-back current level ensures that the driver never folds back when driving loads within the entire 40V common-mode voltages. The very low second fold-back current setting minimizes power dissipation if the driver is enabled when a fault occurs.

In the event of a major short-circuit condition, the ISL32455E also provides a thermal shutdown function that disables the driver whenever the die temperature becomes excessive. This eliminates any power dissipation and allows the die to cool. The driver automatically re-enables after the die temperature drops by 15°C. If the fault condition persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. The receiver stays operational during thermal shutdown, and fault-protection is active, whether the driver is enabled or disabled, and even if the IC is powered down.

The ISL32455E provides high ESD protection of up to ±16kV. To prevent the transceiver's on-chip ESD protection circuits from being triggered by low-level (60V) overvoltages, the ESD trigger threshold lies far outside the ±60V operating range (Figure 10). The symmetric protection range of the ISL32455E presents another major benefit for surge protection designs, as it allows designers to choose from a vast range of symmetrically clamping Transient Voltage Suppressors (TVS).

Further device features of the ISL32455E are:

- A wide supply voltage range from 3.0V to 5.5V, allowing an easy interfacing to low-voltage controllers.
- Low supply current of only 2.1mA, which is 1/20th of the supply current of some legacy transceivers previously used in J1708 applications.
- ¼ UL rating, to ensure the maximum common-mode loading of 20UL for a fully loaded J1708 network supporting 20 nodes is never exceeded.
- Full-failsafe receiver inputs to maintain the receiver output high if the inputs are open or shorted, thus easing the detection of bus failures.

Table 3 lists the key parameters of the ISL32455E compared to competitive devices used in legacy J1708 designs.

Table 3. ISL32455E Key Parameters

Parameters	ISL32455E	ISL81487	DS36277
Fault Protection: DC (Transients referenced in EIA-485)	±60V (±80V)	-8V to +13V	-8V to +13V
Common-Mode Voltage Range	±20V	-7V to +12V	-7V to +12V
Supply Voltage Range	3.0V to 5.5V	4.5V to 5.5V	4.75V to 5.25V
Supply Current (Driver disabled, no Load)	2.1mA	0.35mA	24mA
Unit Load	0.25	0.125	1.5
Failsafe	Open/Short	Open/Short	Open/Short
Driver Enable to Output Low Delay (t_{ZL})	300ns	70ns	60ns
Receiver Input-to-Output Delay (t_{PHL})	200ns	150ns	90ns
ESD Protection (HBM)	±16.5kV	±7kV	±7kV
Operating Temperature Range	-40 to +85°C	-40 to +85°C	-40 to +85°C

The two delay times, t_{ZL} and t_{PHL}, are of utmost importance because they ensure J1708 compliance during the fast HIGH to LOW (recessive-to-dominant) transition on the bus. Here, J1708 specifies a transition time of 600ns for a bus with two nodes and 2.3µs for a fully loaded bus with 20 nodes.

Table 3 lists the maximum values for t_{ZL} and t_{PHL} with 300ns and 200ns respectively, thus assuring a maximum HIGH to LOW or Recessive-to-Dominant transition time (t_{RD}) of 500ns is never exceeded. Note, these numbers hold true over the entire supply and temperature range.

7. Signal Waveforms

Figures 11 to 14 show the signal waveforms at the transceiver bus terminals and the transition times (t_{RD}) for networks with 2 and 20 nodes, when the transceiver supply is 5V. Figures 15 to 18 show similar waveforms for a transceiver supply of 3.3V.

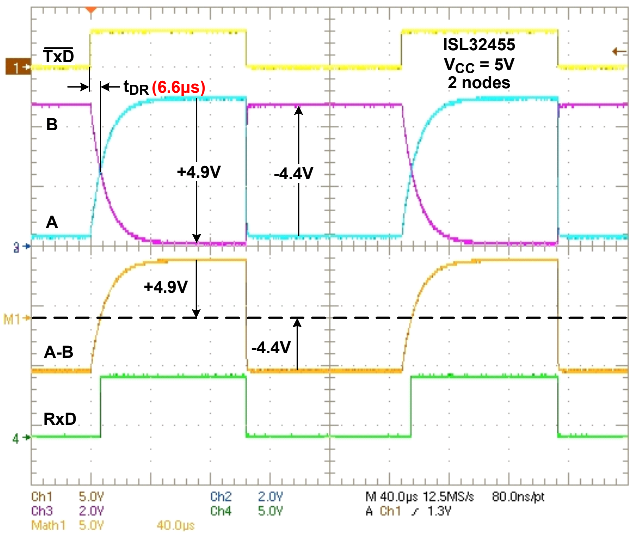

Figure 11. Transceiver Signal Waveforms: 2 Nodes, V_{CC} = 5.0V

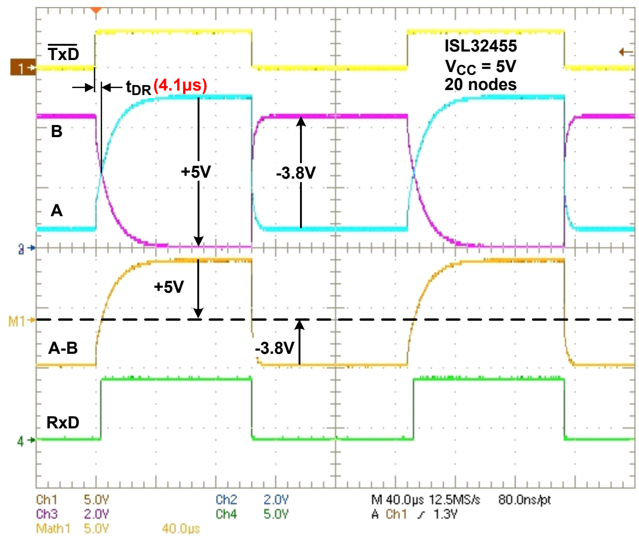

Figure 12. Transceiver Signal Waveforms: 20 Nodes, V_{CC} = 5.0V

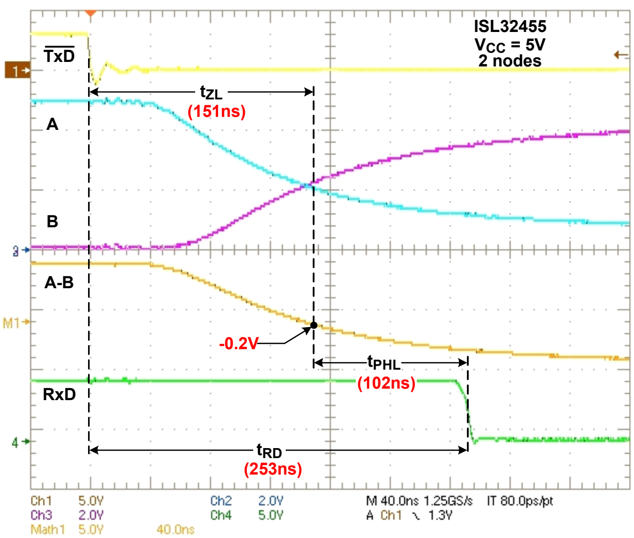

Figure 13. HIGH to LOW Transition: 2 Nodes, V_{CC} = 5.0V

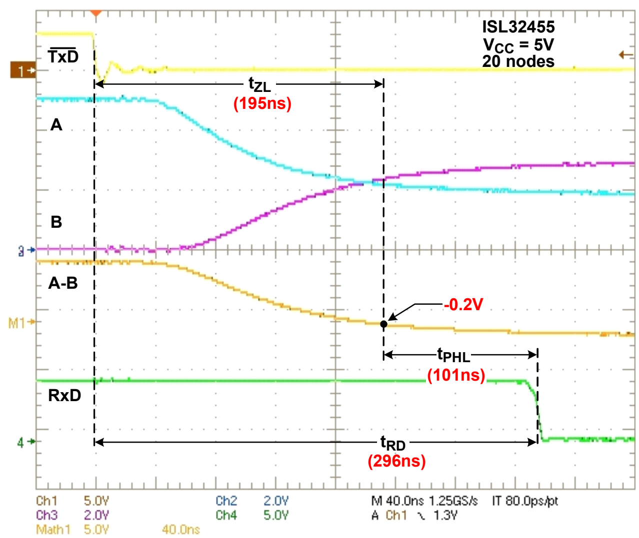

Figure 14. HIGH to LOW Transition: 20 Nodes, V_{CC} = 5.0V

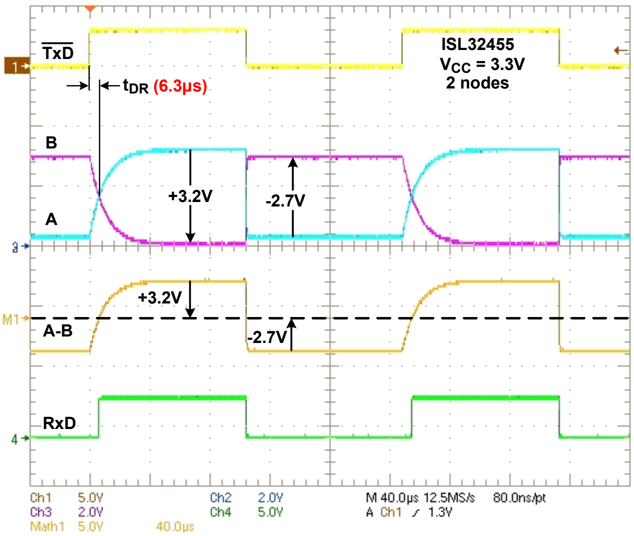

Figure 15. Transceiver Signal Waveforms: 2 Nodes, V_{CC} = 3.3V

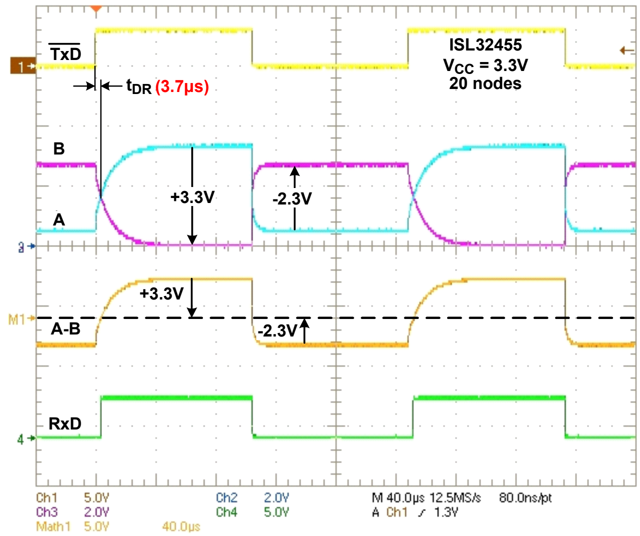

Figure 16. Transceiver Signal Waveforms: 20 Nodes, V_{CC} = 3.3V

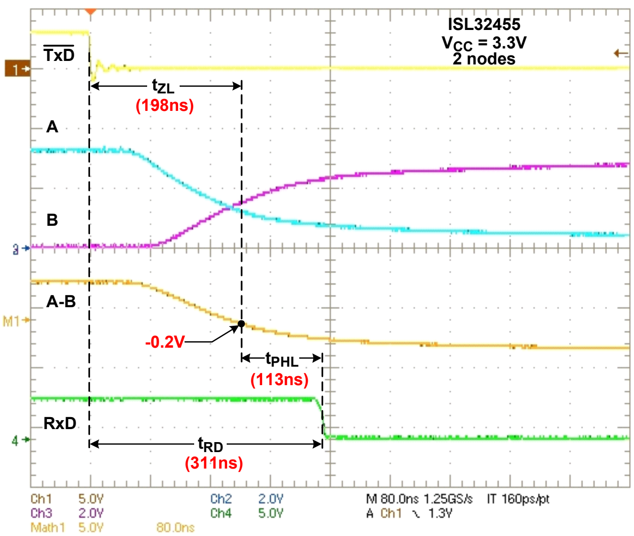

Figure 17. HIGH to LOW Transition: 2 Nodes, V_{CC} = 3.3V

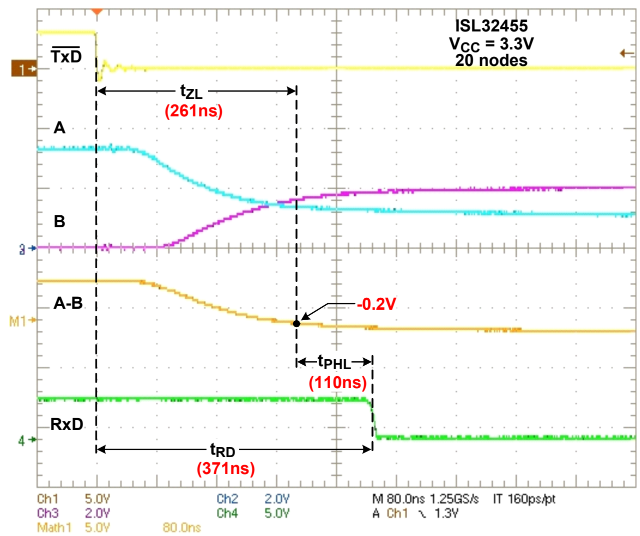

Figure 18. HIGH to LOW Transition: 20 Nodes, V_{CC} = 3.3V

8. Conclusion

The combination of Renesas microcontrollers and RS-485 transceivers not only simplifies the design of J1708 bus nodes, but also ensures reliable data transmission over a wide common-mode range while protecting your bus node against high overvoltages.

9. Revision History

Rev.	Date	Description
0.00	Feb 7, 2018	Initial release

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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