ISL70244SEH and ISL70444SEH

Reducing Power Dissipation with Saturated Outputs

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Abstract

High slew rate op amps are designed to have low quiescent current, yet have a class A-B drive into every internal node which can slew. The A-B drive allows the amplifier to increase its internal bias currents when driving internal nodes, especially those with compensation capacitors, to drive them quickly. As a result of this, any time the amplifier is attempting to drive the output to a place where the output cannot reach due to saturation, the internal bias/drive currents increase to try and drive it there. In the case of the ISL70x44SEH (ISL70244SEH and ISL70444SEH), when the output is driven to the supply rails saturating the output, the A-B drive into the output transistors contributes a bulk of the supply current, with the A-B drive of the input stage contributing a smaller additional amount. There are two applications where this increased supply current for the ISL70x44SEH can occur, one is a comparator setup (without feedback) and the other is any configuration where the outputs are driven into saturation for an extended period in time. This application note will discuss both scenarios.

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1. Applications That Cause a Supply Current Increase

From a worst case perspective, this scenario is exacerbated when the ISL70x44SEH is used as a comparator. Figure 1 is a simplified schematic of the ISL70x44SEH configured as a comparator. In this particular configuration, the positive power supply is at 18V, while the negative supply is at -18V. The positive and negative inputs are tied to 18V and 0V respectively with in-line 10kΩ resistors.

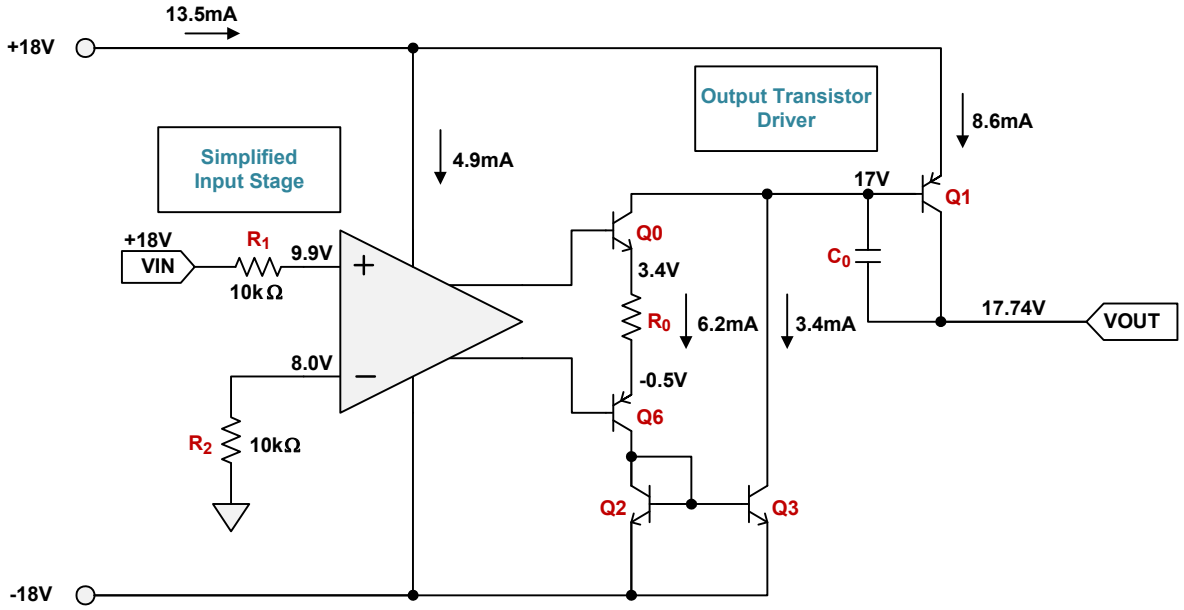

Figure 1. Simplified Schematic of ISL70x44SEH as a Comparator with +18V Differential Across the Inputs

Under this condition (or the other condition stated in the opening), the class A-B pre-driver which drives the output transistors can pull higher amounts of current out of the bases of the output transistor (Q1). The current flowing in each section of the amplifier are annotated in Figure 1 showing a total of 13.5mA of supply current from a single channel (the extra 1mA coming out of the base of Q1 is a result of the over simplification of the op amp schematic and is due to additional circuitry not being shown). The input stage currents do rise as well but not to the levels that the output does as their drive is gained up by the output stages. This increased supply current is affected by several factors such as power supply voltage, temperature, and the differential input voltage. The power supply configuration (split supply or single supply) does not have a major impact on the results so for sake of brevity, the following graphs only show the split supply configuration. The input voltage differential sweep was limited to ±700mV in order to stay within the range of the input anti-parallel diodes. The following data is typical data and is intended to show the trend between input differential and current increase.

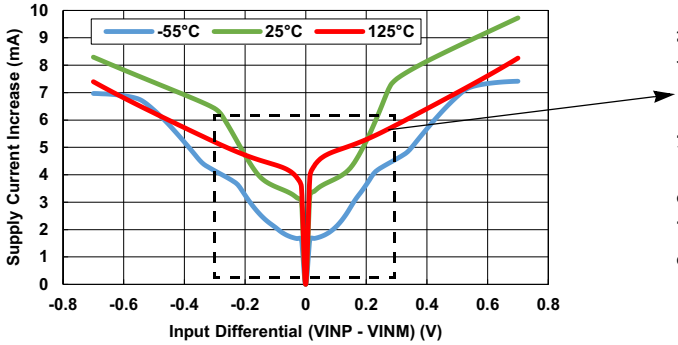

Figure 2. Typical Input Differential Voltage vs I_{SUPPLY} Increase (±18V)

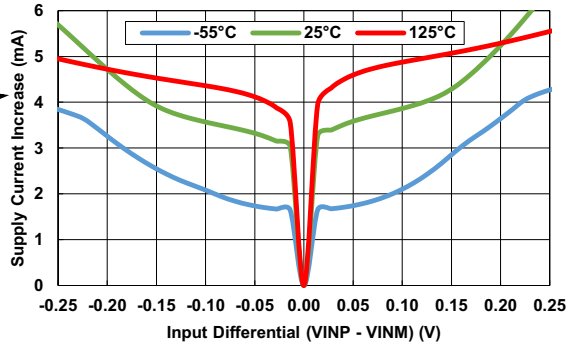

Figure 3. Typical Input Differential Voltage vs I_{SUPPLY} Increase (±18V) (zoomed in)

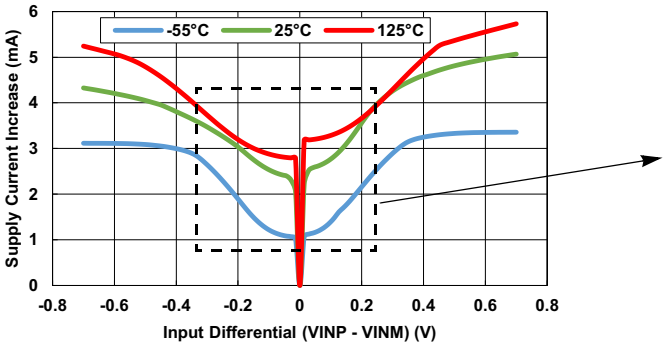

Figure 4. Typical Input Differential Voltage vs I_{SUPPLY} Increase (±2.5V)

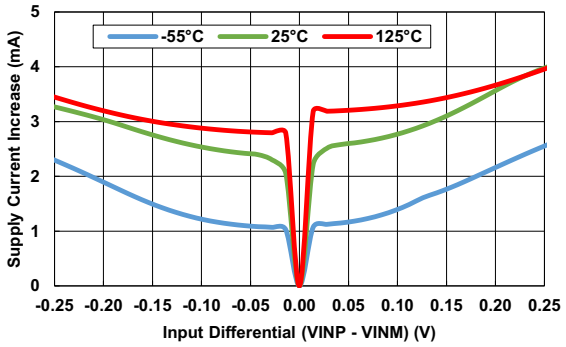

Figure 5. Typical Input Differential Voltage vs I_{SUPPLY} Increase (±2.5V) (zoomed in)

Design simulations were used to observe the increased supply currents for larger differential input voltages. Figure 6 is a design simulation result for the setup shown in Figure 1, the positive input was swept from +18V to -18V with the negative input at GND. This result correlates with the bench data when looking at voltages inside ±0.7V. As it can be seen in Figures 2 through 7, in a comparator configuration (without feedback), a relatively small voltage difference between the inputs is sufficient to trigger the supply current increase.

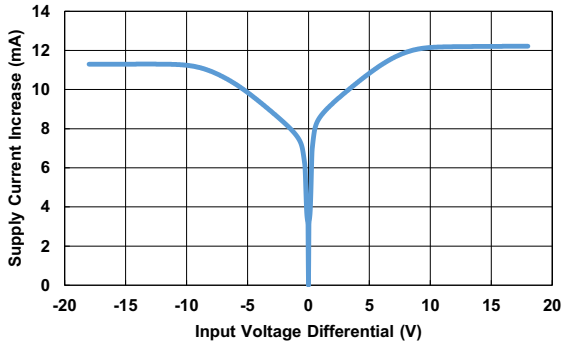

Figure 6. Simulation Input Differential Voltage vs I_{SUPPLY} Increase (±18V)

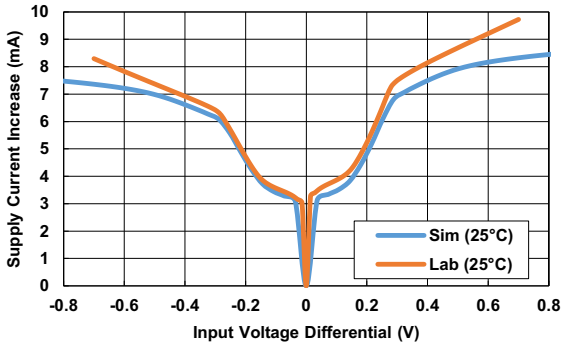

Figure 7. Simulation vs Typical Lab Data Correlation

A possible application work around that would make the ISL70x44SEH work as a comparator should be is shown in Figure 8 on page 4. In this setup, the output will swing from the Zener voltage (5V + V_{REF} in this case) to a diode below V_{REF}. As long as (5V + V_{REF}) and (V_{REF} – 0.7V) are not near the output saturation voltages, this would not cause a supply current increase. V_{REF} can either be a dedicated voltage reference or a resistor divided voltage from V+ that is set to ensure that V_{REF} - 0.7V will still meet the V_{IL} of the downstream device.

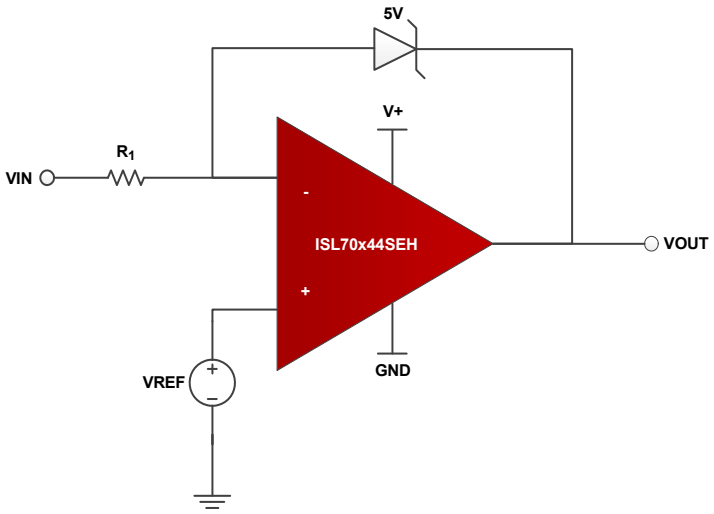

Figure 8. Application Setup to Use ISL70444SEH as a Comparator

Other configurations (with feedback) where the output is allowed to saturate will also exhibit the increase in supply current. Typical configurations are a single supply buffer where the input will be near ground or the positive supply (Figure 9) or the typical configuration for unused channels (Figure 10).

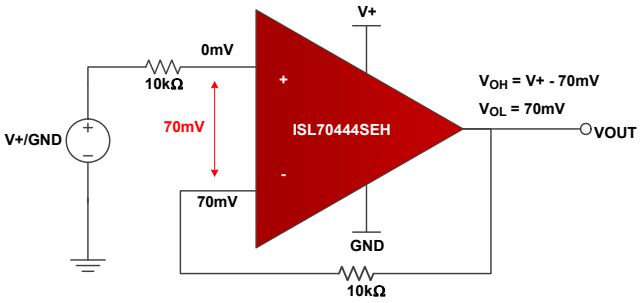

Figure 9. ISL70x44SEH Configured as a Single Supply Buffer (±18V)

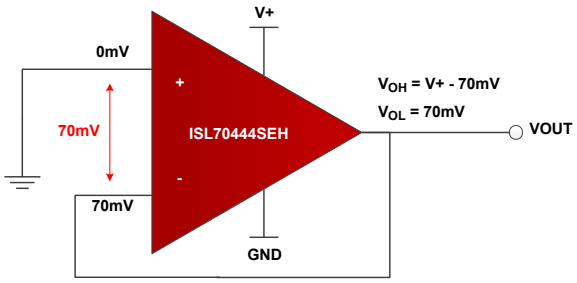

Figure 10. ISL70x44SEH Unused Channel Configuration

In Figure 9, the positive input is tied to ground and the output of the ISL70x44SEH will try to get as close to ground as it can, which in this case is its V_{OL} level of ~70mV (typical) with its supplies at ±18V. This causes a 70mV differential between the inputs which, according to Figure 3 on page 2, translates to a 3.4mA supply current increase. Table 1 shows typical lab data of the ISL70x44SEH configured as shown in Figure 9. As it can be seen, topologies with or without feedback can both exhibit the same increase in supply current if they have the same constant differential voltage across the input pins.

Table 1. Typical Supply Current Increase for the ISL70x44SEH Configured as a Single Supply Buffer with Input at either GND or V+.

	-55°C (mA)	+25°C (mA)	+125°C (mA)
±18V	1.30	3.44	4.06
36V	1.26	3.49	3.92
±2.5V	1.01	2.36	2.48
5V	0.96	2.42	2.47

For the ±2.5V and 5V supply settings, the V_{OH}/V_{OL} of the part is around 50mV (typical) which, according to Figure 5 on page 3, should be around 2.4mA, and this agrees with the lab data. The supply current increases shown in Table 1 are the same whether the input is at negative supply or the positive supply. One thing to note is that the V_{OH} and V_{OL} levels are dependent on the output load, the saturation voltages mentioned so far are for unloaded outputs. The V_{OH}/V_{OL} levels will move further away from either supply with more loading and can cause larger supply current increases.

The proper way to configure unused single supply op amps to avoid the supply current increase can be seen in Figure 11. A good rule of thumb would be to follow Figure 11 when the negative power supply is more than or equal to -1.0V, otherwise follow the configuration shown in Figure 12. The resistors in Figure 11 are of equal value and high resistance (≥10kΩ) to minimize current draw, while keeping the positive input at mid-supply. All unused op amps on the same voltage rails can have their inputs tied to the same resistor divider to minimize the number of components.

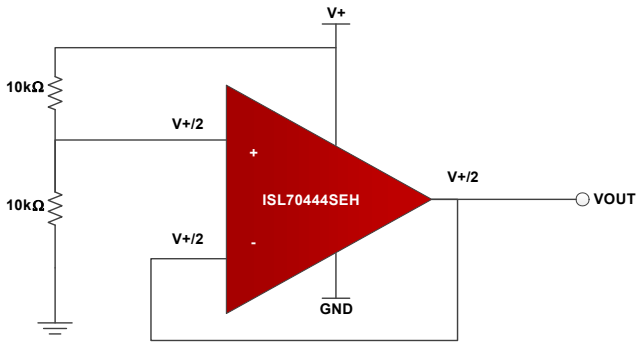

Figure 11. Recommended Configuration for Unused Op Amp Configuration to Minimize Power Dissipation

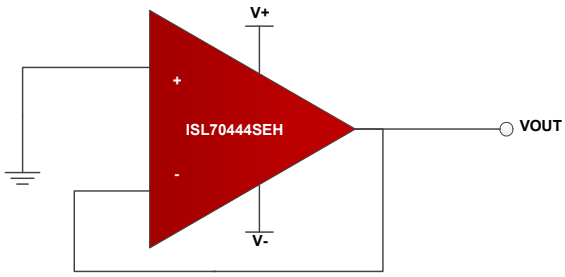

Figure 12. Recommended Configuration for Unused Op Amp Configuration for Split Supplies

2. Thermal Considerations

Design simulations indicate that Q3 in Figure 1 on page 2 is the device that will dissipate the most power (0.12W worst case). To add some margin on top of that the following thermal simulation will assume a 0.15W dissipation in a 48.5x38x18µm Si element surrounded by a 2µm wall oxide tub. Figures 13 through 15 show the results of the thermal simulation.

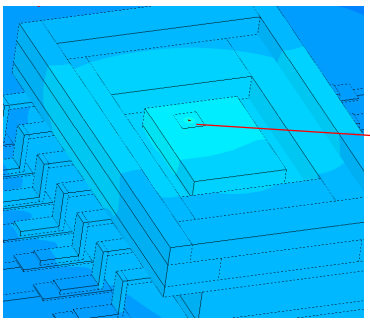

Figure 13. Thermal Simulation of 0.15W Spot Heating (Lid is hidden)

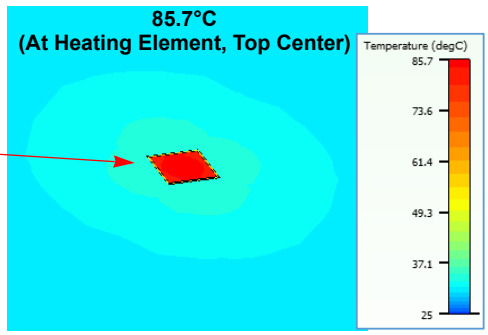

Figure 14. Zoomed In to Spot Where Most of the Power is Dissipated

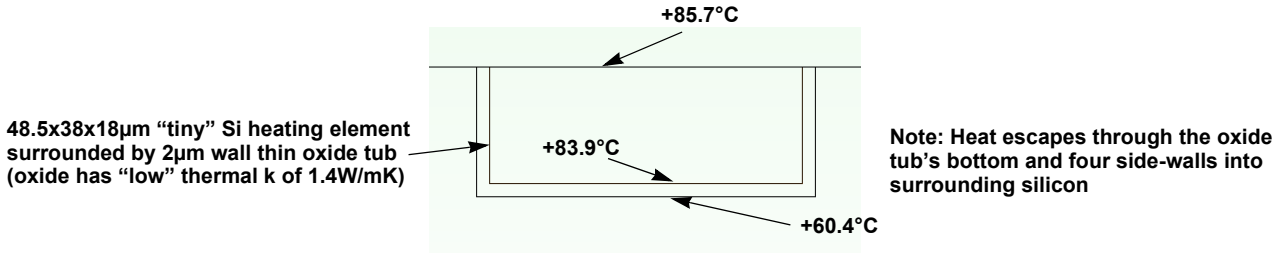

Figure 15. Temperature Spread Across Device Dissipating Power

The results from the thermal simulation shown in Figure 15 provided a θ_{JC} of 374°C/W for the Q3 in Figure 1 on page 2. It is important to note that Figure 1 only shows half the output stage, and that Q3 will only dissipate power if the output is railed high. When the output is railed low, the respective thermal resistance for the hot spot becomes 458°C/W. These thermal resistances are much higher than the normal θ_{JC} of 9.0°C/W where the heat is evenly spread across the die. Despite the larger thermal resistances for the spot heating, as long as the junction temperature is maintained at or below +150°C, there are no reliability implications.

3. Example of Finding the Safe Operating Case Temperature

To understand what this supply current increase means (using Figure 10 on page 4) let’s take an example scenario where there is 36V between V+ and V- (V- = GND), three op amps are working under normal conditions (where the output is not saturated), and the fourth op amp is configured as a buffer with its input grounded. Calculating the temperature rise due to the dissipated power will help determine the maximum allowable case temperature.

Use Equation 1 to calculate the maximum allowable case temperature.

(EQ. 1) $$T_C = 150°C - [(0.080W \bullet n \bullet \theta_{JC(p)}) + (A \bullet m \bullet \theta_{JC(p)}) + (B \bullet \theta_{JC(spot)})]$$

where:

n = number of unsaturated op amps

m = number of saturated op amps

A = value from Table 2

B = value from Table 3

$\theta_{JC(p)}$ = 9.0°C/W

$\theta_{JC(spot)}$ = 458°C/W when output is saturated low or 374°C/W when saturated high

Table 2. Total Wattage for Amplifier

Condition	Output Saturated Low (W)	Output Saturated High (W)	Active (W)
Buffer (Op Amp with Feedback)	0.244	0.262	0.080
Comparator (No Feedback)	4.001	3.557	-

Table 3. Total Wattage for Hot Spot

Condition	Output Saturated Low (W)	Output Saturated High (W)	Active (W)
Buffer (Op Amp with Feedback)	0.093	0.108	-
Comparator (No Feedback)	0.006	0.021	-

The three unsaturated op amps have a worst case power dissipation of 0.080W per amplifier, the fourth amp has a worst case dissipation of 0.244W and a spot heating dissipation of 0.093W (output saturated low). The θ_{JC} when heat is spread across the die is 9.0°C/W and 458°C/W for the spot heating transistor. Multiplying the thermal resistances with their respective power dissipations we get the following temperature rises:

Table 4. Temperature Rise for Each Condition Using Worst Case (+6 Sigma) Power Dissipation

Condition	Wattage (W)	θ_{JC} (°C/W)	Temperature Rise (°C)
Three Op Amps (Unsaturated)	0.080 * 3	9.0	2.17
One Op Amp (Unused, Input Low)	0.244 * 1	9.0	2.20
Spot Power Dissipation (Input Low)	0.093	458.0	42.61
		Total Rise:	46.97

Subtracting the total temperature rise of 46.97°C from the maximum junction temperature of +150°C, results in an allowable maximum case temperature of +103.03°C. As long as the case temperature is maintained below +103.03°C, the spot heating does not rise above +150°C and there is no reliability implications to the device. An excel tool is available that automates the calculations above for various power supply voltages.

4. Life Test Results

Renesas has performed a Life Test on the ISL70444SEH with all four amplifiers configured as buffers with their outputs railed high (worst case power dissipation condition – excluding comparator applications). Pre and post ATE data show zero failures for the 48 units (across 3 wafer lots) tested, which had junction temperatures in excess of +150°C during the life test. The results from the life test conclude that extended operation (800 hours) with all four channels as railed buffers does not represent a reliability threat if the case temperature is maintained at +135°C or less. For more details on the life test please refer to TB516.

5. Conclusion

This increased current needs further consideration for only two applications. We recommend not using this device as a comparator or in a configuration where the outputs are driven into full saturation for an extended period of time. However, if a comparator application is needed, we recommend using the configuration in Figure 8 on page 4. Unused channels should follow the configuration shown in Figure 11 on page 5 for single supply or split supply applications when the V- pin is between ground and -1V, otherwise the input can be tied to ground (as shown in Figure 10 on page 4). Following these guidelines will help avoid any unnecessary power dissipation. In cases where the recommended configurations cannot be followed, Equation 1 on page 6 can be used to calculate the maximum allowable case temperature to ensure that the absolute maximum junction temperature of +150°C is not exceeded.

6. Revision History

Rev.	Date	Description
1.00	Nov 22, 2021	Fixed excel_tool link on page 7.
0.00	Sep 12, 2018	Initial release

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