

Developing a Voltage-Feedback SPICE Op-Amp Macromodel

Introduction

A voltage-feedback amplifier macromodel has been developed that simulates the most common effects, such as transient response, frequency response, voltage noise and input/output slew rate limiting. This application note describes each stage of the macromodel and presents simulation results that demonstrate correlation with typical device performance.

Macromodels provide a practical means of simulating device behavior without requiring access to proprietary transistor-level designs. Of course, the most accurate simulations are conducted from fully-extracted 3-D device models. Not only would it be impractical to share these models because of the need to accommodate the numerous simulation platforms, but also because of proprietary reasons.

One of the first op-amp macromodel techniques was developed by Boyle in 1974 and used only two transistors, a few diodes and linear elements^[1]. Linear elements like resistors, capacitors, inductor and voltage/current control sources simulate much faster than active elements and are used to provide poles, zeros and any gain. For a DC model, a voltage-controlled voltage source can represent the amplifier while resistances can be added to better represent the input and output impedance. Capacitors, inductors, diodes and transistors can then provide the proper AC response. For more information on the development of simulation models, see Alexander and Bowers referenced documents^{[2][3]}.

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1. BOYLE, G.R., D.O. Pederson, B.M. Cohn, J.E. Solomon, *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE J. 1974, SC-9.
2. Derek Bowers, Mark Alexander, Joe Buxton, *A Comprehensive Simulation Macromodels for Current Feedback Operational Amplifiers*, IEEE Proceedings, Vol. 137, April 1990 pp.137-145
3. Mark Alexander, Derek Bowers, *AN-138 SPICE-Compatible Op Amp Macro-Models*, Analog Devices Inc., Application Note 138.

1. ISL28133 Macromodel Architecture

The ISL28133 serves as an example implementation of the voltage-feedback amplifier macromodel described in this application note. The ISL28133 is a zero-drift operational amplifier with voltage-feedback topology. Intended for low frequency and power precision applications, the gain bandwidth product is 400kHz, the slew rate is 0.1V/ μ s, and the supply current is 18 μ A. Figure 1 shows the five-stage macromodel used to represent the ISL28133. The five stages are the input stage, the gain stage, the frequency-shaping stage, the output stage, and the noise module.

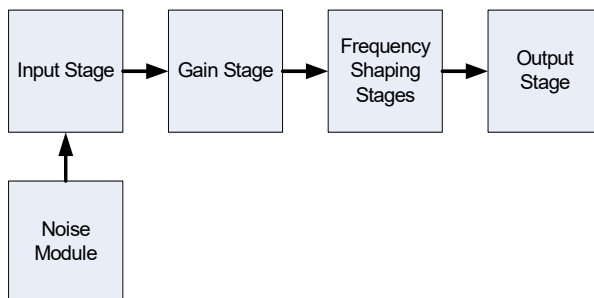


Figure 1. ISL28133 Macromodel Block Diagram

1.1 Input Stage

The input stage of the zero-drift amplifier is shown in Figure 2. The 100 μ A current source I2 feeds the PMOS input pair. Normally, I2 should be chosen less than the quiescent current. Remember, the ISL28133's typical supply current ($R_L = \text{open}$) is only 18 μ A. However, a small I2 ($\sim 10\mu$ A) would make the input voltage noise too large to emulate. This relationship is discussed in Noise Modeling. Choose I2 = 100 μ A and use I1 to compensate back to the total quiescent current. Cin1 and Cin2 are the input common mode capacitance and Cdiff is the input differential mode capacitance.

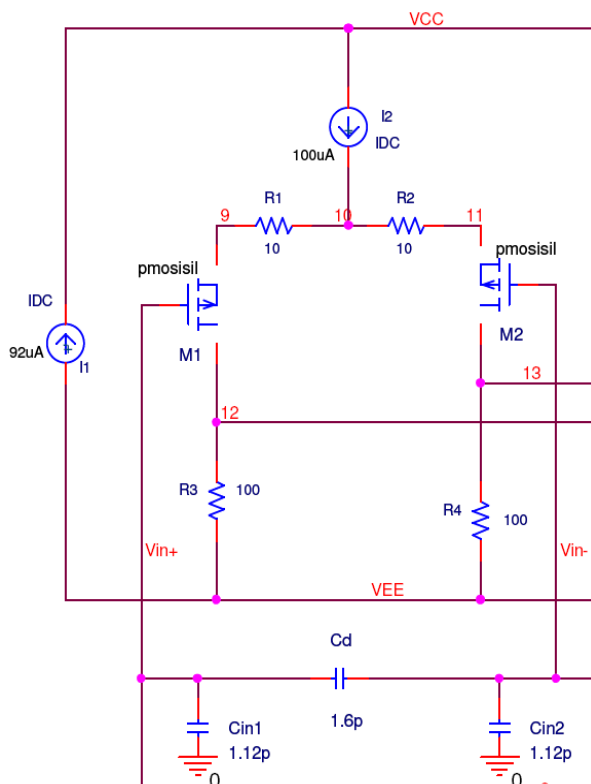


Figure 2. Input Stage

1.2 Gain Stage

The Gain stage (Figure 3) performs the following functions:

- Sets the DC gain of the part.
- Provides slew-rate limiting
- Establishes the dominant pole
- Level shifts the differential input signal to a single-ended signal referenced to mid-supply
- Limits the full-scale output swing

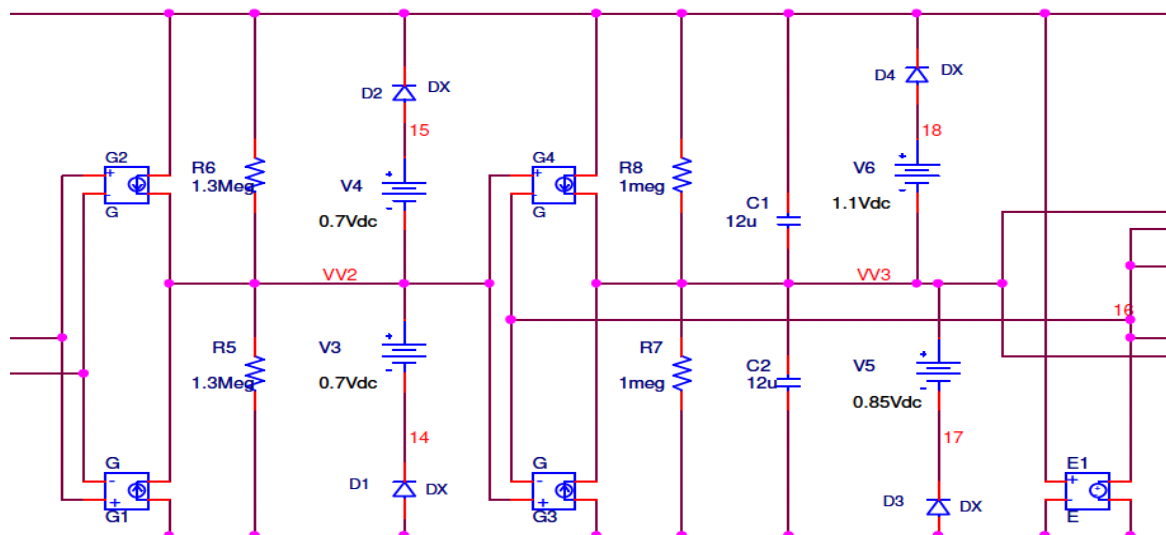


Figure 3. Gain Stage

Referring to Figure 3, Ga is the gain of block G1 and G2. Gb is the gain of block G3 and G4.

$$(EQ. 1) \quad \text{Slew Rate} = \frac{I_2 \times R_3 \times G_a \times R_5 \times G_b}{C_1}$$

Changing the value of V3 and V4 limits the slew rate. Also, R8/C1 and R7/C2 decide the dominant pole of this model. E1 is used to set the reference level at the middle of Vcc and Vee.

1.3 Frequency-Shaping Stages

Cascaded frequency-shaping techniques are commonly used in op-amp macromodel development. It is easy to add more poles and zeros. Each frequency-shaping block provides unity gain. A zero-pole pair is included in this model and shown in [Figure 4](#).

$$(EQ. 2) \quad R_{10} = R_{11} = 1M\Omega$$

$$(EQ. 3) \quad R_9 = R_{12} = R_{10} \times \left(\frac{f_p}{f_z} - 1 \right)$$

$$(EQ. 4) \quad L_1 = L_2 = \frac{R_9}{2\pi f_p}$$

A higher order pole stage is shown in [Figure 5](#), G7/8, R13/14, and C3/4.

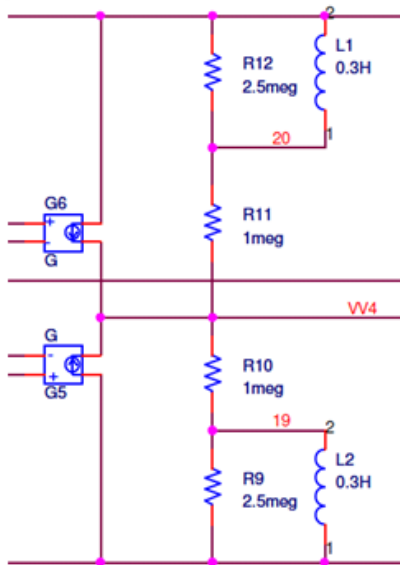


Figure 4. Zero-Pole Pair Stage

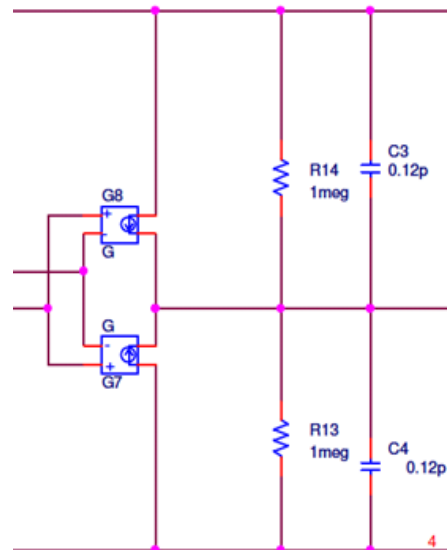


Figure 5. Higher Order Pole Stage

1.4 Noise Modeling

The typical input current noise ($\sim 70\text{fA}$) is sufficiently small, therefore, it is neglected in this model. The voltage noise of the MOSFET can be modeled using the following equations.

$$(EQ. 5) \quad V_i^2(f) = 4kT \left(\frac{2}{3} \right) \frac{1}{g_m} + \frac{K}{WLC_{ox}f}$$

$$(EQ. 6) \quad g_m \propto \sqrt{I_D}$$

I_D is the drain current. High bias current in the model is required to emulate the low voltage noise. At the input stage, the tail current is set high enough to generate the low input voltage noise. Before the noise sources are added, the model has to be rendered lower noise than the spec or typical performance noise curve in the *ISL28133 Datasheet*. The noise-voltage module of Figure 6 generates $1/f$ and white noise by using a 0.1V voltage source biasing a diode-resistor series combination. White noise is generated by the thermal noise-current.

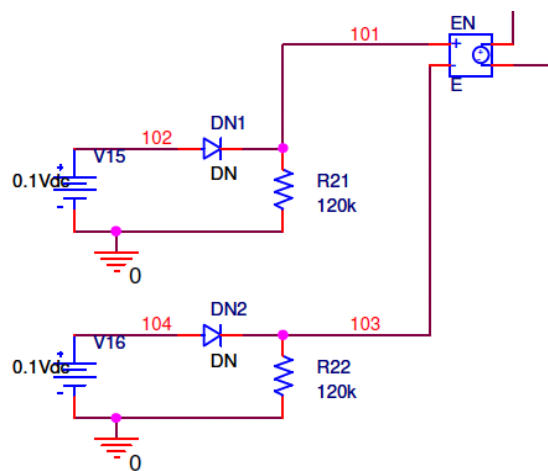


Figure 6. Noise Voltage Module

$$(EQ. 7) \quad i_n^2 = \frac{4kT}{R}$$

where k is the Boltzmann's constant. So, the required value of the resistor for a given noise-voltage spectral density is:

$$(EQ. 8) \quad R = \frac{e_n^2}{2 \times 4kT}$$

where e_n is the spectral density of the white noise voltage. The design of the chopper stabilized amplifier greatly reduces $1/f$ noise. $1/f$ noise (flicker noise) refers to the noise exhibiting power spectral density inversely proportional to the frequency.

$$(EQ. 9) \quad S_N \propto \frac{1}{|f|^\beta} \quad \beta > 0$$

More generally, the noise with the spectral density is also called $1/f$ noise. Normally, the frequency where the flicker noise curve crosses the white noise curve is defined as the corner frequency. The small amount of flicker noise that remains is modeled within the SPICE diode model. Referring to Figure 6,

$$(EQ. 10) \quad i_n^2 = 2qI_d + KF \times \frac{I_d^{AF}}{\text{frequency}}$$

I_d is the DC diode current. AF and KF are the model parameters of the SPICE diode and q is the charge of the electron. The flicker noise exponent (AF) is set to 1 and the flicker noise coefficient (KF) is set

$$(EQ. 11) \quad KF = \frac{E_a^2}{2R^2 \times I_d}$$

where E_a is the noise-voltage spectral density at 1Hz. The simulated voltage noise will show the 1/f noise-voltage spectral density with the correct corner frequency.

1.5 Output Stage

After the frequency shaping-stages, the signal appears at Node VV5, which is referenced to the midpoint of two supply rails. Each controlled source can generate enough current to support the required voltage drop across its paralleled resistor. R15 and R16 are equal to twice the open loop output resistance, so their parallel combination gives the correct Z_{out} . D5-D8 and G9/10 are used to force a current from the positive rail to the negative rail to correct the real current sink or source in the supply pins.

$$(EQ. 12) \quad G9 = G10 = G11 = G12 = \frac{1}{2Z_{out}}$$

$$(EQ. 13) \quad R15 = R16 = 2Z_{out}$$

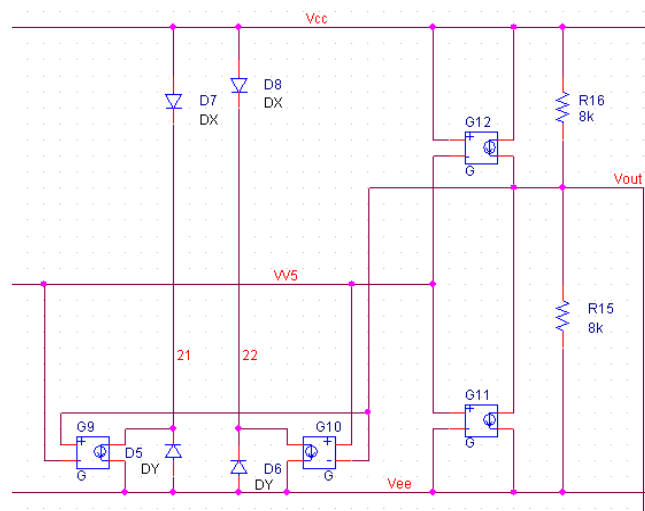


Figure 7. Output Stage

1.6 Model Validation

Some SPICE simulation results are compared with the typical performance curve from the *ISL28133 Datasheet* in the following. (Figure 8 is from the datasheet).

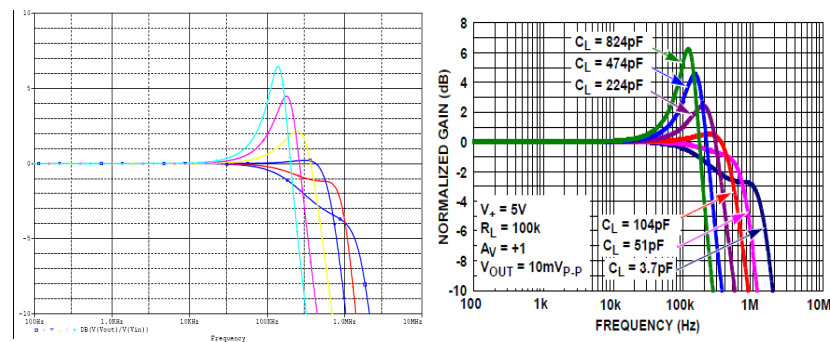


Figure 8. Gain vs Frequency vs Load Capacitance.

Note: It cannot be very accurate because the parasitic capacitance on the board was not included in the model. the error is less than 5%.

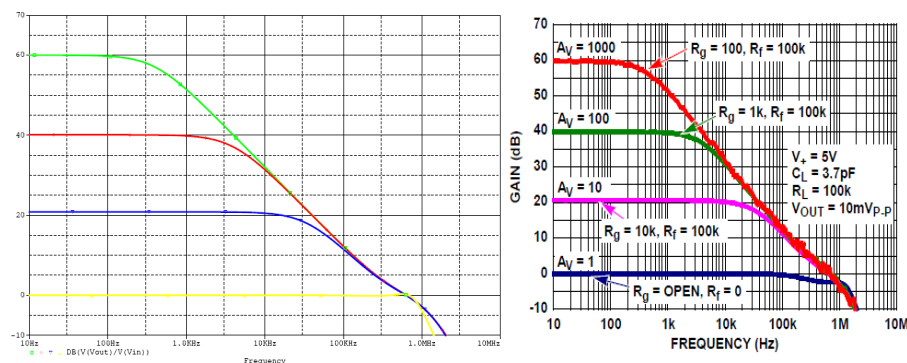


Figure 9. Frequency Response of Closed Loop Gain with Different Gain.

Note: At Gain = 100, the bandwidth is 3.94kHz and the error is less than 5%. At low gain, the bandwidth is expanded because of the zero-pole pair.

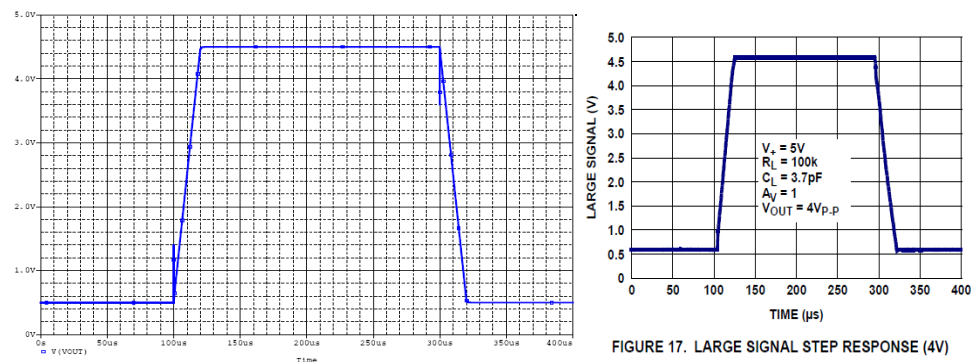


Figure 10. Large Signal Step Response.

Note: The slew rate simulated is 0.198V/μs and the error is 1%.

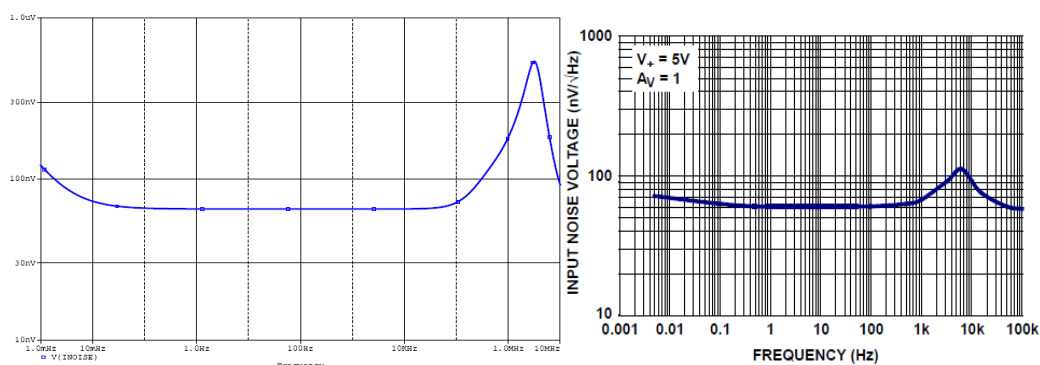


Figure 11. Input Noise Voltage vs Frequency

Note: At 1kHz, the simulated input noise voltage is 64.9nV/Hz, very close to the value in the datasheet 65nV/Hz. The simulated curve cannot catch the peak near 10kHz.

2. Conclusion

A SPICE macromodel for a voltage-feedback amplifier has been developed that accurately represents transient response, AC performance, DC characteristics, and voltage noise. This macromodel includes effects such as transfer response, accurate AC response, DC offset and voltage noise. It is easy to add more features such as CMRR, PSRR, and input current-noise. Also, it is convenient to change the parameters of the model to fit other voltage-feedback amplifiers. The same modeling topology can also be adapted to several other Renesas voltage-feedback amplifiers.

3. ISL28133 Macromodel Netlist

```

* ISL28133 Macromodel
* Revision B, April 2009
* AC characteristics, Voltage Noise
* Connections: +input
*
*          | -input
*          |   | +Vsupply
*          |   |   | -
Vsupply
*          |   |   |   |
output
*          |   |   |   |
|
.subckt ISL28133 3 2 7 4 6
*
*Voltage Noise
D_DN1      102 101 DN
D_DN2      104 103 DN
R_R21      0 101 120k
R_R22      0 103 120k
E_EN       8 3 101 103 1
V_V15      102 0 0.1Vdc
V_V16      104 0 0.1Vdc
*
*Input Stage
C_Cin1     8 0 0.4p
C_Cin2     2 0 2.0p
R_R1       9 10 10
R_R2       10 11 10
R_R3       4 12 100
R_R4       4 13 100
M_M1       12 8 9 9 pmosisil
+ L=50u
+ W=50u
M_M2       13 2 11 11 pmosisil
+ L=50u
+ W=50u
I_I1       4 7 DC 92uA
I_I2       7 10 DC 100uA
*
*Gain stage
G_G1       4 VV2 13 12 0.0002
G_G2       7 VV2 13 12 0.0002
R_R5       4 VV2 1.3Meg
R_R6       VV2 7 1.3Meg
D_D1       4 14 DX
D_D2       15 7 DX
V_V3       VV2 14 0.7Vdc
V_V4       15 VV2 0.7Vdc
*
*SR limit first pole
G_G3       4 VV3 VV2 16 1
G_G4       7 VV3 VV2 16 1
R_R7       4 VV3 1meg
R_R8       VV3 7 1meg
C_C1       VV3 7 12u
C_C2       4 VV3 12u
D_D3       4 17 DX
D_D4       18 7 DX
V_V5       VV3 17 0.7Vdc
V_V6       18 VV3 0.7Vdc
*
*Zero/Pole
E_E1       16 4 7 4 0.5
G_G5       4 VV4 VV3 16 0.000001
G_G6       7 VV4 VV3 16 0.000001
L_L1       20 7 0.3H
R_R12      20 7 2.5meg
R_R11      VV4 20 1meg
L_L2       4 19 0.3H
R_R9       4 19 2.5meg
R_R10      19 VV4 1meg
*Pole
G_G7       4 VV5 VV4 16 0.000001
G_G8       7 VV5 VV4 16 0.000001
C_C3       VV5 7 0.12p
C_C4       4 VV5 0.12p
R_R13      4 VV5 1meg
R_R14      VV5 7 1meg
*
*Output Stage
G_G9       21 4 6 VV5 0.0000125
G_G10      22 4 VV5 6 0.0000125
D_D5       4 21 DY
D_D6       4 22 DY
D_D7       7 21 DX
D_D8       7 22 DX
R_R15      4 6 8k
R_R16      6 7 8k
G_G11      6 4 VV5 4 -0.000125
G_G12      7 6 7 VV5 -0.000125
*
.model pmosisil pmos (kp=16e-3 vto=10m)
.model DN D(KF=6.4E-16 AF=1)
.MODEL DX D(IS=1E-18 Rs=1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28133

```

Figure 12. SPICE Net List

4. Revision History

Revision	Date	Description
1.00	Sep 28, 2026	<ul style="list-style-type: none"> ▪ Applied the latest template ▪ Added Revision History section. ▪ Updated Title and applied minor text updates throughout.
0.00	Feb 20, 2012	Initial release

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