AN1619
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Designing with ISL6752DBEVAL1Z and ISL6754DBEVAL1Z Control Cards

Introduction

The ISL6752DBEVAL1Z and ISL6754DBEVAL1Z are DC-DC power supply controllers on plug-in daughter cards. Both cards utilize Intersil's ZVS resonant switching full bridge topology specifically intended for off-line, 500W or greater applications.

These two controllers are basically the same except for the method used for current limiting. The ISL6752DBEVAL1Z uses pulse by pulse current limiting while the ISL6754DBEVAL1Z uses Intersil's patented average current limiting technique. Both control cards have secondary referenced voltage error amplifiers with a linear opto-isolator used to transition the primary to secondary boundary.

These cards also provide control signals to drive Synchronous Rectifiers (SRs). An optional control circuit is provided for diode emulation.

This design guide references the power topology of the ISL6752_54EVAL1Z power supply which comes complete with both of these daughter cards. The daughter cards are also available as stand alone evaluation boards to be used with customer provided power stages. Reviewing the ISL6752_54EVAL1Z ZVS DC-DC Power Supply with Synchronous Rectifiers-User Guide, AN1603, is highly recommended.

Scope

This application note will cover the methods for compensating the voltage error amplifier using current mode control. Biasing the peak current limit of the ISL6752 and ISL6754 is also reviewed. It is assumed that the reader has fundamental understanding of the peak current mode control. Familiarity with application note, AN1262, "Designing with the ISL6752, ISL6753 ZVS Full-bridge Controllers" is also recommended.

Also covered is the compensation of the average current limit error amplifier of the ISL6754.

Another subject covered by this application note is implementation requirements for proper operation of the ISL6754 when transitioning from voltage regulation to current regulation.

Basic Design Considerations

The ISL6754DBEVAL1Z uses two error amplifiers. One error amplifier is used to regulate the output voltage when the output load current is below the current limit value. The other error amplifier is used to regulate the output current when the output current is equal to the average current limit value. In this design example, the current amplifier is internal to the ISL6754. An external op-amp is used as the voltage amplifier.

The output of the two error amplifiers are connected together with an OR-ing diode, as shown in the simplified schematic of Figure 1. When the voltage amplifier is in control of the output, the output of the amplifier is within the control range of the PWM comparator (~ 0V to 5V). The output of the current amplifier is at the positive rail because it is demanding for more current on the output. Because the output of the current amplifier is more positive than the voltage amplifier, the OR-ing diodes block the current amplifier from controlling the output and is effectively operating open loop.

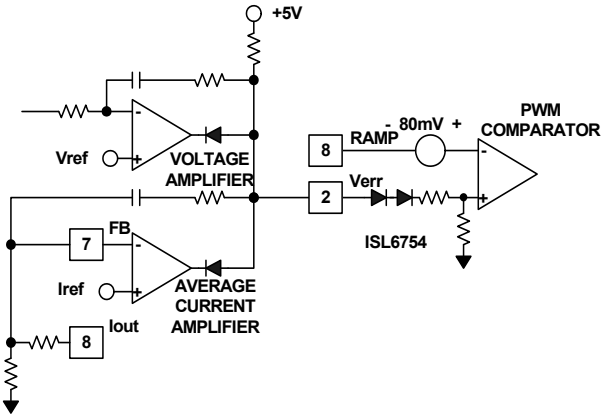

FIGURE 1. TWO AMPLIFIERS CONNECTED TO ONE PWM COMPARATOR

When the output load current exceeds the average current limit value, the output of the current amplifier slews rapidly down to the control range of the PWM comparator to regulate the output current. Because the output load current is being limited, the output voltage sags resulting with the output of the voltage error amplifier increasing towards the positive rail voltage. The voltage error amplifier is now operating open loop. Because only one or the other amplifier is in control of the output, it is sufficient to compensate each amplifier independently of the other.

The designer does have to decide how rapidly he or she wants the transition from voltage control to current control to occur. Usually the load transient performance specification determines the compensation for the voltage error amplifier.

There are other considerations for the compensation of the current amplifier. If it is desirable to allow momentary high amplitude load transients that exceed the current limit value, then the current amplifier should be compensated to respond slowly to the load transient. Because it is still necessary to limit the peak load transient current to some safe level, the pulse by pulse current limit of the ISL6754 should be biased to allow the highest acceptable load transient amplitude.

In applications where it is desirable to rapidly limit the output current to the current limit value, the current amplifier can be compensated to provide nearly instantaneous limiting to the current limit value. The transition can be made so fast that the pulse by pulse current may never activate.

With both fast and slow transitions between voltage and current regulation, it is necessary to insure that the minimum input voltage of -0.3V is not exceeded on the FB pin of the ISL6754. When the output of the voltage amplifier is slewing down towards the control range of the PWM comparator, the negative dv/dt on the VERR pin will cause current to flow through the compensation capacitor of the current error

amplifier resulting with a negative transient on the FB pin. A similar effect can occur on the external amplifier.

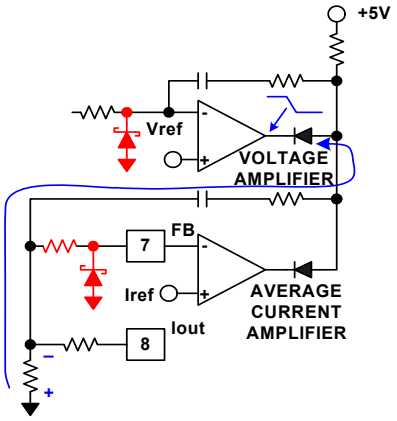

FIGURE 2. VOLTAGE CLAMPS TO PREVENT EXCESSIVE NEGATIVE TRANSIENTS ON FB

A simple solution to the problem is to implement a negative voltage clamp on this pin, as shown in Figure 2. It may also be necessary to have a similar clamp on the negative input pin of the external amplifier depending on how it responds to excessively negative transients.

About this Analysis

The following design procedure is available in a native MathCad file created with MathCad ver. 14. This file may work with older versions of MathCad but it has not been evaluated with any version other than 14. New MathCad versions, when available, will probably maintain backwards compatibility.

The topology used for this analysis is the ISL6752_54EVAL1Z, which uses a current doubler secondary. This analysis does not consider the center tap rectification topology. Calculations for the CT topology must be derived by the user.

For those readers who are not familiar with MathCad, the following symbols are defined as follows:

:=	Assignment operator. The variable on the left side is assigned the value on the right side
=	This is the usual equals operator. The value of a symbol on the left is displayed on the right
= (bold type)	This operator is used to assign any expression to a symbol. It is used most frequently when variables of multiple independent equations are evaluated using the find() function

In most cases, this analysis uses ordinary math rules for precedence and can be understood by readers who are not familiar with MathCad. For detailed help with features and functions of MathCad that are incorporated in this analysis, please refer to the MathCad 14 Users Guide.

Included at the end of this application note are the schematics and the PCB layouts of the ISL6752DBEVAL1A and the ISL6754DBEVAL1Z control cards.

Related Literature

1. AN1262, “Designing with the ISL6752, ISL6753 ZVS Full Bridge Controllers”, Application Note
2. AN1603, “ISL6752_54EVAL1Z ZVS DC-DC Power Supply with Synchronous Rectifiers-User Guide”, Application Note
3. FN6754,“ZVS Full-Bridge PWM Controller with Adjustable Synchronous Rectifier Control”, Data Sheet
4. FN9181,“ZVS Full-Bridge Current-Mode PWM with Adjustable Synchronous Rectifier Control”, Data Sheet
5. “ISL6752_54DBEVAL1Z Board Design.mcdx”, Native MathCad Design File

References

[1] MathCad 14 Users Guide

[2] Unitrode Application Note U-97” Modelling, Analysis and Compensation of the Current-mode Converter”

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Biasing the ISL6752_54EVAL1Z Using Current Mode Control

There are seven major design steps in this analysis:

1. Set the oscillator frequency.
2. Calculate the value of the current sensing resistor, Rs, for peak current limit.
3. Set the slope compensation ratio for peak current mode control for the voltage error amplifier.
4. Establish the DC biasing of the average current limit amplifier (ISL6754 only).
5. Determine the small signal gain of the peak current mode power stage for bode analysis.
6. Compensate the voltage error amplifier.
7. Compensate the current error amplifier (ISL6754 only)

Unless otherwise specified, the following analysis applies to both the ISL6752 and the ISL6754 evaluation daughter cards (ISL6752DBEVAL1Z and ISLI6754DBEVAL1Z). Because these two boards use different reference designators, this analysis uses designators as defined by the equivalent schematics shown in this document. When applicable, a cross reference table is included to identify the specific parts on each board vs. the reference designator used in this analysis.

The following parameters are for the ISL6752_54EVAL1Z power supply. With appropriate changes to power components, these parameters can be modified to satisfy a custom application.

Input and output parameters:

$V_{bus\_max} := 450V$	maximum input operating voltage
$V_{bus\_nom} := 400V$	nominal input operating voltage
$V_{o\_nom} := 12V$	max output voltage
$V_{o\_min} := 0V$	min output voltage (short circuit)
$I_{out\_PK} := 65A$	max for pulse by pulse current limit
$I_{out\_min} := 0A$	no load
$I_{out\_avg} := 60A$	Average current limit

Component parameters:

$L_{ind} := 3.3 \cdot \mu H$	output inductance
$N_t := 13$	turns ratio of the power transformer
$N_{ct} := 50$	turns ratio of the current sensing transformer
$V_{CL} := 1V$	Peak Current Limit voltage
$L_{pri} := 3200\ \mu H$	primary magnetizing inductance of the power transformer
$C_T := 180pF$	Oscillator timing capacitor
$RTD := 6.65K\Omega$	Timing capacitor discharge resistor (used to set dead time)

Step 1) Setting the Oscillator Frequency

$T_C := 11.5 \cdot K\Omega \cdot C_T = 2.07 \cdot \mu s$

Charge time for CT as defined in the data sheet. Note that T_C is increased by the presence of the CT slope transistor Q1. To minimize the loading on the CT pin, the beta of Q1 should be greater than 200.

$T_D := 0.06 \cdot RTD \cdot C_T + 50ns = 122 \cdot ns$

Discharge time for CT (as defined in the data sheet). This is also the dead time between the two FETs on one side of the full bridge.

$P := T_C + T_D = 2.192 \cdot \mu s$

Calculated PWM period for one half cycle

$Freq := (2 \cdot P)^{-1} = 228.121 \cdot KHz$

This is the frequency of the full bridge and of each output current doubler inductor. Note that the actual switching frequency of the ISL6752 54EVAL1Z is 200KHz because of the loading effects of Q1 on the CT pin.

$D_{max} := \frac{P - T_D}{P} = 0.944$

This is the maximum duty cycle

$V_{bus\_min} := \frac{2}{D_{max}} \cdot N_t \cdot V_{o\_nom} = 330.361\ V$

This is the input voltage at which the output begins regulation.

Step 2) Rs for pulse by pulse current limit

The nominal Duty cycle for each current doubler inductor:

$$D_{nom\_ind} := \frac{V_{o\_nom}}{V_{bus\_nom}} \cdot N_t = 0.390$$

The nominal on period for $V_{o\_nom} = 12\,V$ and $V_{bus\_nom} = 400\,V$:

$$T_{on} := 2 \cdot P \cdot D_{nom\_ind} = 1.71 \cdot \mu s$$

I_{upramp} is the Δ i of the current in one output inductor of the current doubler topology.

$$I_{upramp} := \left(\frac{\frac{V_{bus\_nom}}{N_t} - V_{o\_nom}}{L_{ind}} \right) \cdot T_{on} = 9.724\,A$$

I_{pri_mag} is the Δ i of the primary side magnetizing current.

$$I_{pri\_mag} := \frac{V_{bus\_nom}}{L_{pri}} \cdot T_{on} = 0.214\,A$$

$I_{sense.p}$ is the peak output current referenced to the output of the current sensing transformer.

$$I_{sense.p} := \frac{\frac{I_{out\_PK}}{2}}{N_t \cdot N_{ct}} + \frac{\frac{I_{upramp}}{2}}{N_t \cdot N_{ct}} + \frac{\frac{I_{pri\_mag}}{2}}{N_{ct}} = 59.617 \cdot mA$$

$V_{CT.s}$ is the rising slope of the CT signal

$$V_{CT.s} := \frac{2V}{T_C} = 0.966 \cdot \frac{V}{\mu s}$$

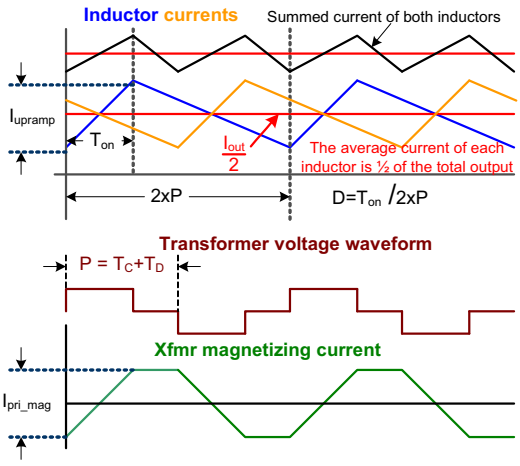
$V_{CTE.p}$ is the peak voltage as seen on the emitter of Q1 at the end of the on period:

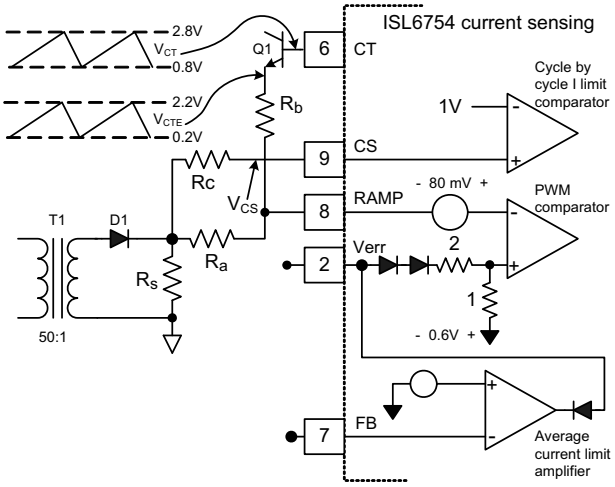
$$V_{CTE.p} := V_{CT.s} \cdot (T_{on}) + .2V = 1.852\,V \quad @\ T_{on} = 1.71 \cdot \mu s$$

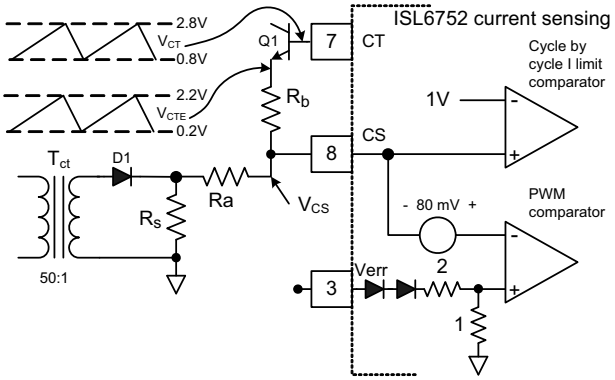
V_{CS} is the voltage that is seen on the CS input (calculated using superposition). Peak current limit occurs when V_{CS} = 1

$$V_{CS} = \frac{R_s}{R_a + R_b + R_s} \cdot V_{CTE.p} + \frac{I_{sense.p}}{R_s^{-1} + (R_a + R_b)^{-1}} = 1V$$

Period for each current doubler inductor is 2P







Step 3) Slope compensation

slope compensation ratio definition:

$$M = \frac{V_{ramp.s}}{V_{down.s}} = 1 \quad \text{or} \quad V_{ramp.s} = V_{down.s}$$

Output Inductor current down slope current scaled to the output of the current sensing transformer :

$$I_{down.s} := \frac{V_{o\_nom}}{L_{ind} \cdot N_t \cdot N_{ct}} \qquad I_{down.s} = 0.006 \cdot \frac{A}{\mu s}$$

$$V_{down.s} = \left[\frac{I_{down.s}}{R_s^{-1} + (R_a + R_b)^{-1}} \cdot \frac{R_b}{R_a + R_b} \right] = \frac{I_{down.s} \cdot R_b \cdot R_s}{R_a + R_b + R_s}$$

M = 1 is the optimal slope compensation ratio. $V_{ramp.s}$ is the ramp added to the current sense scaled to the ramp pin of the ISL6752. $V_{down.s}$ is the effective down slope ramp that is proportional to the down slope current of the output inductor also scaled to the ramp pin of the ISL6752. (reference Unitrode app note U-97)

Note that $I_{down.s}$ does not actually appear on the output of the current sensing transformer. This value is only used to scale $V_{ramp.s}$

Primary side magnetizing up slope current, $V_{mag.s}$, scaled to the output of the current sensing transformer:

$$I_{mag.s} := \frac{V_{bus\_nom}}{L_{pri} \cdot N_{ct}} = 0.003 \cdot \frac{A}{\mu s}$$

$V_{CT.s}$ and $I_{mag.s}$ both contribute to the slope compensation.

$$V_{ramp.s} = \frac{R_a + R_s}{R_a + R_s + R_b} \cdot V_{CT.s} + \frac{R_b \cdot R_s}{R_a + R_b + R_s} \cdot I_{mag.s}$$

substituting (c) and (d) into (b):

$$M = \frac{\frac{R_a + R_s}{R_a + R_s + R_b} \cdot V_{CT.s} + \frac{R_b \cdot R_s}{R_a + R_b + R_s} \cdot I_{mag.s}}{\frac{I_{down.s} \cdot R_b \cdot R_s}{R_a + R_b + R_s}}$$

Simplifying:

$$M = \frac{I_{mag.s}}{I_{down.s}} + \frac{V_{CT.s} \cdot (R_a + R_s)}{I_{down.s} \cdot R_b \cdot R_s}$$

Note that M is composed of two components. $\frac{I_{mag.s}}{I_{down.s}}$ is the slope compensation that is contributed by the magnetizing current of the power transformer

and $\frac{V_{CT.s} \cdot (R_a + R_s)}{I_{down.s} \cdot R_b \cdot R_s}$ is the injected compensation.

Solving for R_b:

(eq 2) $$R_b = -\frac{V_{CT.s} \cdot (R_a + R_s)}{R_s \cdot (I_{mag.s} - I_{down.s} \cdot M)}$$

This is the second of two equations required to solve for two Resistor variables (Rs and Rb)

Given $R_a := 499\Omega$ $R_b := 10000\Omega$ $R_s := 20\Omega$ $M := 2$

$$R_s = \frac{1V \cdot (R_a + R_b)}{V_{CTE.p} - 1V + I_{sense.p} \cdot R_a + I_{sense.p} \cdot R_b}$$

$$R_b = -\frac{V_{CT.s} \cdot (R_a + R_s)}{R_s \cdot (I_{mag.s} - I_{down.s} \cdot M)}$$

$$\begin{pmatrix} R_s \\ R_b \end{pmatrix} := \text{Find}(R_s, R_b) = \begin{pmatrix} 16.713 \\ 3431.248 \end{pmatrix} \Omega$$

$R_a = 499\,\Omega$ $R_b = 3.43 \cdot K\Omega$ $R_s = 16.71\,\Omega$

Initial estimated values (note that M can be made larger than the optimal value of 1 to overcome noise problems on the ramp input).

The following values are for the actual reference designators on the ISL6752 and ISL6754 daughter cards.

$R13 := R_a = 499\,\Omega$ $R17 := R_b = 3431\,\Omega$ $R4 := R_s \cdot 2 = 33.4\,\Omega$ $R6 := R4 = 33.4\,\Omega$

note that R4 and R6 are in parallel

Confirming the slope compensation ratio, M:

$$\frac{I_{mag.s}}{I_{down.s}} + \frac{V_{CT.s} \cdot (R_a + R_s)}{I_{down.s} \cdot R_b \cdot R_s} = 2 \qquad \frac{I_{mag.s}}{I_{down.s}} = 0.447$$

Note that the portion of slope compensation ratio contributed by $\frac{I_{mag.s}}{I_{down.s}}$ can be significant. If L_{pri} is small enough, $\frac{I_{mag.s}}{I_{down.s}}$ by itself can be be greater than 1.

Step 4) Average Current limit (ISL6754 only)

In the above calculations, the value of Rs is calculated for pulse by pulse current limiting for $I_{out\_PK} = 65\,A$. The average current limit is set to a lower value ($I_{out\_avg} = 60\,A$) to prevent the peak current limiting from interfering with the average current limit control loop.

$$V_{Iout} := \frac{I_{out\_avg}}{2 \cdot N_t \cdot N_{ct}} \cdot R_s \cdot 4 = 3.085\,V$$

This is the output voltage on the Iout pin of the ISL6754 when $I_{out\_avg} = 60\,A$.

To limit the output current to I_{out_avg}, the resistor divider of R25 and R26 are chosen so that the voltage on FB (pin 7) is .6V when $V_{Iout} = 3.085\,V$. For accurate performance, the maximum load on the Iout pin should also be limited to approximately 100 uA.

Given

$R26 := 6K\Omega \qquad R25 := 10K\Omega$

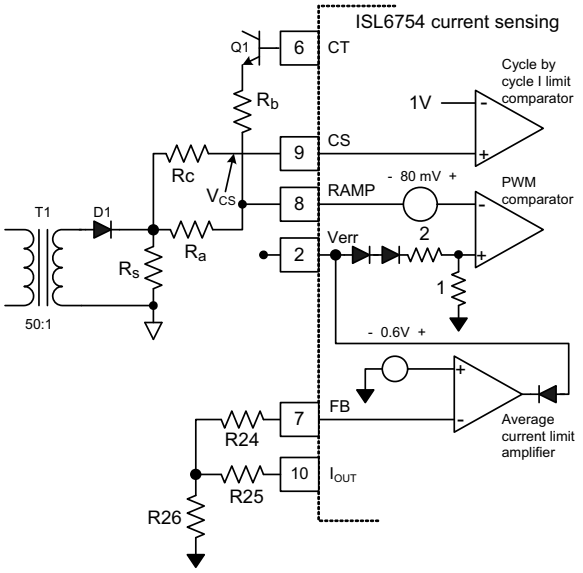
$$\frac{R26}{R25 + R26} \cdot V_{Iout} = .6V$$

$$\frac{V_{Iout}}{R25 + R26} = 100 \cdot \mu A$$

$$\begin{pmatrix} R25 \\ R26 \end{pmatrix} := Find(R25, R26) = \begin{pmatrix} 24.9 \\ 6.0 \end{pmatrix} \cdot K\Omega$$

These are the actual values used on the ISL6754DBEVAL1Z control board:

$R25 := 22100\Omega$ $R26 := 6650\Omega$

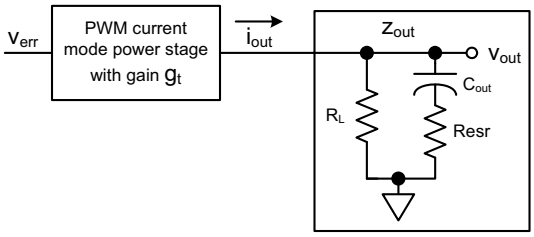


Step 5) Small Signal Gain of the Current Mode Power stage (Iout/Verr)

The input to the positive side of the PWM comparator (using superposition):

$$V_{pwm\_pos} = \frac{I_{sense} \cdot R_b \cdot R_s}{R_a + R_b + R_s} + \frac{R_a + R_s}{R_s + R_a + R_b} \cdot \left(V_{CT.s} \cdot D \cdot 2P - .6V\right) + 80mV$$

where I_{sense} and D are variables



The input to the negative side of the PWM comparator:

$$V_{pwn\_neg} = \frac{Verr - 2 \cdot V_{diode}}{3}$$ where $Verr$ is a variable

The duty cycle terminates when $V_{pmw\_pos} = V_{pwm\_neg}$:

(eq A) $$\frac{I_{sense} \cdot R_b \cdot R_s}{R_a + R_b + R_s} + \frac{R_a + R_s}{R_s + R_a + R_b} \cdot \left(V_{CT.s} \cdot D \cdot 2P - .6V\right) + 80mV = \frac{V_{err} - 2 \cdot .6V}{3}$$

Peak Current sense:

(eq B) $$I_{sense} = \frac{I_{out}}{2 \cdot N_t \cdot N_{ct}} + \frac{V_{bus} \cdot N_t^{-1} - V_o}{L_{ind} N_t \cdot N_{ct}} \cdot D \cdot P + \frac{V_{bus}}{L_{pri} \cdot N_{ct}} \cdot D \cdot P$$

The first term of eq. B is the average current of one current doubler output inductor. The 2nd term is the up slope current of one output inductor. The 3rd term is the up slope current of the primary referenced magnetizing inductance (Lpri) of the power transformer.

Duty cycle:

(eq C) $$D = \frac{V_o}{V_{bus}} \cdot N_t$$

Substituting definitions of duty cycle D, eq C, and I_{sense}, eq b, into eq A and simplifying:

$$\frac{R_b \cdot R_s}{R_a + R_b + R_s} \cdot \left(\frac{I_{out}}{2 \cdot N_t \cdot N_{ct}} + \frac{V_{bus} \cdot N_t^{-1} - V_o}{L_{ind} N_t \cdot N_{ct}} \cdot D \cdot P + \frac{V_{bus}}{L_{pri} \cdot N_{ct}} \cdot D \cdot P \right) + \frac{R_a + R_s}{R_s + R_a + R_b} \cdot \left(\frac{2 \cdot N_t \cdot P \cdot V_o \cdot V_{CT.s}}{V_{bus}} - .6V \right) + 80mV = \frac{V_{err} - 2 \cdot .6V}{3}$$

solving for I_{out} and isolating V_{err}

(eq E)

$$I_{out} = \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R_a + R_b + R_s)}{(R_b \cdot R_s)} \cdot V_{err} + \frac{N_t \cdot N_{ct} \cdot V \cdot (0.24 \cdot R_a - 0.96 \cdot R_b + 0.24 \cdot R_s)}{R_b \cdot R_s} \ldots$$
$$+ \frac{-2 \cdot N_t \cdot P \cdot V_o \cdot V_{CT.s}}{V_{bus}} \cdot \frac{2 \cdot N_t \cdot N_{ct} \cdot (R_a + R_s)}{R_b \cdot R_s} - \frac{P \cdot V_o \cdot (V_{bus} - N_t \cdot V_o)}{L_{ind} \cdot N_t \cdot N_{ct} \cdot V_{bus}} \cdot (2 \cdot N_t \cdot N_{ct}) - \frac{2 \cdot N_t^2 \cdot P \cdot V_o}{L_{pri}}$$

(eq E) is formatted as y=mx+b format where m is the slope and b is the offset of a line equation.

where:

x = V_{err}

$$m = \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R_a + R_b + R_s)}{(R_b \cdot R_s)}$$

and
b =

$$\frac{N_t \cdot N_{ct} \cdot V \cdot (0.24 \cdot R_a - 0.96 \cdot R_b + 0.24 \cdot R_s)}{R_b \cdot R_s} - \frac{2 \cdot N_t \cdot P \cdot V_o \cdot V_{CT.s}}{V_{bus}} \cdot \frac{2 \cdot N_t \cdot N_{ct} \cdot (R_a + R_s)}{R_b \cdot R_s} - \frac{P \cdot V_o \cdot (V_{bus} - N_t \cdot V_o)}{L_{ind} \cdot N_t \cdot N_{ct} \cdot V_{bus}} \cdot (2 \cdot N_t \cdot N_{ct}) - \frac{2 \cdot N_t^2 \cdot P \cdot V_o}{L_{pri}}$$

For AC analysis, V_o and V_{bus} are constants. The slope, m, is the small signal gain, g_t, used for the bode analysis of the peak current mode power stage

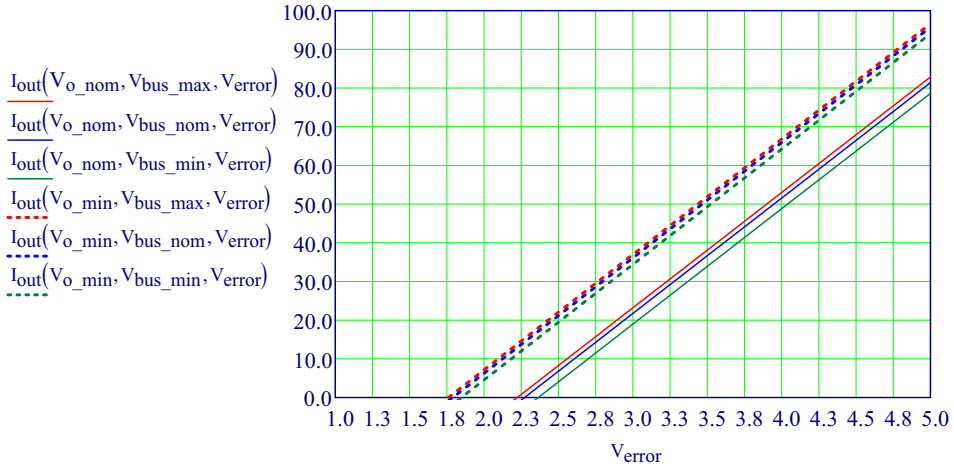
$$g_t := \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R_a + R_b + R_s)}{(R_b \cdot R_s)} \qquad g_t = 29.825 \cdot \frac{A}{V}$$

$R_a = 499\,\Omega$ $R_b = 3.431 \cdot K\Omega$ $R_s = 16.713\,\Omega$ These values are repeated here for reference.

To validate the above calculations, I_{out} is redefined as a function of V_o, V_{bus} and V_{err}

$$I_{out}(V_o, V_{bus}, V_{err}) := \left[\frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R_a + R_b + R_s)}{(R_b \cdot R_s)} \cdot V_{err} + \frac{N_t \cdot N_{ct} \cdot V \cdot (0.24 \cdot R_a - 0.96 \cdot R_b + 0.24 \cdot R_s)}{R_b \cdot R_s} \ldots \right.$$
$$\left. + \frac{-2 \cdot N_t \cdot P \cdot V_o \cdot V_{CT.s}}{V_{bus}} \cdot \frac{2 \cdot N_t \cdot N_{ct} \cdot (R_a + R_s)}{R_b \cdot R_s} - \frac{P \cdot V_o \cdot (V_{bus} - N_t \cdot V_o)}{L_{ind} \cdot N_t \cdot N_{ct} \cdot V_{bus}} \cdot (2 \cdot N_t \cdot N_{ct}) - \frac{2 \cdot N_t^2 \cdot P \cdot V_o}{L_{pri}} \right]$$

$V_{error} := 0.5V, 1V .. 5V$ $V_{o\_nom} := 12V$ $V_{o\_min} := 6V$ $V_{bus\_max} = 450\,V$ $V_{bus\_nom} = 400\,V$ $V_{bus\_min} = 330.361\,V$



The slope of these lines is the small signal gain $\frac{i_{out}}{v_{err}} = g_t$

These plots illustrate how Iout varies as V_{error}, V_{bus}, and V_o are changed. For constant $V_{o\_nom} = 12\,V$ (solid lines) or constant $V_{o\_min} = 6\,V$ (dotted lines), Vbus exhibits minimal influence on I_{out} as expected. For $V_{bus\_min} = 330.4\,V$ to $V_{bus\_max} = 450\,V$ (the operating input voltage range), I_{out} changes very little for a constant V_{error}.

As V_o is varied, between V_{o_nom} and V_{o_min}, g_t remains constant. This is also expected because the slope compensation does not changed as V_o deviates from the nominal output voltage of 12V. When V_o decreases, as it will during current limit, the down slope current of the output inductors also decreases effectively increasing the slope compensation because the injected slope compensation from Vct does not change.

$$X_{pwm} = \frac{v_{out}}{v_{err}}$$

$$g_t = \frac{i_{out}}{v_{err}} \quad \text{or} \quad v_{err} = \frac{i_{out}}{g_t}$$

$$i_{out} = \frac{v_{out}}{z_{out}} \qquad v_{err} = \frac{i_{out}}{g_t} = \frac{v_{out}}{g_t \cdot z_{out}}$$

$$X_{pwm} = \frac{v_{out}}{\frac{v_{out}}{g_t \cdot z_{out}}} = g_t \cdot z_{out}$$

$$z_{out} = \left[R_L^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s} \right)^{-1} \right]^{-1}$$

$$R_L = \frac{V_{out}}{I_{out}}$$

$$g_t = g_t \cdot \left(\frac{s}{\frac{Freq}{2} \cdot 2 \cdot \pi} + 1 \right)^{-1}$$

X_{pwm} is the gain of the PWM current mode power stage. v_{out} is the small signal output voltage and v_{err} is the small signal control voltage from the error amplifier.

g_t is the transconductance of the PWM current mode stage.

z_{out} is the load impedance on the output of the current mode power stage. R_L is the output load, C_{out} is the output capacitance and R_{esr} is the ESR of the output capacitance.

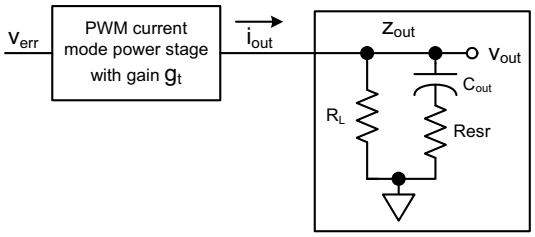
note: the impedance of two parallel components is

$$\frac{1}{z} = \frac{1}{z1} + \frac{1}{z2} \quad \text{or} \quad z = \left(z1^{-1} + z2^{-1} \right)^{-1}$$

The small signal gain has a pole at 1/2 the switching frequency (refer to **Unitrode application note U-97)**

This gain function is used in the bode analysis for the ISL6752 and ISL6754.

$$X_{pwm}(s) = g_t \cdot \left[\frac{s}{(\pi \cdot Freq)} + 1 \right]^{-1} \cdot \left[R_L^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s} \right)^{-1} \right]^{-1}$$



Step 6) Compensation of the Voltage Error Amplifier

Functions for Bode Analysis

$db(G,f) := 20\log(|G(2\pi f\cdot j)|)$ Gain in decibels of a Laplace gain function G for frequency f

$\phi(G,f) := \mathrm{mod}\left(\arg(G(2\pi f\cdot j))\cdot\frac{180}{\pi},360\right)$ Phase in degrees of a Laplace gain function G

$f_{UnityGain}(G) := |root(db(G,f),f,100,10^8)|$ Unity gain frequency of function G

$\phi_{margin}(G) := \phi(G,f_{UnityGain}(G)) + 0$ Unity gain phase margin of function G

$V_{db2V}(db_v) := 10^{(db_v\cdot 20^{-1})}$ db to voltage function

$F(f_0,f_N,N,i) :=$ Equidistant frequency data points for plotting:

```
for i ∈ 0..N
    f_i ← f_0·(f_N/f_0)^(i/N)
f
```

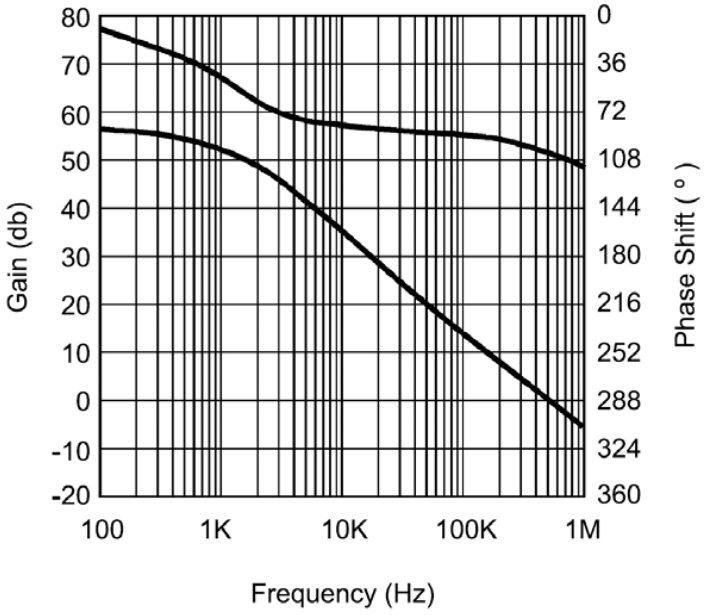
This function generates N equidistant frequency data points on the log X scale with starting frequency f_0 and ending frequency f_N

$N := 200$ $i := 0..N$

$f := F(.01,1\times10^8,N,i)$ $f_0 = 0.01$ $f_N = 100\times10^6$

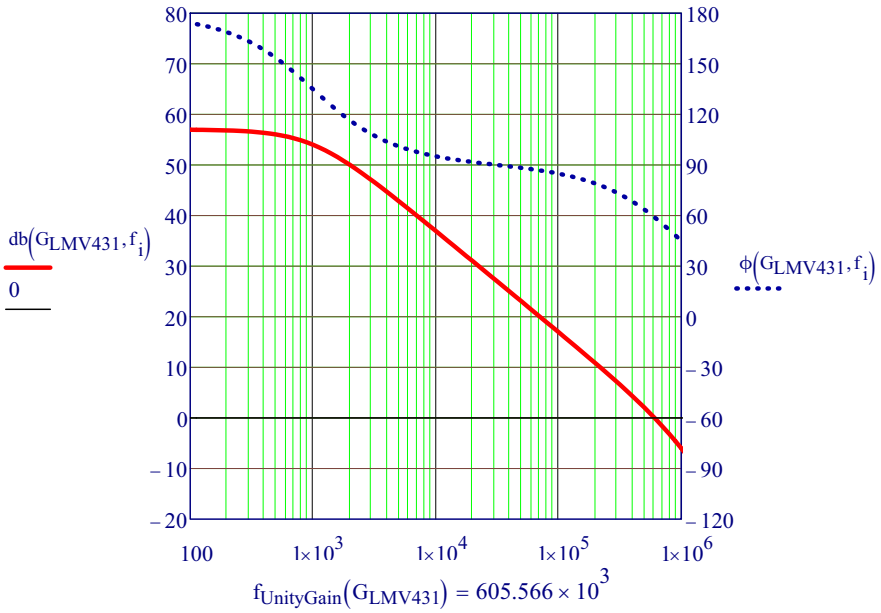
Open loop gain of the LMV431

From LMV431data sheet



The open loop transfer function of the LMV431 is created here by inserting poles as necessary to recreate the Gain/Phase plot found in the data sheet. Note that the phase shift is relative to the input.

$$G_{LMV431}(s) := \frac{-V_{db2V}(57)}{\left(\frac{s}{1000\cdot 2\cdot\pi}+1\right)\cdot\left(\frac{s}{1\times 10^{6}\cdot 2\cdot\pi}+1\right)}$$



$$f_{UnityGain}(G_{LMV431}) = 605.566\times 10^{3}$$

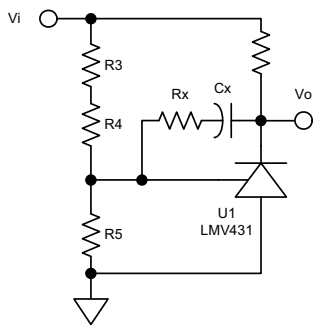
Gain of the Voltage Amplifier

For an Inverting Opamp the gain function, X(s), can be simplified to:

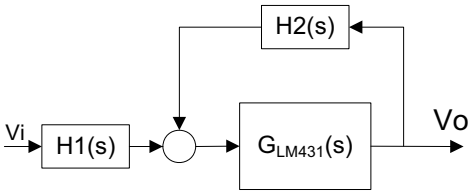
$$X_{Verror.Amp}(s) = \frac{Vo}{Vi} = \frac{H1(s)\cdot G_{LMV431}(s)}{1 - H2(s)\cdot G_{LMV431}(s)}$$

$$H1_{U1}(s,R3,R4,R5,Rx,Cx) := \frac{\left[\left(\frac{1}{Cx\cdot s} + Rx\right)^{-1} + \frac{1}{R5}\right]^{-1}}{\left[\left(\frac{1}{Cx\cdot s} + Rx\right)^{-1} + \frac{1}{R5}\right]^{-1} + (R3 + R4)}$$

$$H2_{U1}(s,R3,R4,R5,Rx,Cx) := \frac{\left[\frac{1}{(R3+R4)} + \frac{1}{R5}\right]^{-1}}{\left[\frac{1}{(R3+R4)} + \frac{1}{R5}\right]^{-1} + \left[\left(\frac{1}{Cx\cdot s} + Rx\right)^{-1}\right]^{-1}}$$



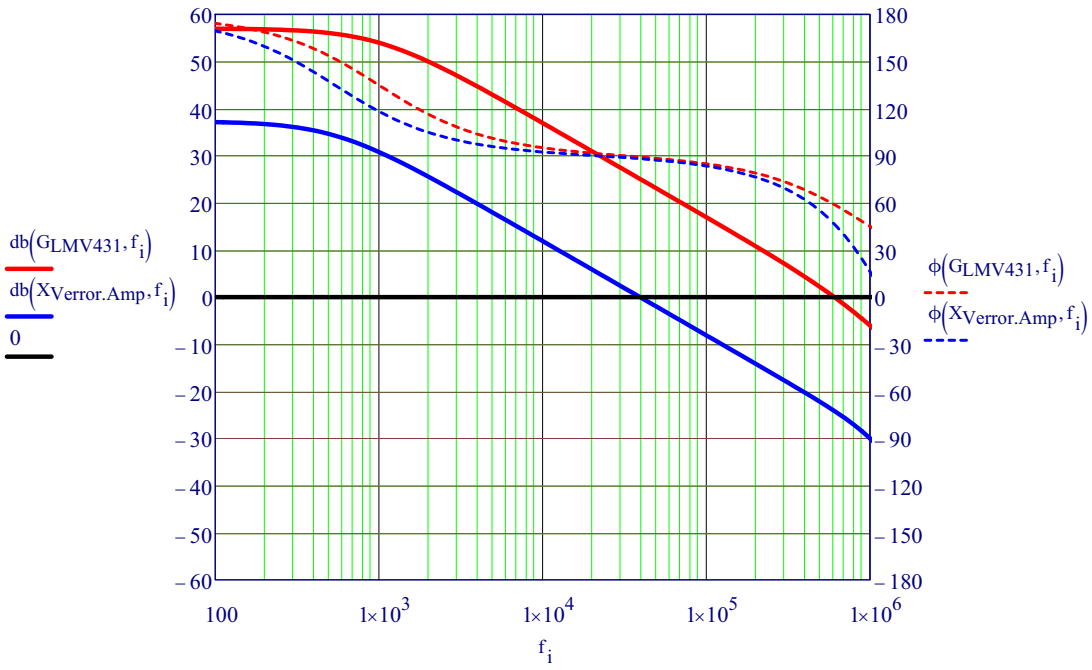
gain block diagram for an inverting amplifier



These values are used here only to illustrate and confirm the gain/phase functions

$$R3 := 18\cdot 10^{3} \qquad Cx := .1\cdot 10^{-9} \qquad R4 := 649 \qquad R5 := 2.15\cdot 10^{3} \qquad Rx := 0$$

$$X_{Verror.Amp}(s) := \frac{H1_{U1}(s,R3,R4,R5,Rx,Cx)\cdot G_{LMV431}(s)}{1 - H2_{U1}(s,R3,R4,R5,Rx,Cx)\cdot G_{LMV431}(s)}$$



Open loop gain of EL5111

(note: some earlier releases of the ISL6752DBEVAL1Z and ISL6754DVEVAL1A use the EL5120 instead of the EL5111. The EL5120 has been obsoleted and is not recommended for new designs. In this application, the EL5120 and EL5111 are interchangeable.)

From EL5111 data sheet

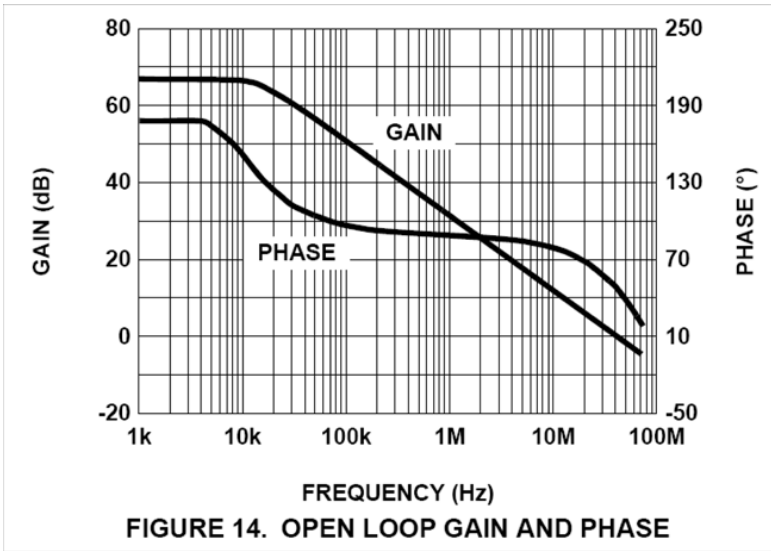
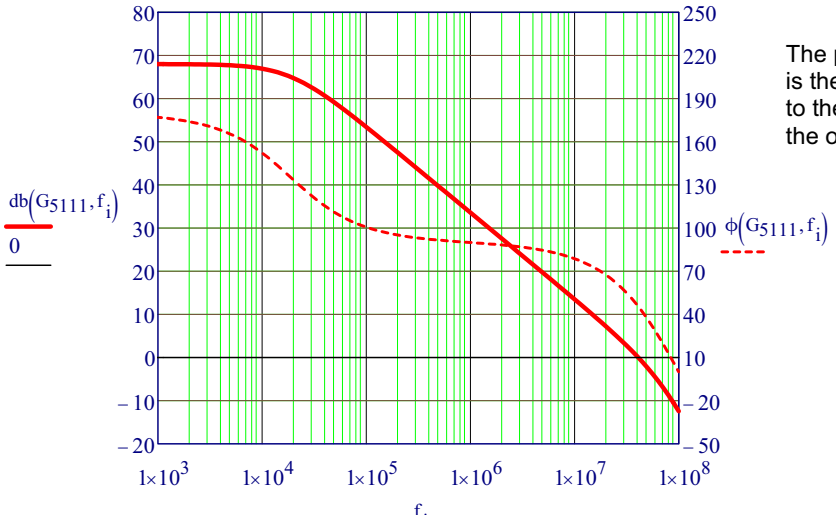


FIGURE 14. OPEN LOOP GAIN AND PHASE

Note that the phase of this graph is the output referenced to the negative input of the opamp.

The open loop transfer function of the EL5111 is created here by inserting poles as necessary to recreate the gain/phase plot found in the data sheet.

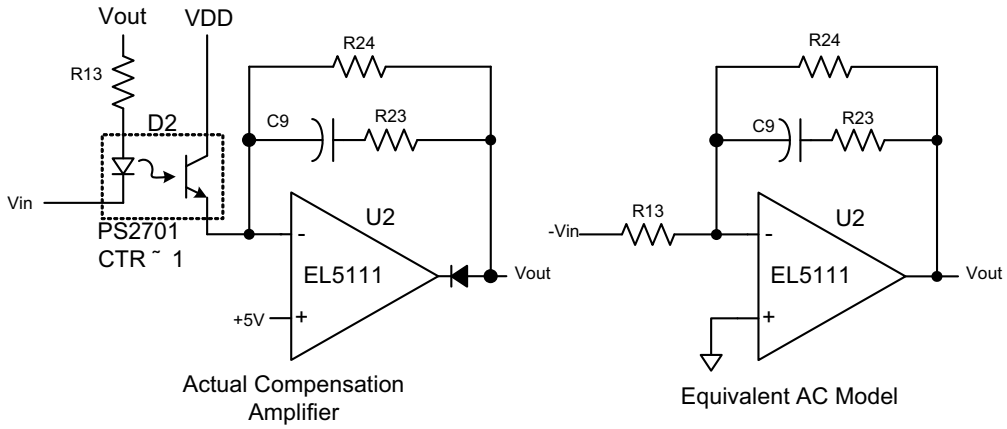
$$G_{5111}(s) := \frac{-V_{db2V}(68)}{\left(\frac{s}{19000\cdot 2\cdot\pi}+1\right)\cdot\left(\frac{s}{100\times 10^{6}\cdot 2\cdot\pi}+1\right)^{2}}$$



$$f_{UnityGain}(G_{5111}) = 40.889\times 10^{6}$$

The phase of this graph is the output referenced to the **negative** input of the opamp.

Gain of the EL5111 Compensation amplifier



The compensation amplifier provides two functional advantages. First, the optocoupler, D2, is biased with a constant voltage across the collector and emitter. The closed DC feedback loop around U2 keeps the negative input virtually at the same voltage as the positive input resulting with a constant DC voltage (VDD - 5V) across the optocoupler. The advantage of this cascode configuration is that there is no regenerative AC feed back through Ccb of the opto transistor. Consequently, the pole introduced by the optocoupler is greatly increased in frequency. The improved bandwidth of the opto removes its detrimental influence on the voltage feedback loop.

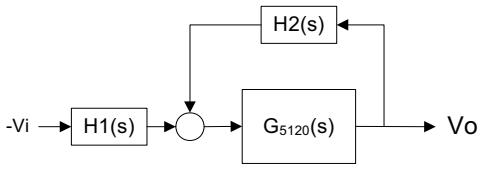
Note that R13 is the same value in the ac model as it is in the actual circuit. This is the consequence of the optocoupler having a nominal ctr = 1. Also, note the negative value of Vin in the equivalent AC Model. This is necessary because in the actual circuit, Vin and Vout at low frequencies are in phase. In the equivalent AC Model, because the opamp is an inverting configuration, Vin must be negated to preserve the correct phase of the actual circuit.

The second advantage of this opamp is that the loop compensation network is on the secondary side. Traditionally, the compensation network is applied around the LMV431. The problem is that when the average current regulator takes control of the loop to regulate the output current (by controlling the PWM input), the voltage regulator loop is opened causing the LMV431 output to saturate to the positive rail (Vout). If the voltage loop compensation is around the LMV431, the feedback network will greatly slow the slew rate (~ msecs) of the output of the LMV431. If the load is quickly reduced below the current regulation value (the current limit), the output voltage will overshoot until the output of the LMV431 slews down to the voltage necessary to regulate the output voltage (taking control away from the current regulator). This effect is especially bad for a short circuit load dump. If the loop compensation is not located around the LMV431, the output of the LMV431 will still saturate when the current regulator is in control of the PWM input, but the output is not now impeded by the local feedback and will recover very quickly minimizing the output voltage overshoot.

Note that the compensation network around U2 is decoupled from the output of U2 by the series diode on the output. This diode prevents the feedback network capacitor from charging up to the rail voltage. This same technique is used on the output of the current regulator opamp (internal to the ISL6754). In a manner similar to the voltage control loop, the output of the current regulator is saturated when the voltage loop has control. Without the diode on its output, the current regulator would also be slow to respond to an over current for the same reason as stated for the voltage regulator loop.

The voltage gain function for an Inverting Opamp:

gain block diagram for an inverting amplifier



$$X(s) = \frac{Vo}{Vi} = \frac{-H1(s)\cdot G_{5111}(s)}{1 - H2(s)\cdot G_{5111}(s)}$$

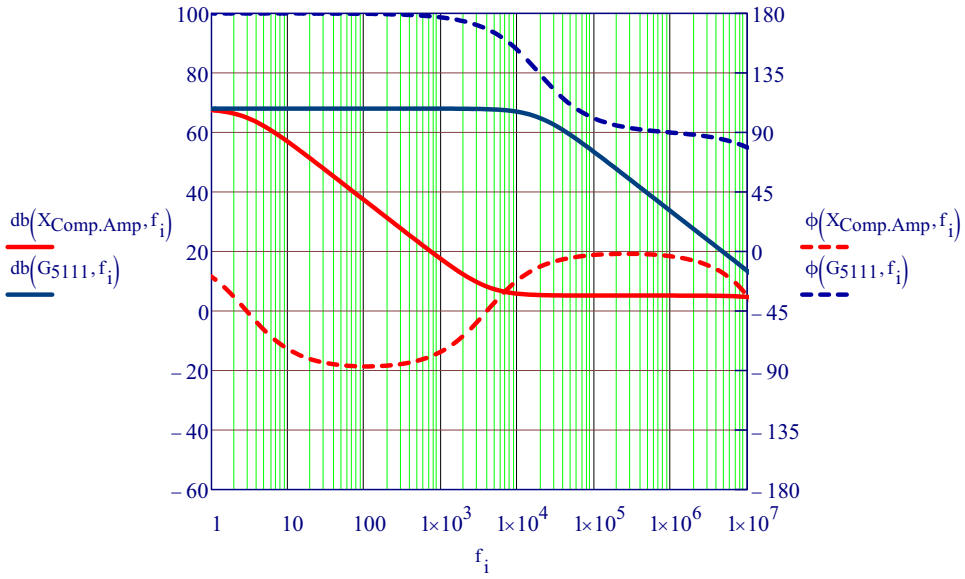
$$H1_{U2}(s, R13, R24, R23, C9, Cx) := \frac{\left[\left(\frac{1}{C9\cdot s} + R23\right)^{-1} + \frac{1}{R24} + Cx\cdot s\right]^{-1}}{\left[\left(\frac{1}{C9\cdot s} + R23\right)^{-1} + \frac{1}{R24} + Cx\cdot s\right]^{-1} + R13}$$

$$H2_{U2}(s, R13, R24, R23, C9, Cx) := \frac{R13}{R13 + \left[\left(\frac{1}{C9\cdot s} + R23\right)^{-1} + \frac{1}{R24} + Cx\cdot s\right]^{-1}}$$

These values are used here only to illustrate and confirm the compensation around the EL5111 amplifier:

$R23 := 4000 \quad R24 := 10\cdot 10^{126} \quad R13 := 2200 \quad Cx := 100\cdot 10^{-123} \quad C9 := .01\cdot 10^{-6}$

$$X_{Comp.Amp}(s) := \frac{-\left(H1_{U2}(s, R13, R24, R23, C9, Cx)\cdot G_{5111}(s)\right)}{1 - H2_{U2}(s, R13, R24, R23, C9, Cx)\cdot G_{5111}(s)}$$

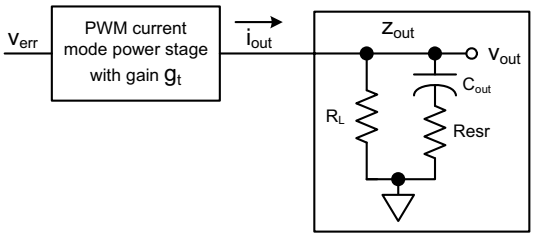


Current mode PWM power stage gain with output loads

The derivation of this small signal gain for the PWM power stage is found in step 5).

$$g_t = \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R11 + R14 + R1\_2)}{(R14 \cdot R1\_2)}$$

$$X_{pwm}(s) = g_t \cdot \left(\frac{s}{Freq \cdot \pi} + 1\right)^{-1} \cdot \left[R_L^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s}\right)^{-1}\right]^{-1}$$



Converting X_{pwm} to a function:

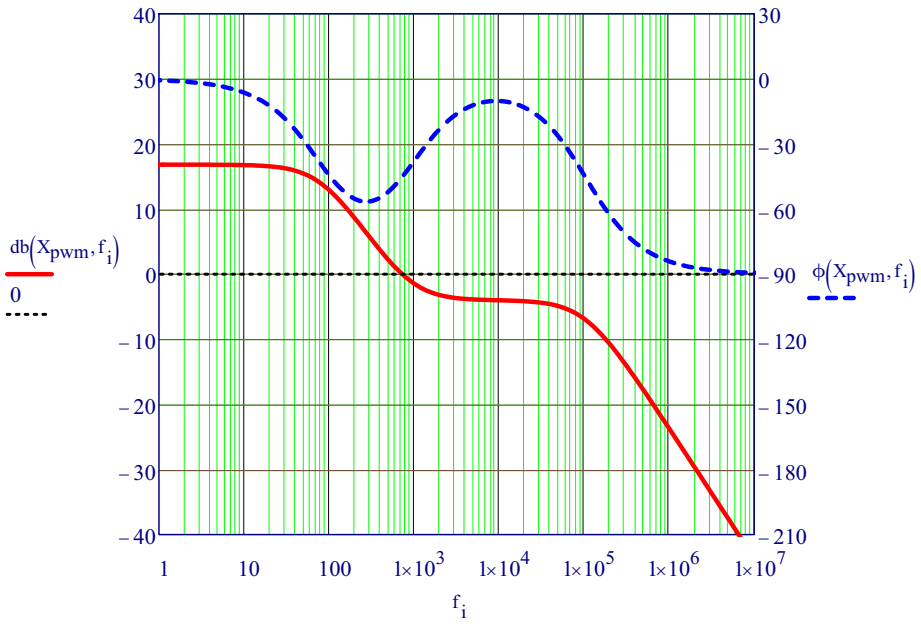
$R11 := 499$ $\quad N_t := 13$ $\quad C_{out} := 8800 \cdot 10^{-6}$ $\quad V_{out} := 12$

$R14 := 9.09 \cdot 10^{3}$ $\quad N_{ct} := 50$ $\quad R_{esr} := 0.02$ $\quad I_{out} := 60$

$R1\_2 := 13.2$ $\quad Freq := 208300$ $\quad R_L := \frac{V_{out}}{I_{out}}$

$$g_t := \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R11 + R14 + R1\_2)}{(R14 \cdot R1\_2)} = 34.678$$

$$X_{pwm}(s) := g_t \cdot \left(\frac{s}{Freq \cdot \pi} + 1\right)^{-1} \cdot \left[R_L^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s}\right)^{-1}\right]^{-1}$$



Bode plot for the total Voltage loop gain

The R_{esr} contributes significantly to the stability of the loop by introducing a zero to the bode of PWM current mode power stage. With R_{esr} = 0, the phase margin of the complete loop is at a minimum (but still stable). With increasing values of ESR, the phase margin improves and the unity grain frequency increases. The nominal value of R_{esr} of the ISL6754EVAL board is 0.02 ohms. But as operating temperatures decrease, the R_{esr} value increases resulting in the unity gain frequency approaching the PWM switching frequency. To avoid PWM switching frequency instability, it is wise to add a pole on the U2 amplifier to reduce the unity gain frequency.

In this design example, if the gain of the compensation amplifier is set for no poles and zeros (except for the inherent pole of the amplifier) by setting R23 to infinity and/or by setting C9 to a very small value (although not zero), the loop is stable without any further compensation. This is the consequence of the single pole of the LMV431 error amplifier and the zero of the PWM current mode stage canceling each other.

As with any analysis, some assumptions are made. In this bode analysis, the following assumptions were made:

1) The esl of the output capacitors are assumed not to significantly contribute the the bode of the PWM to output gain stage.

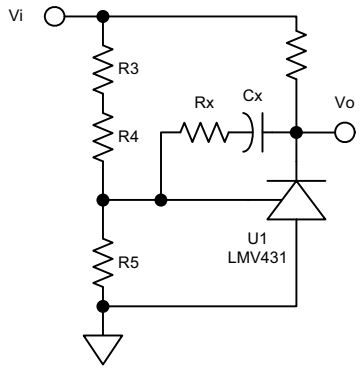
2) the turn off delays of the PWM control and bridge FETs is assumed to be insignificant. In reality, the turn off delay may result in non-linear transconductance gains of the PWM current mode stage. It is important that the turn off delays be as minimal as possible (~1% of the total PWM switching period).

3) the bandwidth of the opto transistor is assumed to be high enough to not contribute poles that affect the closed loop phase.

Because other parasitic effects may also result with unexpected loop response, it is absolutely necessary to actually measure the bode response to insure that the loop compensation is adequate.

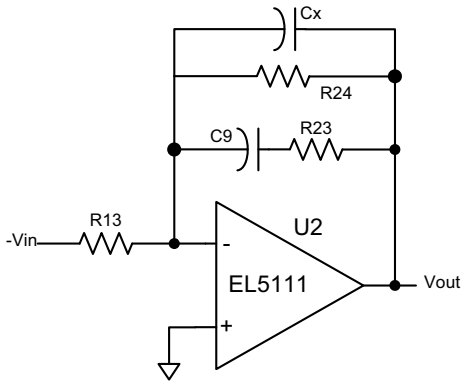
Error amplifier

$$R3 := 18\cdot 10^{3}$$
$$R4 := 649$$
$$R5 := 2.15\cdot 10^{3}$$
$$Rx := 0$$
$$Cx := 100\cdot 10^{-12}$$
$$X_{error.Amp}(s) := \frac{H1_{U1}(s,R3,R4,R5,Rx,Cx)\cdot G_{LMV431}(s)}{1 - H2_{U1}(s,R3,R4,R5,Rx,Cx)\cdot G_{LMV431}(s)}$$



Compensation amplifier

$$R23 := 5000$$
$$R13 := 5000$$
$$R24 := 5000$$
$$C9 := 1\times 10^{-6}$$
$$Cx := 1\cdot 10^{-126}$$
$$X_{Comp.Amp}(s) := \frac{-\left(H1_{U2}(s,R13,R24,R23,C9,Cx)\cdot G_{5111}(s)\right)}{1 - H2_{U2}(s,R13,R24,R23,C9,Cx)\cdot G_{5111}(s)}$$



Equivalent AC Model of the Compensation Amp

PWM Current Mode Stage

$R14 := 10000$

$R11 := 499$

$R1\_2 := \frac{30.9}{2}$

$N_{ct} := 50$

$N_t := 13$

Output parameters

$C_{out} := 8800 \cdot 10^{-6}$

$R_{esr} := .020$

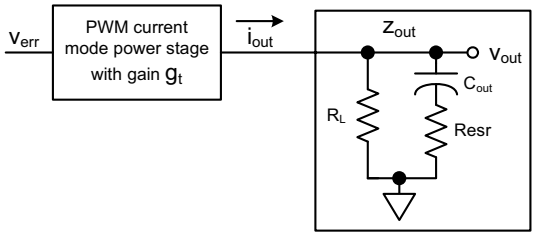
$V_{out} := 12$

$I_{out.min} := .011$

$I_{out.max} := 66$

$R_{L\_min} := V_{out} \cdot I_{out.min}^{-1}$

$R_{L\_max} := V_{out} \cdot I_{out.max}^{-1}$



$$g_t := \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R11 + R14 + R1\_2)}{(R14 \cdot R1\_2)} = 29.49$$

$$X_{pwm.RLmin}(s) := \frac{g_t}{\left(\frac{s}{Freq \cdot \pi} + 1\right) \cdot \left[R_{L\_min}^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s}\right)^{-1}\right]}$$

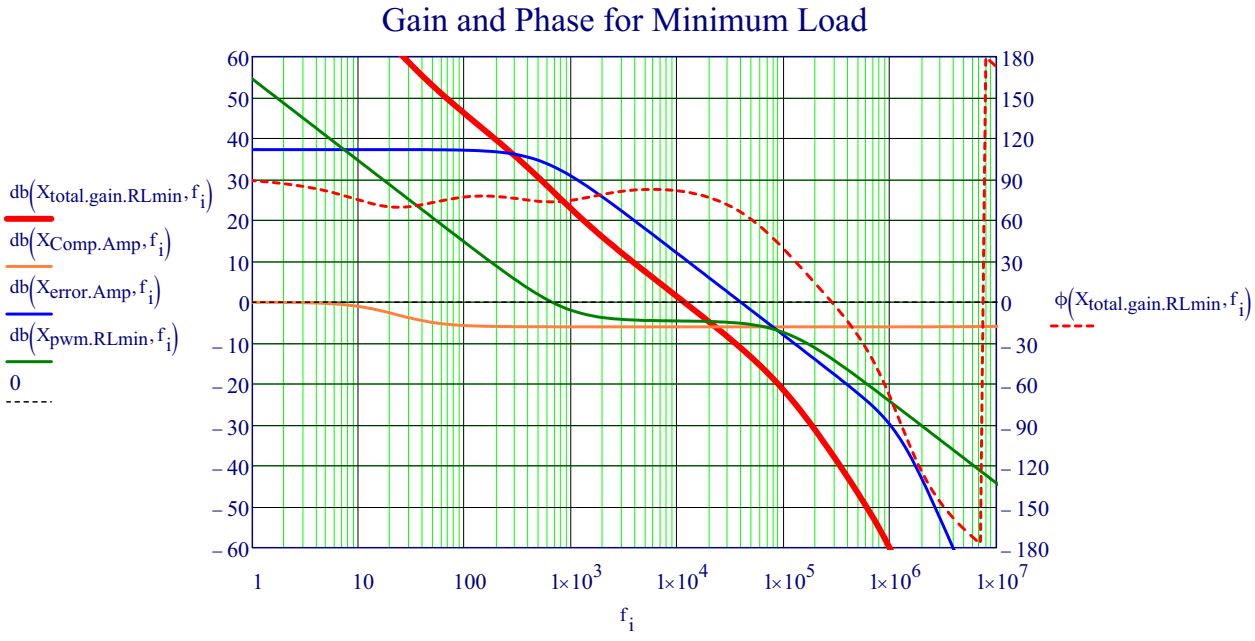
$X_{pwm.RLmin}$ Gain function for min load

$$X_{pwm.RLmax}(s) := \frac{g_t}{\left(\frac{s}{Freq \cdot \pi} + 1\right) \times \left[R_{L\_max}^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s}\right)^{-1}\right]}$$

$X_{pwm.RLmax}$ Gain function for max load

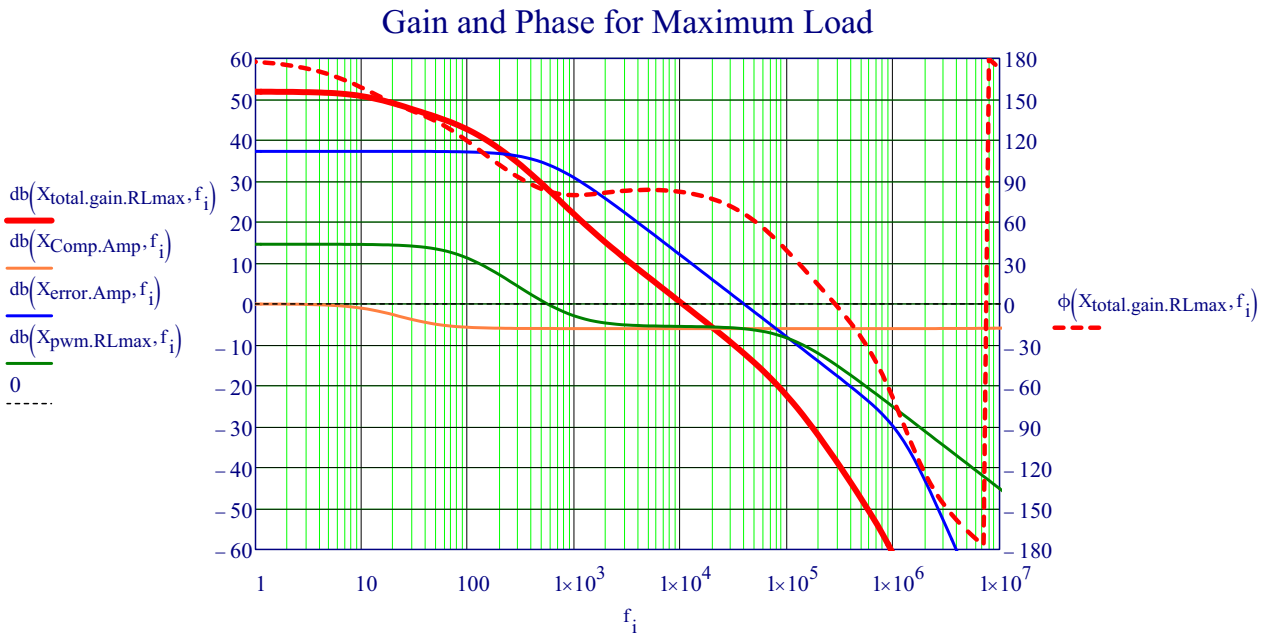
$X_{total.gain.RLmin}(s) := X_{error.Amp}(s) \times X_{Comp.Amp}(s) \cdot X_{pwm.RLmin}(s)$

$X_{total.gain.RLmax}(s) := X_{error.Amp}(s) \cdot X_{Comp.Amp}(s) \cdot X_{pwm.RLmax}(s)$



$f_{UnityGain}(X_{total.gain.RLmin}) = 11557$

$\phi_{margin}(X_{total.gain.RLmin}) = 81$



$f_{UnityGain}(X_{total.gain.RLmax}) = 10428$ $\phi_{margin}(X_{total.gain.RLmax}) = 82$

Load Regulation

As can be seen in the above bode plots, the low frequency closed loop gains at minimum load and maximum load varies significantly primarily because of the change in gain of the PWM output stage. The consequence is that the output voltage will droop as the load increases from minimum to maximum. This droop is relatively large in this design example because the gain of the LMV431 error amplifier is relatively low (especially when compared to the EL5111).

$V_{ref} := 1.24V$ The reference voltage of the LMV431

$V_{out} := 12V$ The output voltage of the ISL6754EVAL board

$R5 := 2.15K\Omega$

$R3\_4 := 18.649K\Omega$ R3_4 is the sum of R3 and R4

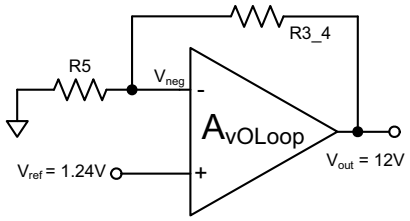
1) $(V_{ref} - V_{neg}) \cdot A_{VOLoop} = V_{out}$ Where A_{vOLoop} is the open loop gain including all of the gain elements (LMV431, EL5111, and PWM output).

also

2) $V_{neg} := \frac{R5}{R5 + R3\_4} \cdot V_{out}$

substituting 2) into 1):

$$\left(V_{ref} - \frac{R5 \cdot V_{out}}{R5 + R3\_4}\right) \cdot A_{VOLoop} = V_{out}$$



Equivalent DC Model of the Closed Loop

solving for Vout and converting to a function:

$$Vout(A_{VOLoop}) := \frac{V_{ref}}{\frac{R5}{R5 + R3\_4} + \frac{1}{A_{VOLoop}}}$$

Because the Xtotal.gain includes the degenerative gain of the voltage scaling resistors R3_4 and R5, we must exclude this gain stage from this load regulation analysis.

$Vout\left(V_{db2V}\left(db\left(G_{LMV431}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmin}, f_0\right)\right)\right) = 11.9957 \cdot V$ This is the DC output voltage when $I_{out.min} = 0.011$

$Vout\left(V_{db2V}\left(db\left(G_{LMV431}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmax}, f_0\right)\right)\right) = 11.9652 \cdot V$ This is the DC output voltage when $I_{out.max} = 66$

Load regulation:

$$LoadReg_{LMV431} := \frac{Vout\left(V_{db2V}\left(db\left(G_{LMV431}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmax}, f_0\right)\right)\right)}{Vout\left(V_{db2V}\left(db\left(G_{LMV431}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmin}, f_0\right)\right)\right)} = 99.746 \cdot \%$$

If an EL5111 is substituted for the LMV431 as the error amplifier, additional gain is added to the open loop gain which improves the load regulation:

$db\left(G_{LMV431}, f_0\right) = 57$ Low Frequency gain of the LMV431

$db\left(G_{5111}, f_0\right) = 68$ Low Frequency gain of the EL5111

$Vout\left(V_{db2V}\left(db\left(G_{5111}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmin}, f_0\right)\right)\right) = 11.9957 \cdot V$ This is the DC output voltage when $I_{out.min} = 0.011$

$Vout\left(V_{db2V}\left(db\left(G_{5111}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmax}, f_0\right)\right)\right) = 11.9871 \cdot V$ This is the improved DC output voltage when $I_{out.max} = 66$

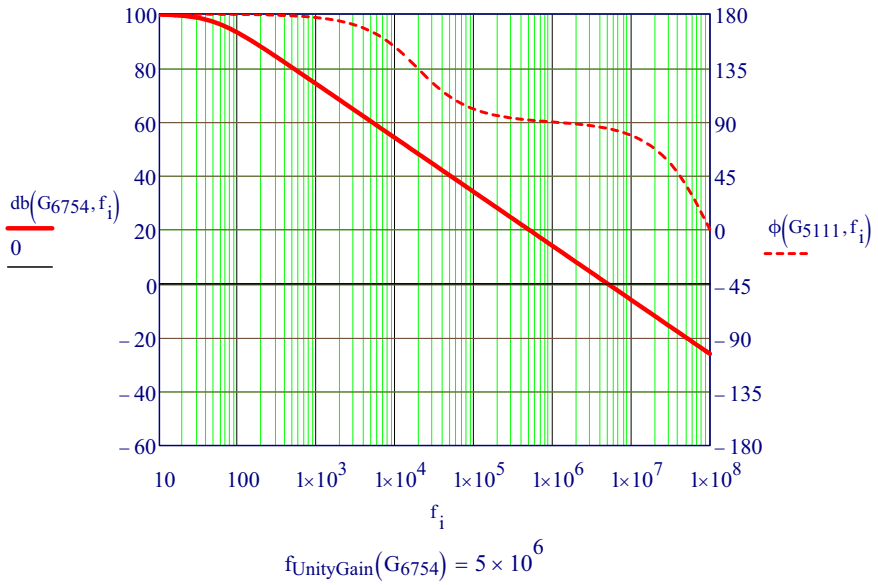
$$LoadReg_{EL5111} := \frac{Vout\left(V_{db2V}\left(db\left(G_{5111}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmax}, f_0\right)\right)\right)}{Vout\left(V_{db2V}\left(db\left(G_{5111}, f_0\right) + db\left(X_{Comp.Amp}, f_0\right) + db\left(X_{pwm.RLmin}, f_0\right)\right)\right)} = 99.928 \cdot \%$$

Step 7) Compensation of the Current Error Amplifier

Open Loop Gain of the ISL6754 Internal Amplifier

$$G_{6754}(s) := \frac{-V_{db2V}(100)}{\left(\frac{s}{50 \cdot 2 \cdot \pi} + 1\right)}$$

The GBWP of the internal amplifier is specified as 5MHz. Although, the maximum gain a low frequencies is not specified, for the purpose of this analysis, the max gain is assumed to be 100db.



$f_{UnityGain}\left(G_{6754}\right) = 5 \times 10^6$

Gain of the Current Error Amplifier

The scaling factor for current sensing (From step 4)

R25 := 22100 R26 := 6650

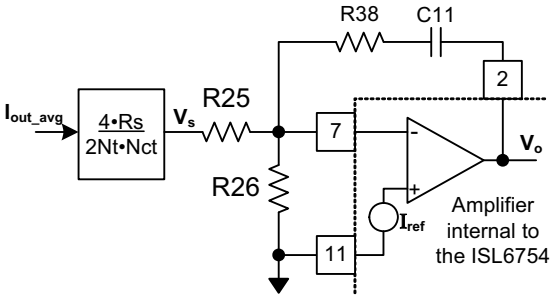
$$V_S := I_{out\_avg} \cdot \left(\frac{4R1\_2}{2 \cdot N_t \cdot N_{ct}}\right)$$

For an Inverting Opamp the gain function, X(s), can be simplified to:

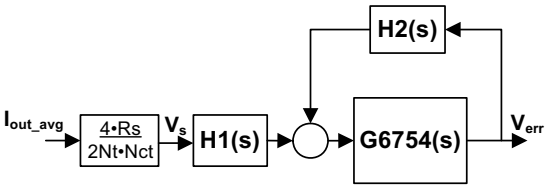
$$X_{Ierror.Amp}(s) = \frac{V_o}{I_{out\_avg}} = \frac{H1(s)\cdot G_{6754}(s)}{1 - H2(s)\cdot G_{6754}(s)}\cdot\left(\frac{4R_s}{2\cdot N_t\cdot N_{ct}}\right)$$

$$H1_{U1}(s,R25,R26,R38,C11) := \frac{\left[\left(\frac{1}{C11\cdot s} + R38\right)^{-1} + \frac{1}{R26}\right]^{-1}}{\left[\left(\frac{1}{C11\cdot s} + R38\right)^{-1} + \frac{1}{R26}\right]^{-1} + (R25)}$$

$$H2_{U1}(s,R25,R26,R38,C11) := \frac{\left[\frac{1}{(R25)} + \frac{1}{R26}\right]^{-1}}{\left[\frac{1}{(R25)} + \frac{1}{R26}\right]^{-1} + \left[\left(\frac{1}{C11\cdot s} + R38\right)^{-1}\right]^{-1}}$$



These values are used to compensate the current regulation closed loop.



gain block diagram for the Current error amplifier

$C11 := .01\cdot 10^{-6}$ $R38 := 0$

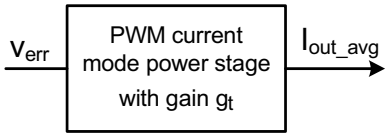
$$X_{Ierror.Amp}(s) := \frac{H1_{U1}(s,R25,R26,R38,C11)\cdot G_{6754}(s)}{1 - H2_{U1}(s,R25,R26,R38,C11)\cdot G_{6754}(s)}\cdot\left(\frac{4\times 100}{2\cdot N_t\cdot N_{ct}}\right)$$

Gain of the PWM Current Mode Power Stage

From step 5)

$g_t = 29.49$ Low frequency gain (I_{out_avg}/V_{err})

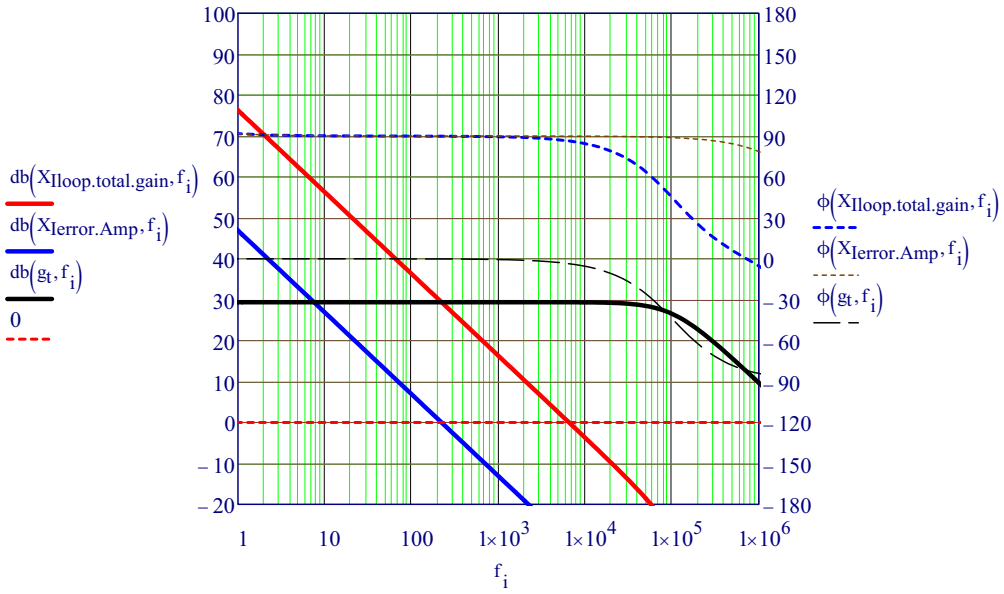
$$g_t(s) := g_t\cdot\left(\frac{s}{\frac{Freq}{2}\cdot 2\cdot\pi} + 1\right)^{-1}$$ with switching frequency pole



Total Current Regulation Loop Gain

$C11 = 10\times 10^{-9}$ $R38 = 0$

$X_{Iloop.total.gain}(s) := X_{Ierror.Amp}(s)\cdot g_t(s)$



$f_{UnityGain}(X_{Iloop.total.gain}) = 6518$ $\phi_{margin}(X_{Iloop.total.gain}) = 86$

ISL6754DBEVAL1Z Schematic

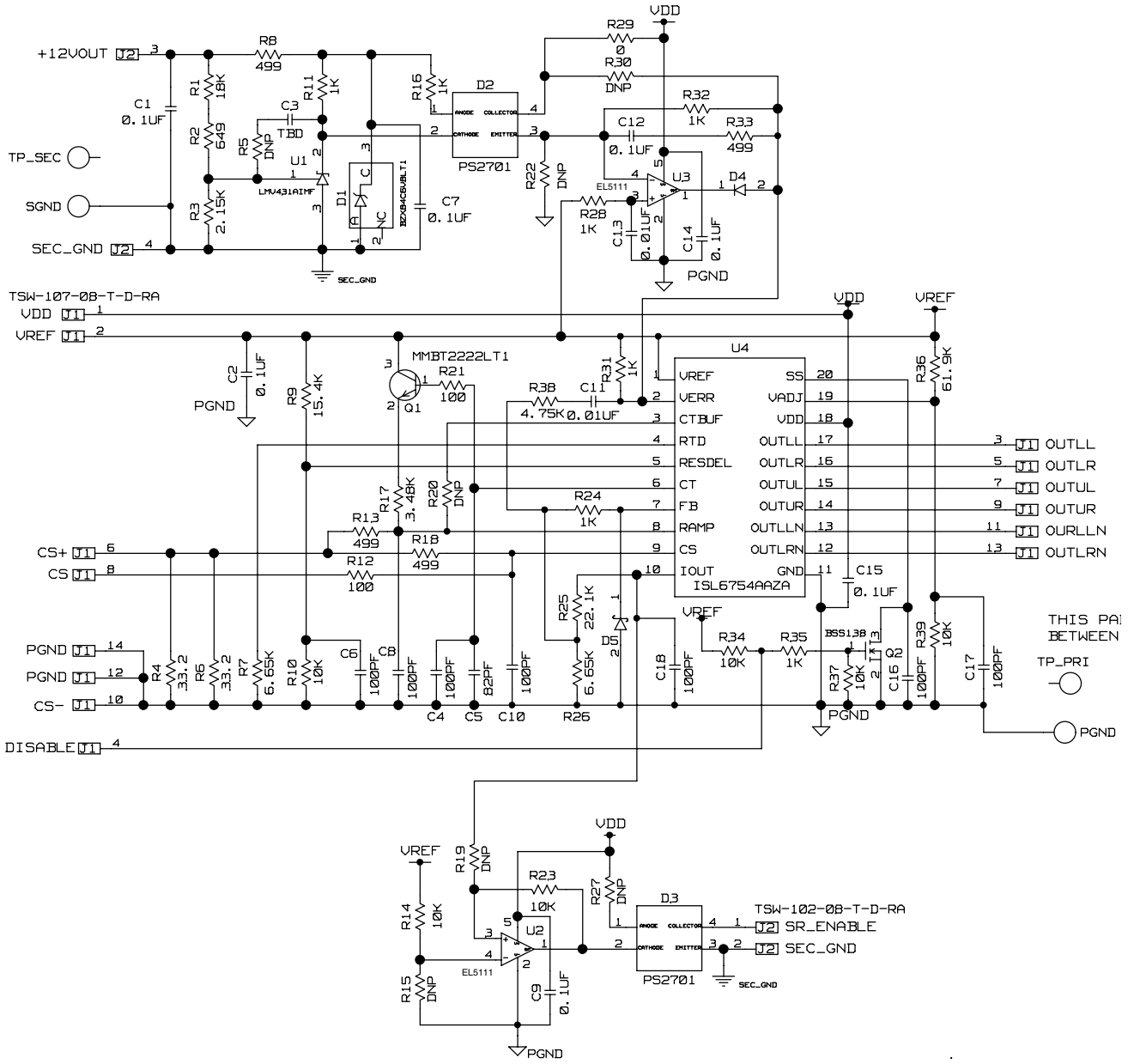


FIGURE 3. ISL6754 CONTROL CARD SCHEMATIC

ISL6752DBEVAL1Z Schematic

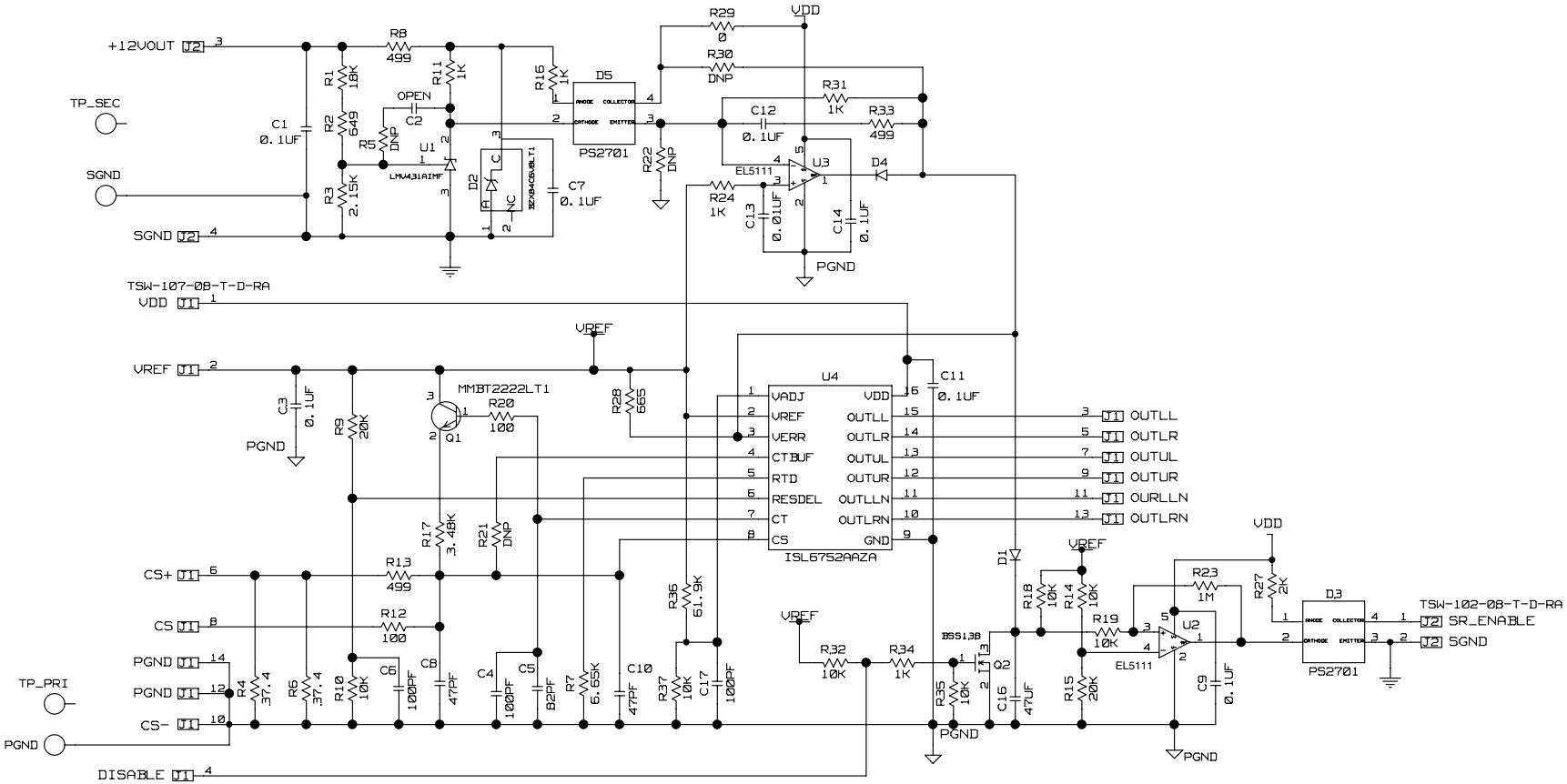


FIGURE 4. ISL6752 CONTROL CARD SCHEMATIC

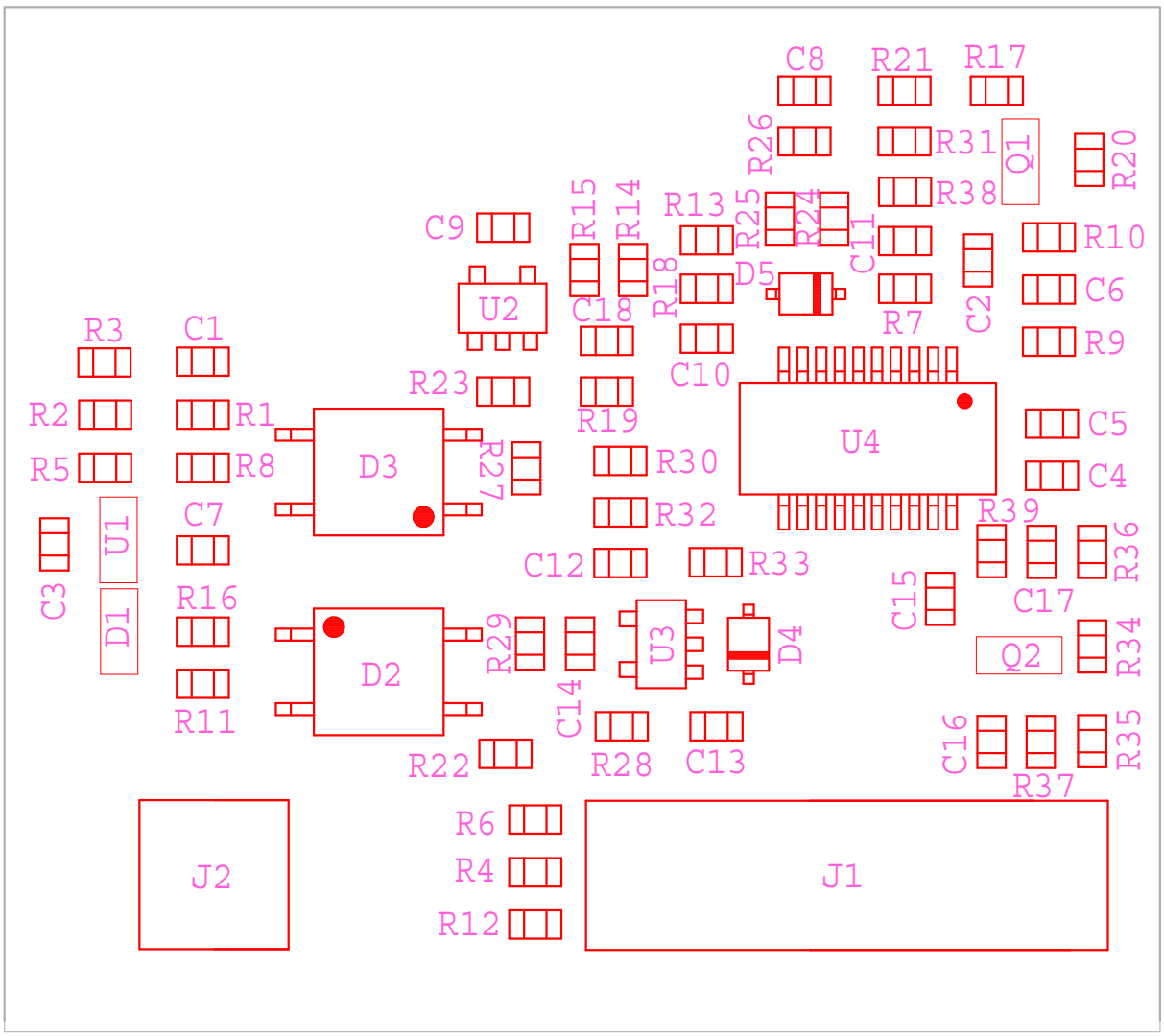


FIGURE 5. ISL6754 CONTROL CARD TOP ASSEMBLY

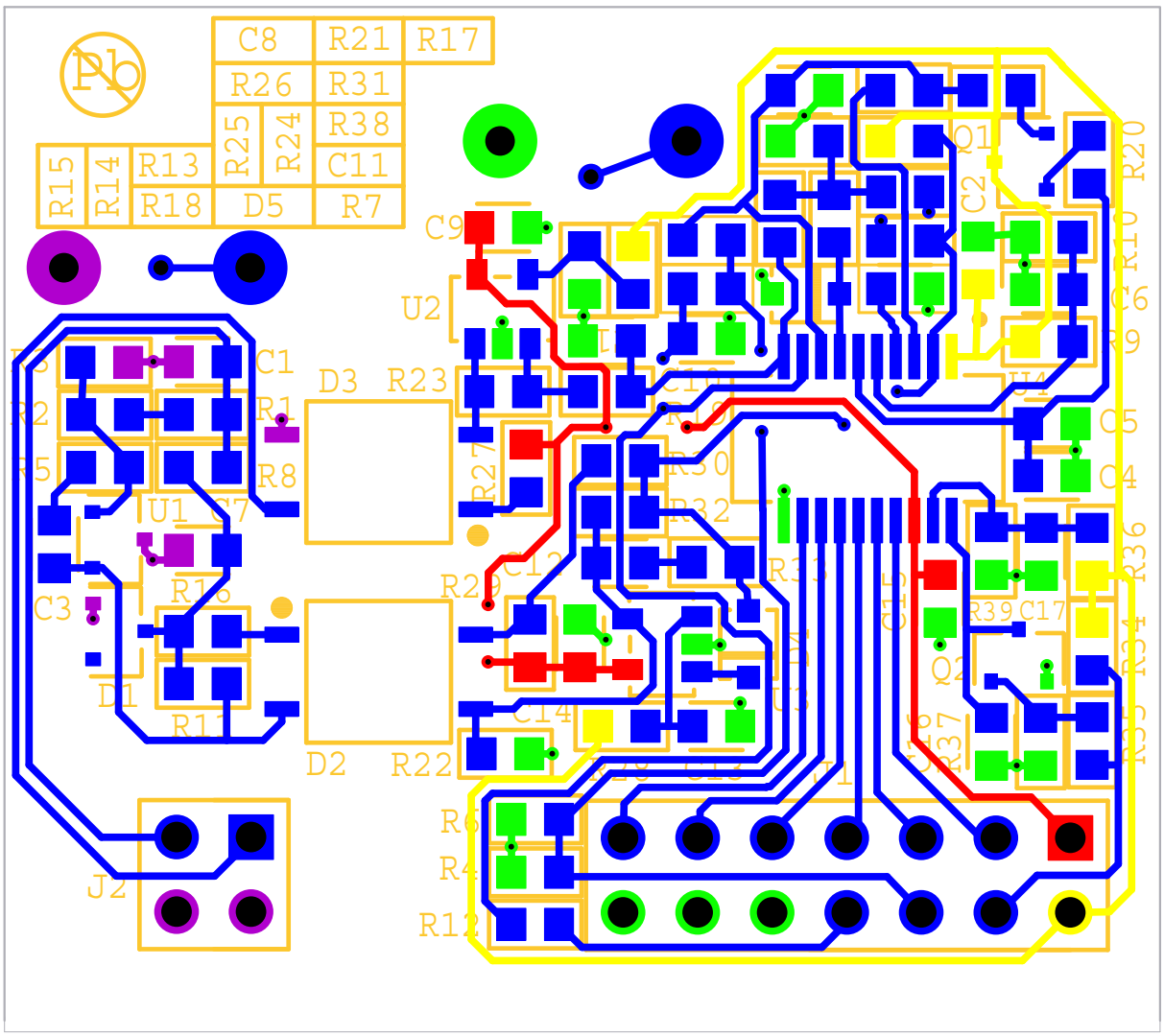


FIGURE 6. ISL6754 CONTROL CARD TOP LAYER

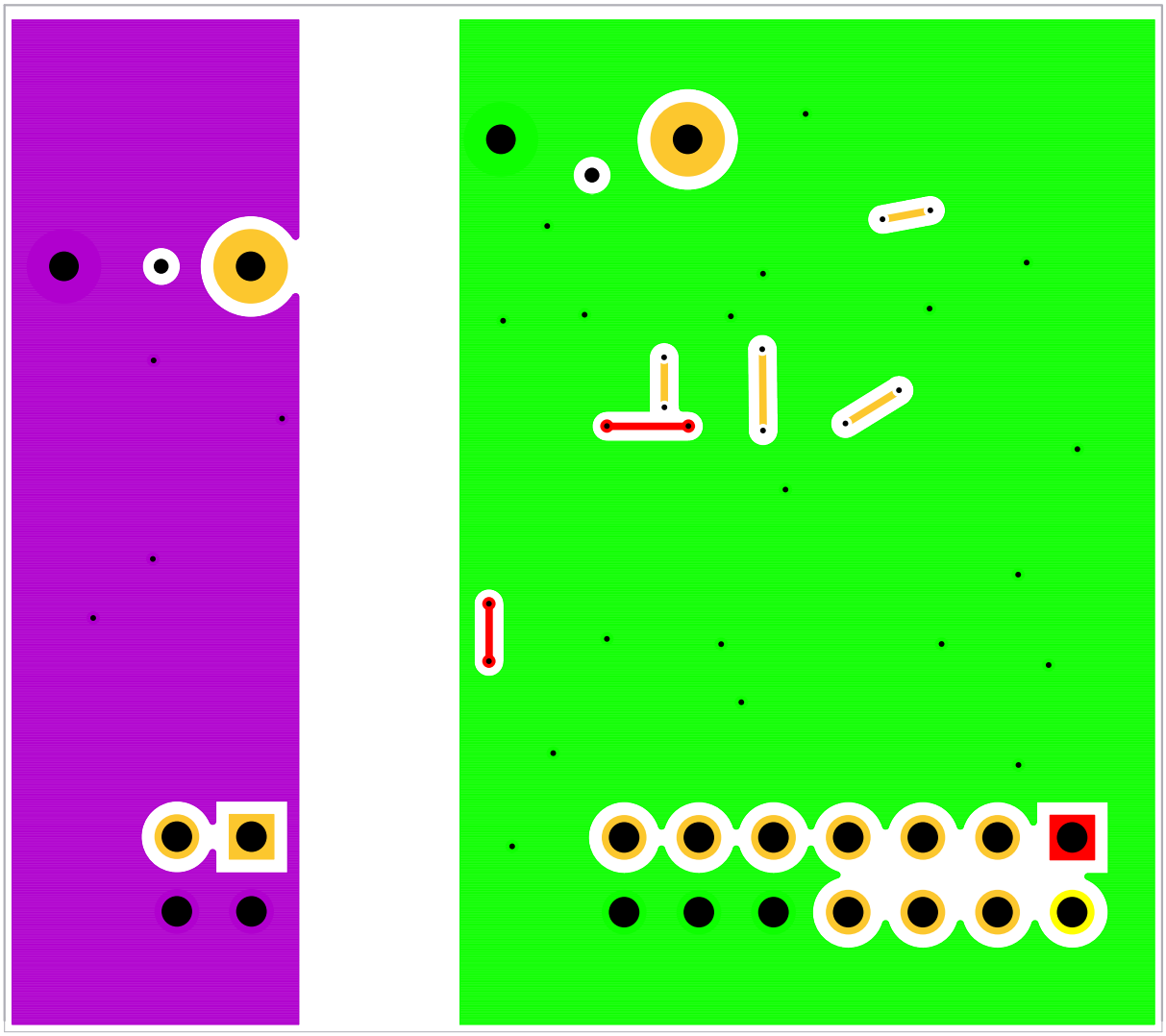


FIGURE 7. ISL6754 CONTROL CARD BOTTOM LAYER

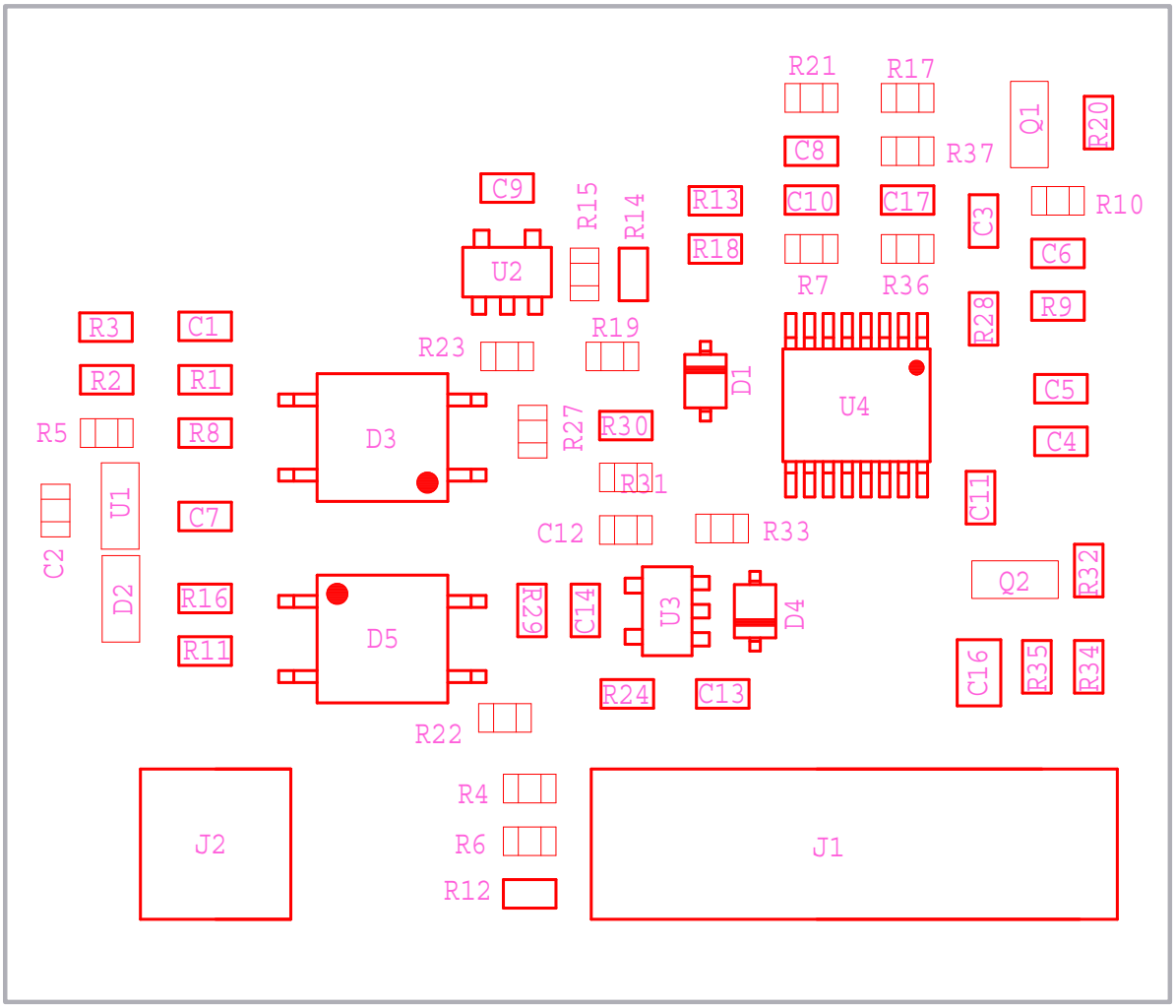


FIGURE 8. ISL6752 CONTROL CARD TOP ASSEMBLY

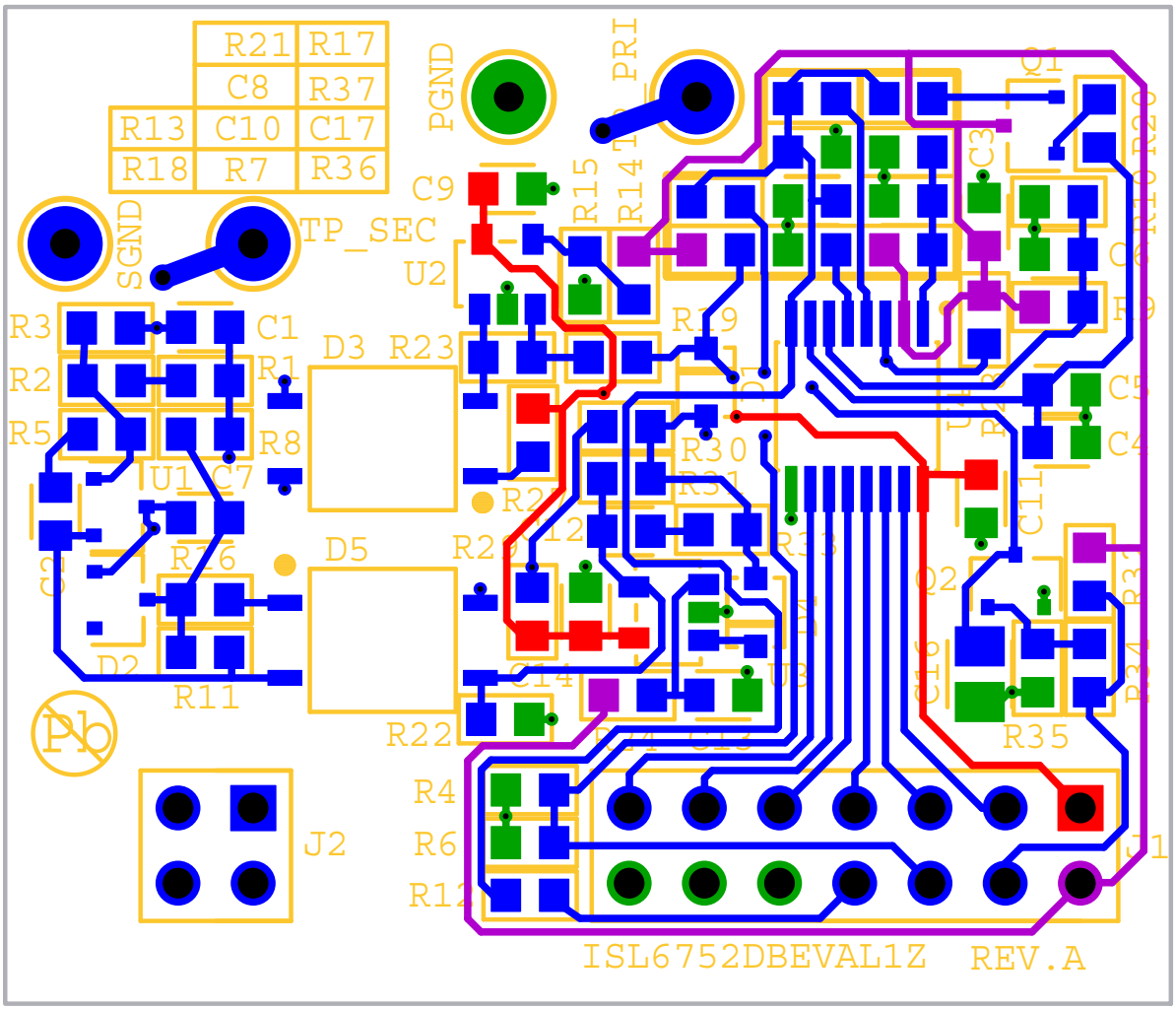


FIGURE 9. ISL6752 CONTROL CARD TOP LAYER

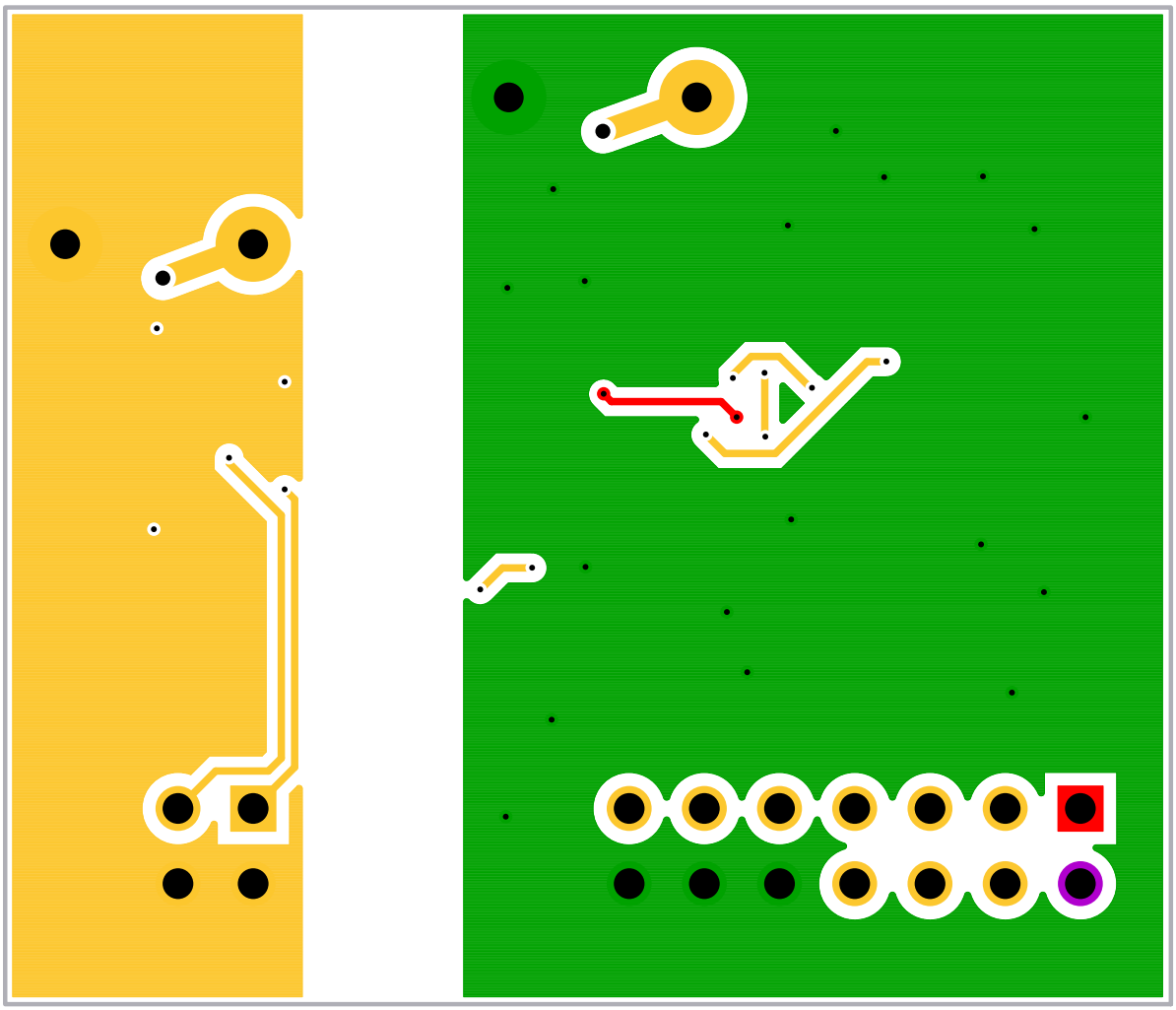


FIGURE 10. ISL6752 CONTROL CARD BOTTOM LAYER

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