Making Accurate Voltage Noise and Current Noise Measurements on Operational Amplifiers Down to 0.1Hz

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Abstract

Making accurate voltage and current noise measurements on op amps in the nV and fA range can be challenging. This problem is often addressed by two different approaches. Both approaches concentrate on reducing the noise of the amplifiers used to measure the Device Under Test (DUT). The first approach uses conventional cross-correlation techniques to remove un-correlated noise and a procedure to remove the correlated noise contributions made by the amplifiers used to measure the DUT [1]. The second approach, and the subject of this Application Note, consists of designing a test platform with an effective background noise at least 10dB lower than the DUT.

To obtain a test platform with this level of performance requires: the removal of environmental electrical disturbances, the use of batteries for low noise voltage sources, the use of a Post Amplifier (PA) to raise the DUT noise above the measurement system's noise floor, control software to measure accurate noise data down to 0.1Hz and processing software to eliminate external noise and generate the DUT's voltage (e_n) and current (i_n) noise plots.

This Application Note will discuss the procedures used to obtain a test platform that is capable of measuring nV and fA down to 0.1Hz. The test platform's capability is illustrated by measuring the voltage and current noise of Intersil's ISL28190 (Bipolar inputs, 1nV/√Hz) operational amplifier and Intersil's ISL28148 (MOS inputs, 16fA/√Hz) operational amplifier.

Introduction

To measure an accurate internal noise of an Op Amp, for a data sheet spec, two types of external noise sources (Environmental and Johnson) must be removed from the measurement. Environmental noise is any unwanted signals arriving as either voltage or current, at any of the amplifiers terminals or surrounding circuitry. It can appear as spikes, steps, sign waves or random noise. This noise can come from anywhere: nearby machinery, power lines, RF transmitters, lab power supplies or lab computers. The Environmental noise is minimized by isolating the DUT in a Faraday cage and powering the DUT with batteries.

The second external noise source is Johnson noise. Johnson noise is the noise generated by the external biasing and gain setting resistors of the DUT and test platform. Johnson noise is subtracted out from the total noise measurement through processing software so only the internal noise of the DUT is reported.

This Application Note will:

1. Discuss basic noise equations (external and internal) and then use these equations to extract the DUT noise from our test platform's noise.
2. Discuss the use of a Post Amplifier (PA) to lower our HP35670A Dynamic Signal Analyzer's (DSA) effective noise floor from 20nV/√Hz to 3nV/√Hz.
3. Illustrate the effectiveness of our Faraday cage to remove environmental noise.
4. Discuss AC coupling of DUT, PA and DSA.
5. Determine the required gain of the DUT to enable the test platform to measure voltage noise below 3nV/√Hz.
6. Discuss considerations for choosing the optimum series resistor R_S to measure current noise.
7. Discuss the Test Platform Algorithm.
8. Present conclusions.

Basic Equations For Calculating Noise

Johnson noise is the only resistive noise source considered in this controlled lab study. Other resistive noise sources such as contact noise, shot noise and parasitics associated with particular types of resistors could also contribute noise in an application.

A typical figure of merit for amplifier noise is noise density. Voltage-noise density is specified in nV/√Hz, while current-noise density is usually in units of pA/√Hz [2]. For simplicity, these measurements are referred to the amplifier inputs; thus removing the need to account for the amplifiers gain.

External Johnson Noise

At temperatures above absolute zero, all resistances generate Johnson noise due to the thermal movement of charge carriers. This noise increases with resistance, temperature and bandwidth. The voltage and current noise are given by Equations 1 and 2, respectively [3, 4, 5].

External Johnson Voltage Noise

$$V_n = e_n = \sqrt{4kTBR} \quad \text{(EQ. 1)}$$

External Johnson Current Noise

$$i_n = \sqrt{\frac{4kTB}{R}} \quad \text{(EQ. 2)}$$

Where:

k is Boltzmann's constant (1.38×10^{-23} J/K).

T is the temperature in Kelvin (273.15 + Ambient °C).

R is the resistance (Ω)

B is the bandwidth in Hz.

Note: Bandwidth is 1Hz for all measurements and not shown in all Equations presented in the Application Note.

Internal Noise of the DUT

Figure 1 shows the internal noise of an Op Amp referenced to the amplifiers inputs. Measurements Referenced To the Input are referred to as RTI. To generate this curve, the external noise has been removed from the final values shown along with any gain the measurement circuits may have added. The internal noise of an amplifier has two distinct frequency ranges. At very low frequencies, the noise amplitude is inversely proportional to frequency and is referred to as the 1/f noise. At frequencies above the corner frequency, the noise amplitude is essentially flat.

Equation 3 is used to calculate the total noise voltage Referenced To the Output (RTO) for the basic Op Amp in Figure 2.

$$e_t = \sqrt{e_n^2 + (R_S \times i_n)^2 + (R_1 \| R_2 \times i_n)^2 + 4kT(R_S + R_1 \| R_2)} \times A_V \quad \text{(EQ. 3)}$$

Where:

e_t = Total voltage noise RTO at a given frequency.

e_n = RTI voltage-noise of DUT at a given frequency.

$R_1 \| R_2 = R_1R_2/(R_1 + R_2)]\Omega$

i_n = RTI current-noise of the DUT at a given frequency.

k = Boltzmann's constant (1.38×10^{-23} J/K).

T = Ambient temp in Kelvin (273.15 + Ambient °C).

A_V = Gain of Op Amp ($1 + R_1/R_2$).

Procedure to Improve the DSA's Effective Noise Floor

Figure 3 shows the noise floor of the HP35670A DSA measured with the input grounded. From this graph, the minimum noise floor is around 20nV/√Hz. A technique to improve the measurement noise floor of the test platform is to add a Post Amplifier to gain the noise being measured above the noise floor of the DSA. Figure 4 shows the final test platform schematic which includes the DSA, HA-5147 PA, DUT and the AC coupling of the DUT offset and the PA offset voltage. Note: the HA-5147 was cherry picked for its low (11nV/√Hz at 0.1Hz) 1/f noise performance.

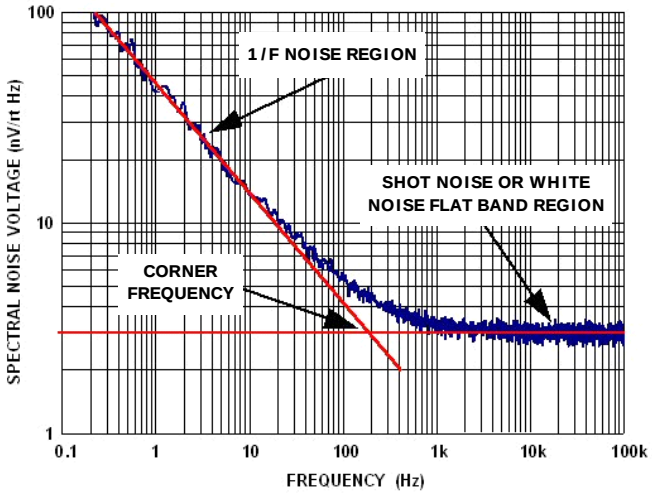

FIGURE 1. AMPLIFIER INTERNAL VOLTAGE NOISE (RTI) vs FREQUENCY

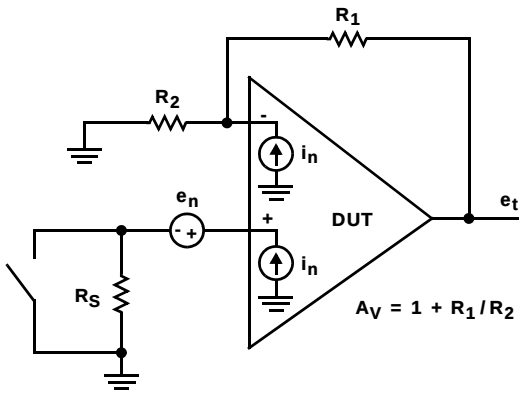

FIGURE 2. OP AMP NOISE MODEL

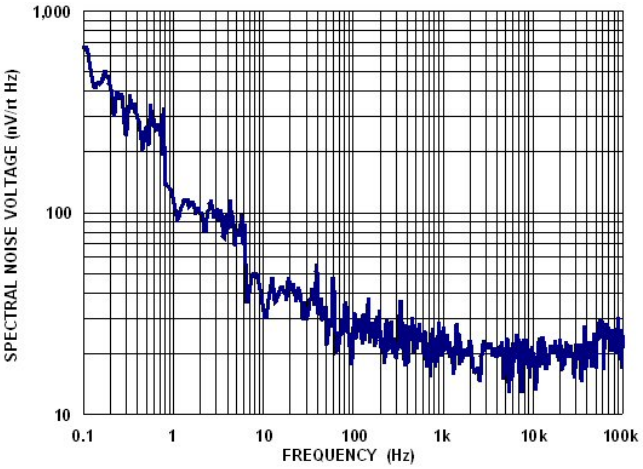

FIGURE 3. NOISE FLOOR OF THE HP35670A DYNAMIC SIGNAL ANALYZER

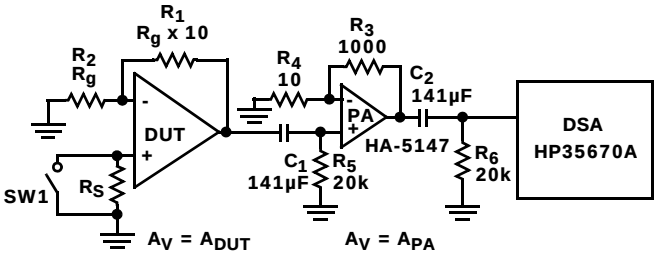

FIGURE 4. COMPLETE LOW NOISE TEST PLATFORM SCHEMATIC

The minimum gain of the PA is the gain that overcomes the noise floor of the DSA down to 0.1Hz frequency. Figure 5 shows the noise floor of the HP35670A DSA (pink curve), the RTO noise voltage of the PA with the gain set to 26 (blue curve), and the RTO noise voltage of the PA with the gain set to 101 (green curve). Notice that the gain of 26 is not enough and the PA's RTO noise voltage is swamped out by the DSA's noise floor for frequencies less than 10Hz. Setting the PA's gain to 101 is enough to overcome the DSA noise floor by 20dB at 1kHz and 3.3 dB at 0.1Hz.

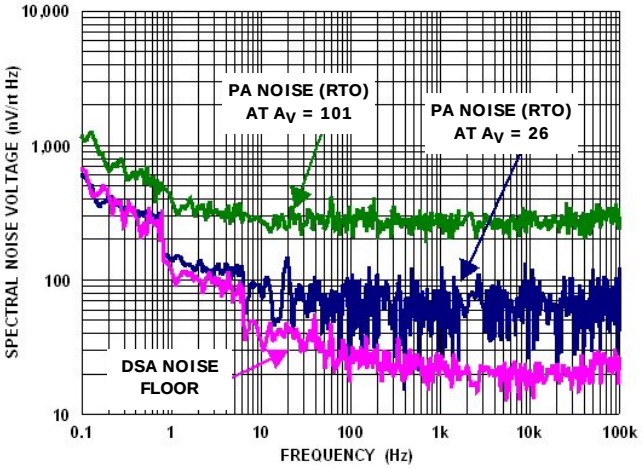

FIGURE 5. SETTING THE GAIN OF THE POST AMPLIFIER TO OVERCOME THE RTO DSA NOISE FLOOR

Figure 6 shows the RTI noise voltage of our PA set to a gain of 101 (green trace) and the original DSA noise floor (pink trace) repeated for comparison purposes. By referencing the PA noise to the input, (dividing by A_V = 101) we are now able to effectively measure a flat band RTI noise of 3nV/√Hz, which is the noise floor of our HA-5147.

Faraday Cage to Remove Environmental Noise

Figure 7 shows the result of testing an HA-5147 (A_V = 101) inside and outside our Faraday cage. The Faraday cage enables us to maintain a noise floor of 3nV/√Hz over an additional decade of frequency in the flat band region. For frequencies below 100Hz, the improvement in the noise floor is critical in making noise measurements down to 0.1Hz. For frequencies above 100Hz, environmental noise was not a factor for our given lab conditions.

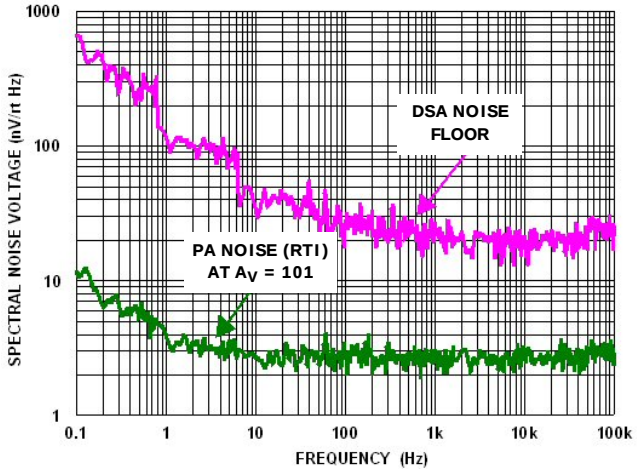

FIGURE 6. EFFECTIVE RTI 3nV/√Hz NOISE FLOOR OF THE PA AND DSA

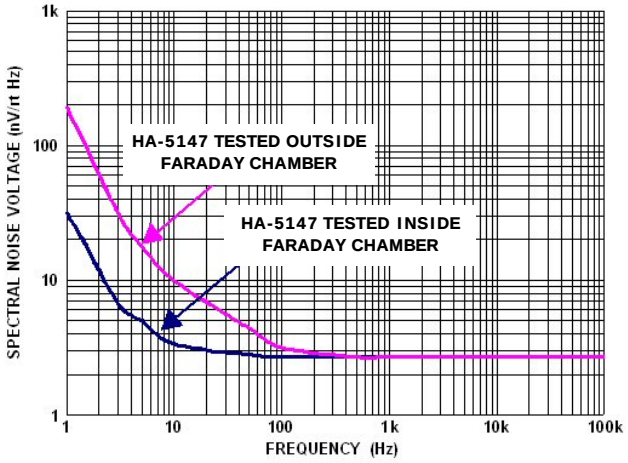

FIGURE 7. EFFECTS OF FARADAY CAGE ON LOW FREQUENCY ENVIRONMENTAL NOISE

AC Coupling of the Post Amp and the DUT

The output of the PA and DUT need to be AC coupled to avoid over-driving the DSA's input or railing the output of the PA, as a result of the DC offset caused by VOS and Ib (reference Figure 4). The subsequent measurements were performed on the PA and DSA to minimize any errors before measuring any noise on the DUT.

Initially, the test platform used the internal AC coupling of the HP35670A DSA. Test results at frequencies below 10Hz were artificially low, when compared to the expected results for HA-5147 at 1Hz. The cause of the error was determined to be the internal AC coupling circuitry of our DSA. Figure 8 shows the effective roll-off in gain of the DSA's internal AC coupling circuit (red trace) compared to the roll-off in gain when using an external AC coupling

circuit (blue trace). The curves were generated by taking 3 measurements, with the goal of detecting amplitude loss. The input signal was a $2mV_{P-P}$ sine wave. The 1st measurement was with the DSA DC coupled to get the base line. The 2nd was measured using the DSA's internal AC coupling and the 3rd was with an external AC coupling. The AC loss was determined by the ratio of the AC amplitude to the DC amplitude (normalized to zero).

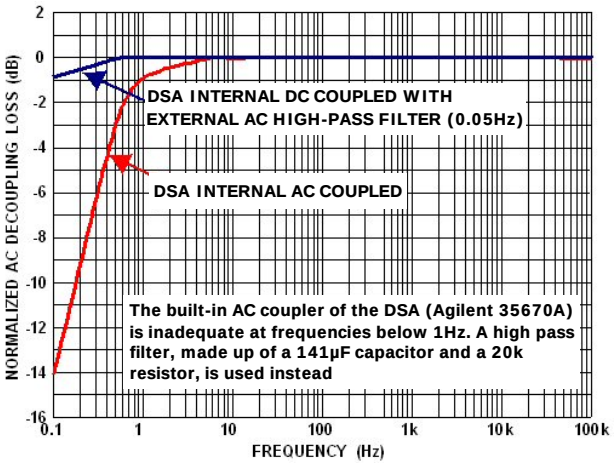

FIGURE 8. EFFECT OF DSA's INTERNAL AC COUPLING vs EXTERNAL AC COUPLING ON THE PA's LOW FREQUENCY GAIN

The results show the gain of the signal cannot be considered constant for frequencies below 10Hz when AC coupled via the DSA or 0.5Hz when externally AC coupled with the C_2 and R_6 in Figure 4. This error in gain accounted for the lower than expected calculated noise. The final solution was to go with the external AC coupling (DSA DC coupled) and account for the drop in the gain by performing gain measurements for each frequency of the PA across the entire frequency range. Through software, the individual gain values were subsequently used in the calculation for the RTI current and voltage noise of the DUT for each frequency plotted in the curve.

Figure 9 shows the final optimized noise floor of the PA-DSA (blue trace) and the effect of the RC time constant of the external AC coupling circuit (pink trace). Because of the long RC time constant of the external filter (20kΩ and 141µF) we need to allow time for the coupling circuit to settle out before starting to test. The pink curve is the noise measurement of the HA-5147 1 minute after power is applied to the PA. The blue trace is the same measurement after waiting 30 minutes for the circuit to settle out.

Determining the Required Gain of the DUT

The optimized noise floor of the PA-DSA is 100nV/√Hz at 0.1Hz and 3nV/√Hz in the flat-band range (Figure 9). Measuring the noise of an amplifier like the ISL28190 (Bipolar inputs, 1nV/√Hz), is achieved by gaining up the output of the DUT by 10. This will lower the effective noise floor in the flat band range to 0.3nV/√Hz, which meets our requirement of 10dB greater than the system's noise floor. Before committing to running the full battery of sweeps to average out the readings, we first run a single sweep (SW1, Figure 4 closed) to verify the 1/f noise is not being swamped out by the 100nV/√Hz noise floor of the test platform at 0.1Hz. If so, then the gain of the DUT needs to be increased to insure the measurement is not that of the test system's noise floor.

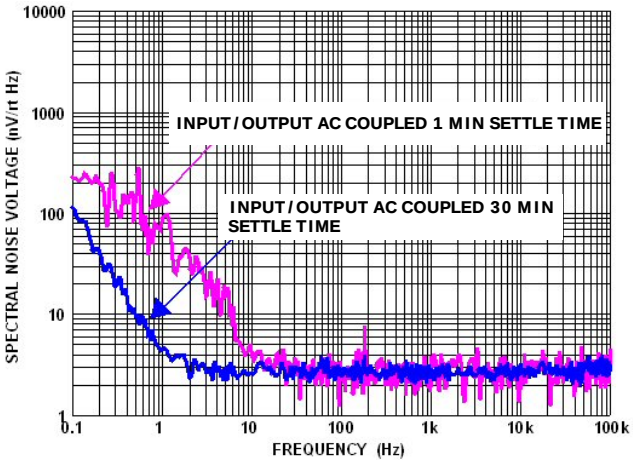

FIGURE 9. EFFECTIVE RTI NOISE FLOOR OF THE PA-DSA WITH EXTERNAL AC COUPLING

Considerations for Choosing the Series Resistor to Measure the Current Noise

The goal of selecting the value for R_S is to make it as large as possible to raise the DUT's input current noise (dropped across R_S) above the background and R_S voltage noise, all without driving the DUT's output voltage into the rails or limiting the noise bandwidth of the amplifier. Reference the section titled "Measurement Algorithm" for the details of the process to measure current noise and then voltage noise of the DUT.

Figure 10 illustrates the voltage noise power relationship between the $4kTR_S$ and the product of $R_S^2 i_n^2$ (reference Equations 4 and 5).

Johnson Voltage Noise of R_S:

$$V_n = \sqrt{4kTR_S} \rightarrow V_n^2 = 4kTR_S \quad \text{(EQ. 4)}$$

Johnson Current Noise contribution of R_S:

$$V_n^2 = R_S^2 i_n^2 \quad \text{(EQ. 5)}$$

Figure 10 can be used as a tool for selecting the value of the R_S resistor. The almost diagonal curve in Figure 10 is the $4kTR_S$ Johnson noise. The other parallel lines are the (R_S^2 I_n^2) current noise contributions. A good starting point is to choose a value of R_S that results in the current noise contribution being larger than the Johnson noise contribution.

Notice in Figure 10, that the current noise contribution ($R_S^2\ I_n^2$) is very small at low resistances in comparison with the dominant $4kTR_S$ noise. At higher values of R_S, the squared function of the noise current quickly makes it the dominant noise source.

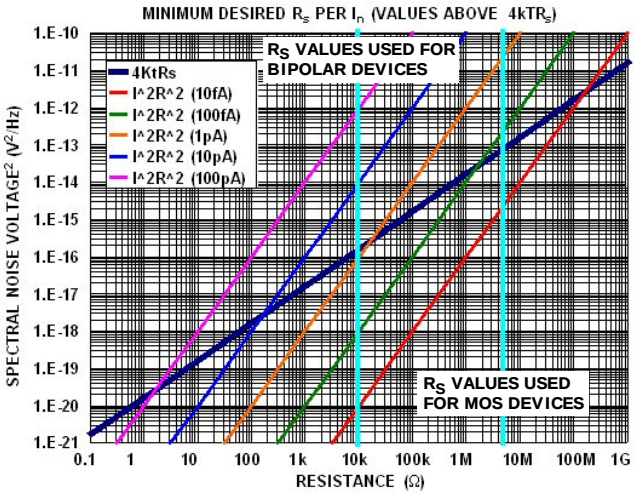

FIGURE 10. TOOL FOR SELECTING R_S RESISTANCE VALUE

At some point the product $R_S^2\ I_n^2$ magnitude becomes high enough to raise it above background noise and make it a measurable signal. Preferably, the value of R_S should be chosen in a way that $R_S^2\ I_n^2 \geq 4kTR_S$, but that is not always possible. There is an upper limit to the value of R_S upon which leakage resistance degrades accuracy of the measurement. This typically occurs for R_S values greater than 5MΩ. To measure noise currents in the tens of fA requires a large number of averages to smooth out the data. The data presented in this Application Note for the ISL28148 went through the process of averaging each frequency measurement 500 times, then repeating this process 10 times and averaging the corresponding measurements to obtain one value per frequency plotted. The theory of this process is not covered in this Application Note, and is the subject of another Application Note.

Based on empirical results, the value of the R_S resistor depends upon the Bias current (I_b) of the device. For Bipolar input devices with I_b in the µA range, R_S is 10kΩ and 100kΩ for I_b in the pA range. For MOS input devices, R_S is 5MΩ with I_b in the f_A range. The following two graphs further demonstrate the signal to noise improvement in both e_n and i_n as R_S is increased.

Figure 11 shows the spectral voltage noise (e_n) of the DUT (HA-5147, A_V = 1) and PA (HA-5147, A_V = 101) with different values of R_S. The $4kTR_S$ is also plotted to show when the voltage noise level is above the background noise of the $4kTR_S$ value. From this spectrum, the 1kΩ value of R_S cannot resolve voltage noise from the $4kTR_S$, where as the 100kΩ R_S generates very clean and accurate results for voltage noise.

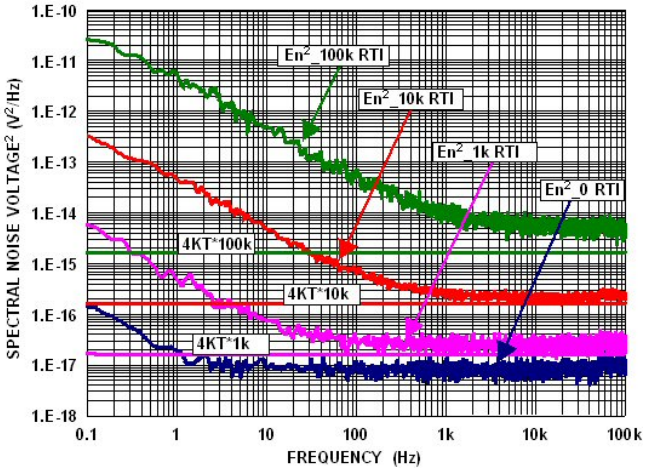

FIGURE 11. SPECTRAL VOLTAGE NOISE DENSITY OF DUT, PA vs R_S vs $4kTR_S$

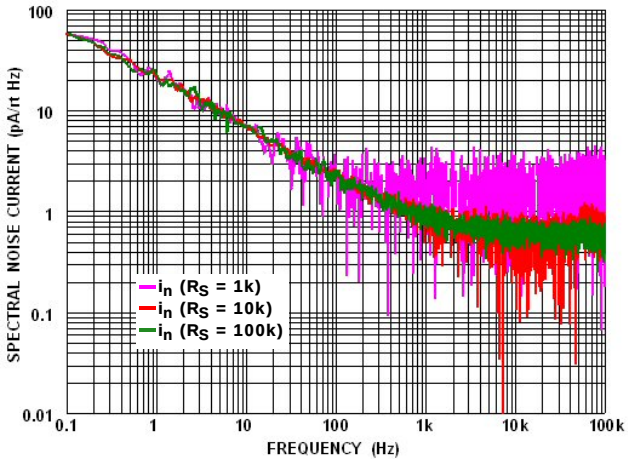

FIGURE 12. SPECTRAL CURRENT NOISE DENSITY OF DUT, PA vs R_S

Figure 12 shows the calculated current noise (i_n) for three different R_S values. The current noise was calculated using Equation 10. From this spectrum, we see the same results as with the voltage noise spectrum in Figure 11. The 1kΩ value of R_S cannot resolve current noise from the $4kTR_S$, where as the 100kΩ R_S generates very clean and accurate results for current noise.

Measurement Algorithm

Now that our Test Platform's noise floor is optimized for our DSA, PA and DUT, it's time to discuss the Test Platform's algorithm. Back in the "Basic Equations For Calculating Noise" section, Equation 3 was used calculate the total noise voltage referenced to the output for the basic Op Amp in Figure 2. The total voltage noise of a basic Op Amp is made up of three components: (A) Internal voltage noise of the DUT, (B) External voltage noise as a result of the current noise through the resistors and (C) External Johnson noise of the resistors. Equation 6 is the same as Equation 3 but with the three components of noise replaced with "A", "B" and "C".

Equation 6 will enable the noise equation, for our test platform with two Op Amps, to be easily displayed and discussed. Let:

A^2 = Voltage noise contribution from DUT $(e_n)^2$

B^2 = Current noise contribution from all resistor $(R_S\ i_n)^2 + (R_1\ ||\ R_2\ i_n)^2$

C^2 = Johnson noise of all the resistors $4kT(R_S + R_1||R_2)$.

Then the total RTO noise (e_t) is:

$$e_t = \sqrt{(A^2 + B^2 + C^2)} \times A_V \quad \text{(EQ. 6)}$$

Equations 7 and 8 calculate the RTO noise voltage for our test platform (Figure 4), with R_S equal to a resistance between 10kΩ to 5MΩ and 0Ω respectively.

$$e_{t(RS)}^2 = [A^2 + B^2 + C^2]A_{DUT}^2 A_{PA}^2 + [A^2 + B^{2!} + C^{2!}]A_{PA}^2 \quad \text{(EQ. 7)}$$

$$e_{t(0)}^2 = [A^2 + B^2 + C^2]A_{DUT}^2 A_{PA}^2 + [A^2 + B^{2!} + C^{2!}]A_{PA}^2 \quad \text{(EQ. 8)}$$

Where:

$e_t^2{}_{(RS)}$ = Is the total RTO noise voltage with R_S = 10kΩ to 5MΩ

$e_t^2{}_{(0)}$ = Is the total RTO noise voltage with R_S = 0Ω

$B^{2!} = (R_3\ ||\ R_4\ i_n)^2$

$C^{2!} = 4kTR_3\ ||\ R_4$

A_{DUT} = Gain of DUT

A_{PA} = Gain of PA

Our procedure for measuring the voltage and current noise is to measure the RTI current noise first, and then use this value in the calculation of the RTI voltage noise. Current noise is measured by converting the DUT's current noise into a voltage noise, via the R_S resistor, which is then amplified and measured by the DSA. Measuring the current noise of an Op Amp is a two step process. The theory is to measure the RTO noise voltage with R_S equal to the value determined in the "Considerations for Choosing the Series Resistor to Measure the Current Noise" section, and then R_S equal to zero. The noise voltage measured with R_S in the circuit is the total noise of the test system plus the noise voltage resulting from the current noise of the DUT. The noise voltage measured with R_S equal to zero is just the total noise voltage of the system. Subtracting these two measured values gives the noise voltage resulting from the current noise of the DUT only. Any noise or errors in gains from the test system are cancelled out.

Equation 9 is the result of subtracting Equation 8 from Equation 7. Solving Equation 9 for the current noise in results in Equation 10. Equation 10 gives the RTI current noise of the DUT.

$$e_{t(RS)}^2 - e_{t(0)}^2 = [R_S^2 i_n^2 + 4kTR_S] \times A_{DUT}^2 A_{PA}^2 \quad \text{(EQ. 9)}$$

$$i_n = \frac{\sqrt{\frac{e_{t(RS)}^2}{A_{DUT}^2 A_{PA}^2} - \frac{e_{t(0)}^2}{A_{DUT}^2 A_{PA}^2} - 4kTR_S}}{R_S} \quad \text{(EQ. 10)}$$

Equation 11 is a modified Equation 8 with the critical noise components added back in to help understand the RTI voltage noise calculation of the DUT. e_n is the RTI noise voltage of the DUT and i_n is the RTI current noise, solved for in Equation 10.

Equation 12 is the result of solving Equation 11 for the RTI noise voltage e_n. The term PA_{NOISE}^2 is the noise contribution from the PA and is equal to "$[A^2 + B^{!2} + C^{!2}]\ A_{PA}^2$". This value was characterized back in the "Procedure to Improve the DSA's Effective Noise Floor" section on page 2 (Figure 5) and will be used to determine the RTI voltage noise (e_n) of the DUT in Equation 12.

$$e_{t(0)}^2 = [e_n^2 + (R_S i_n)^2 + (R_1 \| R_2 i_n)^2 + 4kT(R_{EQ})]A_{DUT}^2 A_{PA}^2 + [A^2 + B^{2!} + C^{2!}]A_{PA}^2 \quad \text{(EQ. 11)}$$

$$e_n = \sqrt{\frac{e_{t(0)}^2 - PA_{NOISE}^2}{A_{DUT}^2 A_{PA}^2} - (R_S i_n)^2 - (R_1 \| R_2 i_n)^2 - 4kT(R_{EQ})} \quad \text{(EQ. 12)}$$

Where:

$PA_{NOISE}^2 = [A^2 + B^{!2} + C^{!2}]\ A_{PA}^2$

$R_{EQ} = R_1R_2/(R_1+R_2) + R_S\ (\Omega)$

i_n = Current noise calculated in Equation 10.

Figures 13 and 14 illustrate the ISL28290 (bipolar inputs) RTI current noise and voltage noise. The current noise measures 3.5pA/√Hz at 10kHz and the voltage noise is 1nV/√Hz. Figures 15 and 16 illustrate the ISL28148 (MOS inputs) RTI current noise and voltage noise. The current noise measures 10fA/√Hz. The typical noise increase, at higher frequencies, you see in a MOS device is swamped out by the high R_S and board parasitic causing the noise signal to roll off at the higher frequencies. The voltage noise for the ISL28148 measured 24nV/√Hz.

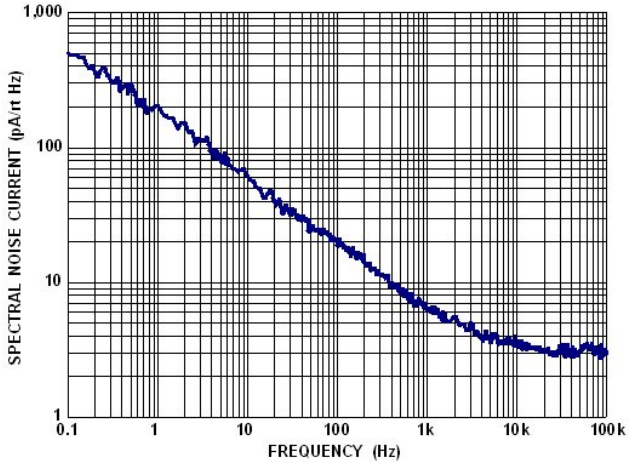

FIGURE 13. RTI CURRENT NOISE OF ISL28290

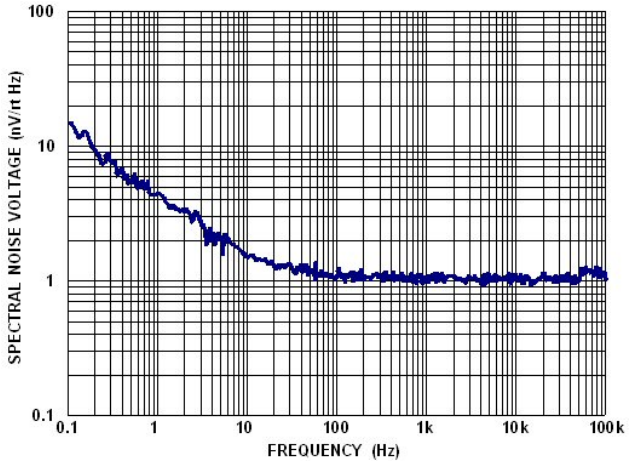

FIGURE 14. RTI VOLTAGE NOISE OF ISL28290

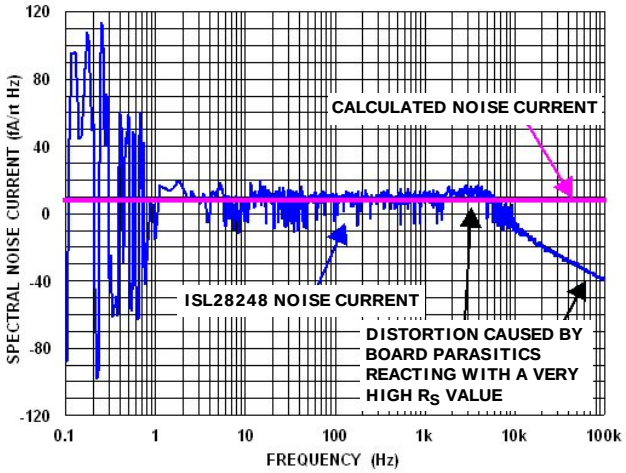

FIGURE 15. RTI CURRENT NOISE OF ISL28148

Conclusion

This Application Note has shown the test platform is capable of accurately measuring RTI noise voltages in the nV/√Hz range and currents in the fA/√Hz range down to 0.1Hz.

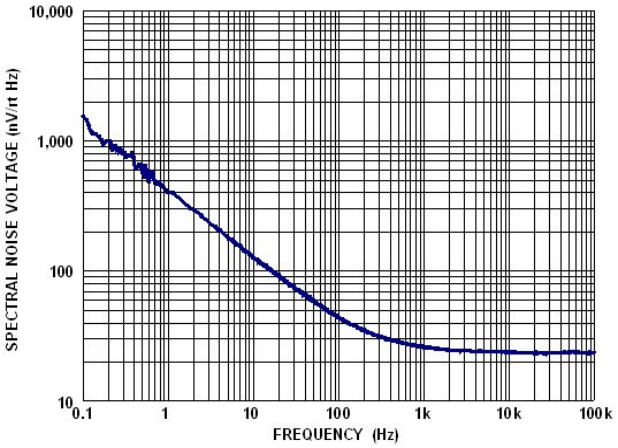

FIGURE 16. RTI VOLTAGE NOISE OF ISL28148

Things Learned Along the Way

1. The Post amplifier is necessary to improve the effective system noise floor of the DSA.
2. Measuring voltage noise of a device below 3 nV/√Hz can be accomplished by gaining up the DUT. The gain of the DUT lowers the contribution of the PA-DSA noise. This gain should be just enough to enable the measurement of the DUT's noise at 0.1Hz.
3. The Faraday cage provides another decade of frequency with a noise floor of 3nV/√Hz in the flat band range. This is critical for low frequency noise measurements.
4. The internal AC coupling of the DSA is inadequate for measurements below 1Hz.
5. The external AC coupling network results in having to account for the long time constant before accurate measurements could be made.
6. The series resistor used in the measurement of current noise needs to be as large as possible. The product of R_S^2 I_n^2 magnitude needs to be high enough to raise it above background noise and make it a measurable signal. Suggested starting point is to make R_S^2 I_n^2 >= $4kTR_S$.
7. Current noise measurements in the femto amps require sufficient averaging to be able smooth out the data.

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