Using a Digitally Controlled Potentiometer (DCP) for Video Gain and Cable Compensation

Introduction

Certain scenarios require video gain control. digitally controlled potentiometers (DCPs) are often overlooked for this application because they are thought to have too low of a bandwidth for video applications. Selecting the proper DCP can extend the circuit bandwidth to sufficiently support NTSC, PAL, and HDTV video. This application note reviews four DCP Solutions:

- Video Gain from 0.5 to Gain of 2
- Low-Noise Video Gain Control
- Low-Noise Cable Compensation
- Low-Noise Video Gain Control and Cable Compensation

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1. Compensation

The high operating capacitance of the CMOS switches used in the DCPs with large end-to-end resistance values reduces the DCP's signal bandwidth (see Figure 1). A low end-to-end resistance value DCPs is used for video to maintain as large a bandwidth as possible. The X9317ZS8Z is a good choice because it features a 1kΩ end-to-end.

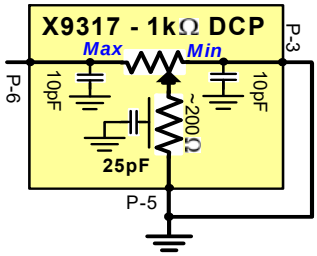


Figure 1. DCP Spice Model

A conventional gain control design, using a DCP, provides input signal attenuation and is followed by a fixed gain op amp. However, in a video application, the DCP requires bandwidth compensation.

2. Video Gain from 0.5 to Gain of 2

Figure 2 shows a basic design. No terminal of the DCP is left open. Reducing the chance of induced noise. The gain control, in this configuration, is as linear as the linearity of DCP. The video termination requires the typical gain of 2, but using the DCP (shown in Figure 2), as a voltage divider, requires an extra gain of 2. For comparison, using a DCP in the op amp feedback path would lower the bandwidth because of the internal capacitors shown in Figure 1. The design overcomes the effect of these DCP parasitic capacitors on bandwidth. Figure 2 shows the DCP configured as a voltage divider, which requires an extra gain of 2 to overcome this voltage divider loss. But, the added gain doubles the op amp noise. Because the op amp noise is small, compared to the video signal, this additional gain is not an issue except for large screen displays.

3. Bandwidth Enhancement

Figure 2 uses two small capacitors, C2 and C3, for bandwidth recovery to compensate for the bandwidth loss of the DCP. The capacitors have small values that have little risk of causing excess peaking. The stray DCP capacitance can cause excessive bandwidth lost when the wiper is at the low end of the DCP. The wiper has ~25pF to ground forming an RC pole with the resistance of the DCP. The pole causes high-frequency bandwidth roll-off.

When the wiper is at the bottom of the DCP, adding C2 gives an AC divider with the DCPs internal capacitance. This forms the same divider ratio as the DC resistive divider of the DCP. As a result, the AC and DC gains are equal and reduce the risk of excessive peaking. Because of the non-linearity of the AC performance of the DCP, C4 boosts the gain at the middle of the DCP range. C4 generates a little positive feedback to compensate for the loss at this mid-range.

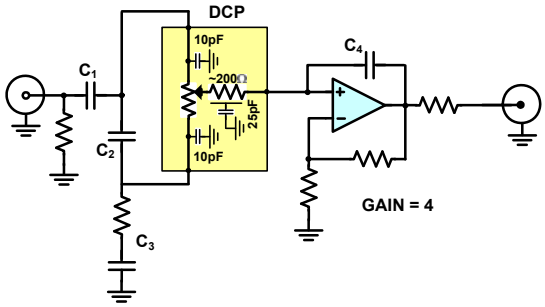


Figure 2. Video Gain DCP Bandwidth Compensation

4. Circuit Biasing

The X9317 DCP operates from a 0V to 5V supply. However, because the composite video signal is AC-coupled, the DCP can be exposed to negative voltages that exceed the device's absolute maximum ratings. To correct this, use a two diode clamp (D_1 and D_2) to clamp the sync tip to approximately 100mV above ground, see Figure 3. The 100mV is the result of the difference in the bias current of the diode D2 about 16:1 ratio relative to D1 Current. The clamp circuit also reduces some power line noise on the video input signal. At the beginning of each line, the sync tip clamps to zero. Therefore, any AC noise is clamped to zero, reducing the AC noise.

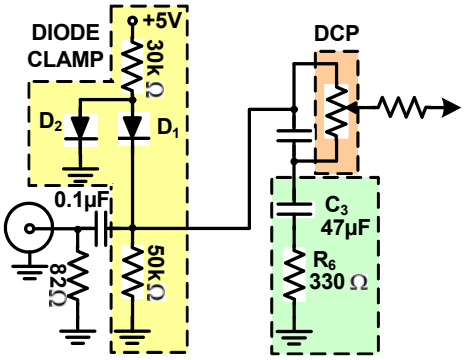


Figure 3. Input Diode Clamp And Biased Network

One end must be grounded to attenuate the incoming signal for the DCP. Form an AC Ground placing C_3 from the bottom of the DCP to ground. However, when the DCP wiper is at the bottom, there is no video output. Offsetting this node must allow for a required level of video out. By using R_6 = 330Ω, a 4:1 divider forms with the DCP end-to-end resistance. Therefore, the input is 2V, the output of the DCP is ¼ or 0.5V, and the gain of 4 of the amplifier, is 2V output of the amplifier.

The C_3 capacitor is large enough to maintain an average value of the video signal, which varies from ~0.4VDC to ~1VDC,and is unipolar. The average value is video content dependent. Because of the size of C_3, bias moves slow, and the range of bias works with the DCP and op amp. The op amp is a 0V to 5V supply part. Therefore, the sync-tip changes from 0.1V to 0.5V caused by the DCP setting and the video content. This requires using an output coupling capacitor to remove this DC bias.

Figure 4 shows the circuit with R_1= 82Ω input termination to ground for a 75 cable input. The 82Ω resistor is in parallel with the series combination of 1k DCP and R_6, a 330Ω resistor. Therefore, it provides approximately 75Ω termination for the incoming cable. There is also an output series resistor (75Ω) for back loaded cable driving.

If there is no output cable load then the op amp gain is set at two by changing the value of the gain and feedback resistors R_G and R_F to 1kΩ each.

4.1 DCP

The X9317 is a 3-wire up/down logic control DCP, and the datasheet gives all the details required for its proper control operation over the 3-wire interface. *Note*: The 3-wire interface operation in this application note is not covered.

4.2 Test Results

Testing of this attenuation design used a $1V_{P-P}$ AC signal to represent a standard $1V_{P-P}$ video signal. Adjusting the DCP to a $1V_{P-P}$ output with different input AC levels allows the determination of the 3dB bandwidth.

Table 1. Figure 4 Test Results

Input (V_{P-P})	Output (V_{P-P})	BW (MHz)
0.5	1.0	23.5
1.0	1.0	17
1.8	1.0	32

In summary the bandwidth of the design supports the bandwidth requirements for composite video.

Note: A key design is that the external comp (C_4 and C_2) were added to compensate for the effects of DCP.

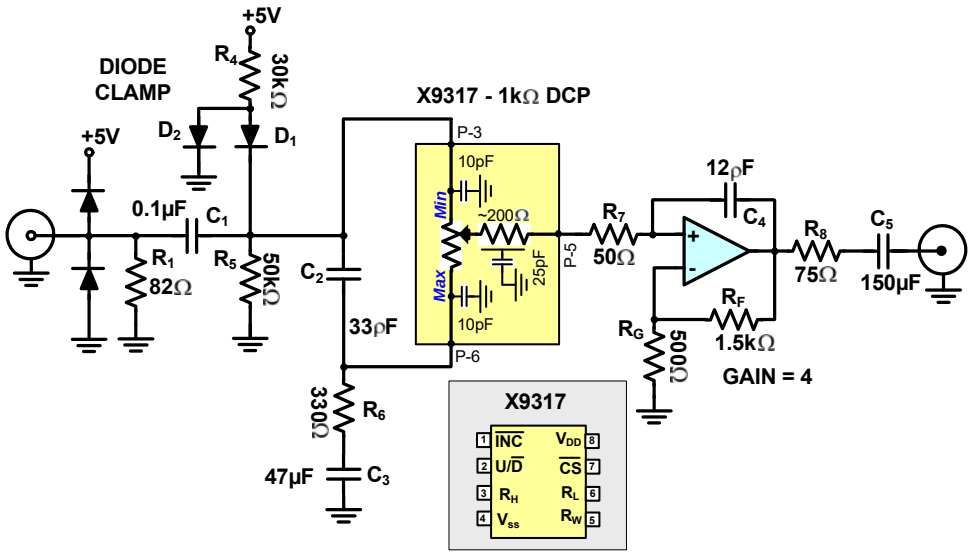


Figure 4. Complete Video Gain with Cable Compensation

5. Low-Noise Video Gain Control

This design shows how to use a DCP to program the video gain. Low-Noise Video Cable Compensation addresses Cable Compensation for loss of bandwidth because of the cable and Combination – Programmable Video Gain with Cable Compensation combines the video gain and cable compensation while addressing the signal to noise (SNR) issue.

5.1 Video Gain Control Problem

Medical video and projection video applications require high performance and require low noise to maintain image quality. This video design employs standard design techniques but lacks optimization for low-noise, see Video Gain from 0.5 to Gain of 2. This section develops a new design that addresses the low-noise requirements.

5.1.1 Comparison

Video Gain from 0.5 to Gain of 2 uses a fixed gain of 4x and the DCP acting as a voltage divider to attenuate the video for a fixed $1V_{P-P}$ output. The 4x amplifier amplifies both the video signal and noise to achieve a 1V output level. This has an adverse effect on the normal level video signal-to-noise ratio that is not best for image quality when the input video is 1V. At a 0.5V video input, the amp noise is the same for both designs, and the low-noise design is half the amp noise at 1V video input.

5.2 Design Considerations

Figure 2 shows the implementation of the DCP in the feedback loop as a gain control and not as an attenuator. The Video Gain DCP is outside the signal path and serves as the Video Gain Control potentiometer. The drawback to this design is the DCP stray capacitance and parasitic effects which limit the bandwidth. The parasitics cause gain changes within the frequency band of interest.

To reduce some of the parasitic capacitance, configure the DCP. Tie the R_W wiper and R_L of the DCP terminal to ground, to remove these pin's parasitic capacitance. This configuration leaves only the single 10pF of R_H and the DCP resistance to ground on the (-) summing node (see Figure 5).

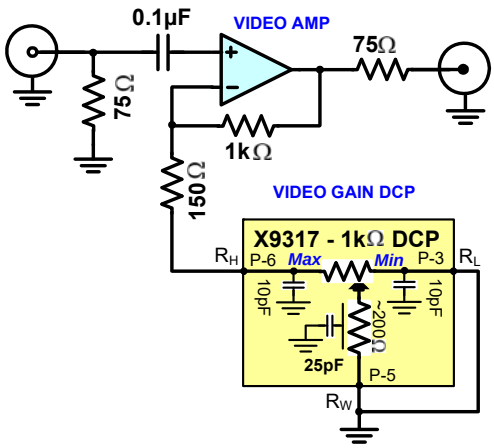


Figure 5. Basic Adjustable Video Gain Using DCP Control

The problem is if the pot runs to the top (Max, R_H), the ~200 wiper resistance limits the gain but the wiper resistance can vary up to 30%. Limit the gain to about 4. Therefore, the overall resistance of DCP leg would requires about 330Ω.

To resolve, place a 150Ω resistor at the (-) to the Video Amp, to insure a max gain of about 4. This 150Ω resistor has a second function, isolate the stray capacitance of the DCP R_H pin from the op amp summing node. This is to prevent capacitive loading of the node and the possibility of the op amp going into oscillations.

An unexpected issue is experiencing a high frequency gain loss of a few dB with the DCP at a max DC gain of 4, up to about 4MHz.

Looking closer at the DCP wiper FETs, even though it is small, ~200Ω, the wiper resistance influence the overall gain when the DCP is near the maximum gain (see Figure 7, the tail off of the lower trace).

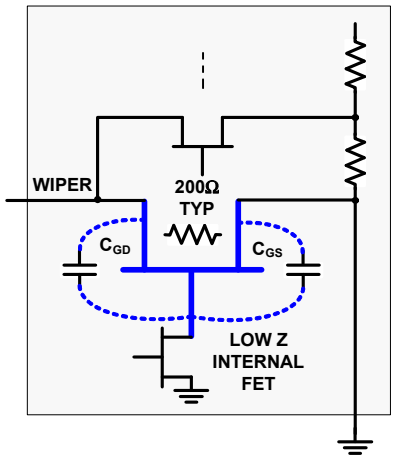


Figure 6. Basic DCP Wiper FET

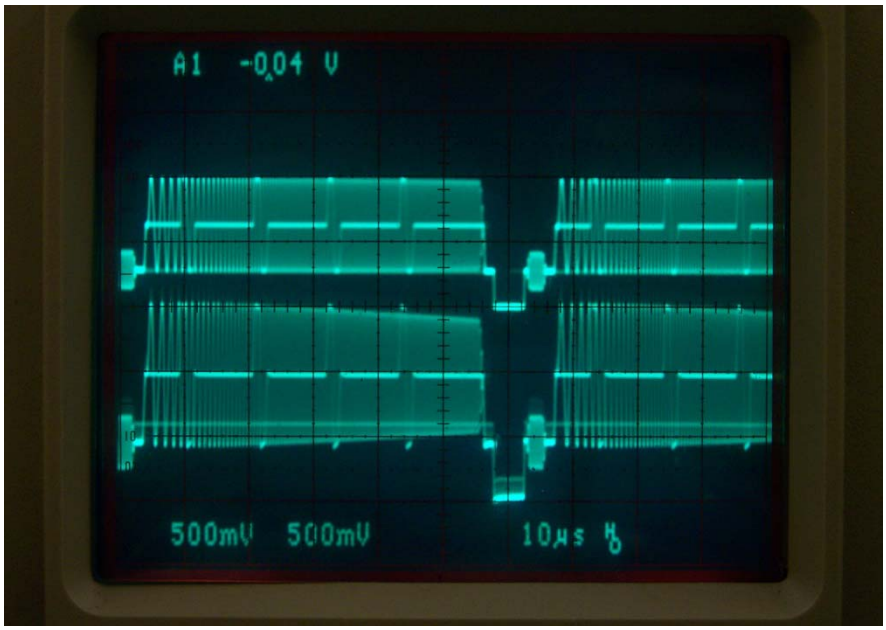


Figure 7. Effects Of The DCP Wiper Parasitics

In Figure 6, the design of FETs makes the capacitances the same for gate-to-drain (C_{GD}) and gate-to-source (C_{GS}). Because the wiper capacitance, from this basic model is about 25pF, and the wiper is the drain of this wiper FET, C_{GD} is about 25pF. Now looking at the wiper FET when it is at or near RH and the wiper is driving (Drain) with a 5MHz video signal, the C_{GD} forms a negative feedback path to the gate.

As the frequency increases so does the magnitude of the negative feedback, which drives the gate relatively out of saturation. As the FET comes out of saturation an FET starts to operate in a non saturated region. This results in lowering the gain of the video amplifier by increasing R_G. Therefore, the wiper becomes a frequency dependent impedance at higher frequency and have a negative impact on the higher gain settings.

Figure 7 at the lower trace, the top trace is the input and the lower trace the output. At the right side of the bottom trace, the gain is a lower gain than at the left end. This is the wiper FET changing impedance with frequency.

5.3 Solution

The impedance change caused by the wiper is small, but ,impacts the overall gain because it becomes more of the controlling impedance of the gain network. Lowering the impedance of the series 150Ω resistor as the wiper impedance increases, it maintains the overall value of RG constant at the higher gains and higher frequency. A simple method is to parallel some value of capacitance with the 150Ω so that the impedance decreases proportionally with the RW impedance increase.

The RC forms a frequency variable impedance to boost the high-end loss. Because the design includes a 150Ω resistor, the target capacitance requires an impedance of <150Ω at 5MHz. Testing demonstrated that placing a 360pF in parallel with the 150Ω resistor compensates for the DCP wiper impedance (see Figure 8).

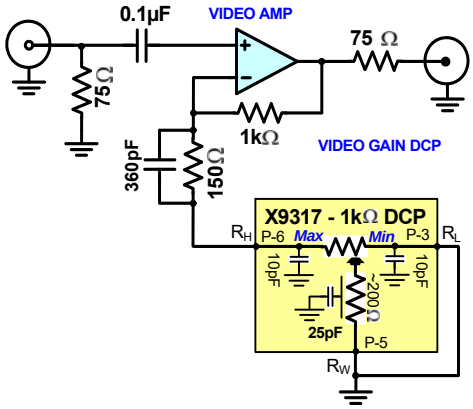


Figure 8. Video Gain DCP With Wiper Compensation

Note: This solution is for the selected DCP X9317 as other DCPs have different parasitic.

This configuration applied a standard NTSC video signal with the active video sweeping from 50kHz to 5.0MHz over a typical short length of cable [<25']. This short length cable does not cause any approachable frequency loss.

The wiper capacitance is considered as a lumped capacitance but technically it is distributed. This application using a lumped capacitance approach is sufficient to support the test results. The symbols in Figure 9 represent the wiper distributed capacitance for the 25pF capacitance on the wiper terminal, P-5.

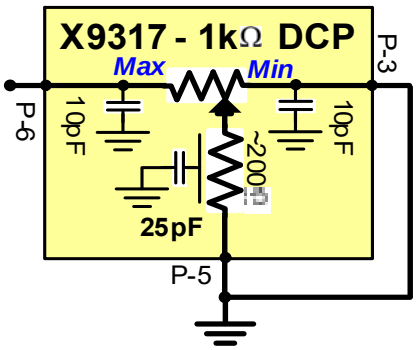


Figure 9. DCP Parasitic Capacitance

When the wiper is at RL there is a gain of about 2. However, at high frequencies, there are additional losses of about a few dB. The pot has a resistance of 1k + 150Ω that yields a DC gain just slightly under 2. The results show the gain was lower than expected, but only at the high frequencies. As with any DCP, the internal resistor string is made up of a series resistors switched in and out of the signal path by FETs. These FETs have a similar feedback issue as does the wiper FET. Take a similar approach to solve this problem.

Even though the wiper resistance and the DCP's parasitic capacitance form a parallel RC network, this internal 10pF from RH to ground is not sufficient to recover the frequency loss. The capacitance must increase by placing an external capacitor from RH to ground. Adding an external 22pF across the (-) summing node to ground, compensates for the loss at low-end gain. However, the capacitive loading the (-) summing node can cause instability and result in oscillation. Adding 75Ω at the summing node in series with the 22pF isolates the node from the added capacitance but still retains the HF gain compensation. The added 75Ω does not affect the DC gain as it is capacitively isolated from ground.

The min and max 10% range of the DCP are slightly over compensated at 5MHz so that the most important mid 80% of the range has a flat frequency response.

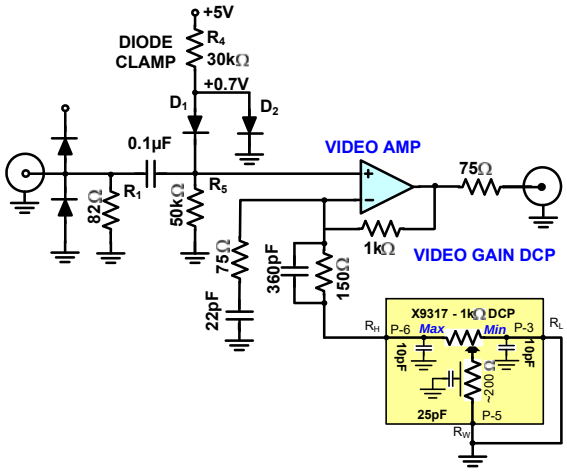


Figure 10. Complete Detailed Video Gain Control

5.4 Summary

Figure 11, shows the results of iSim simulation of Figure 10. The green trace is with the DCP at RH, minimum gain and the blue trace is with the DCP at RL, maximum gain.

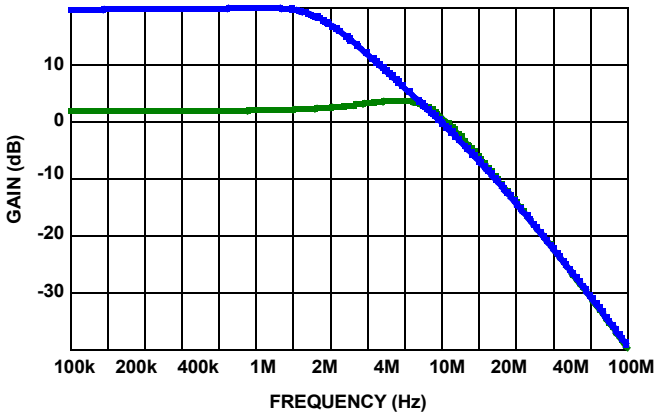


Figure 11. iSiM Simulation of the Gain

The simulation shows the gain is relatively constant over the video frequency range.

Note: All scope trace scales are 500mV per division for both top and bottom traces. The Video signal spans 0.1MHz to 5MHz. The envelope shape of the video signal from 0.1MHz to 5MHz is the only interest, not the fine details of the content of these envelopes.

5.5 Low-Noise Gain Control Figure 10 Test Results

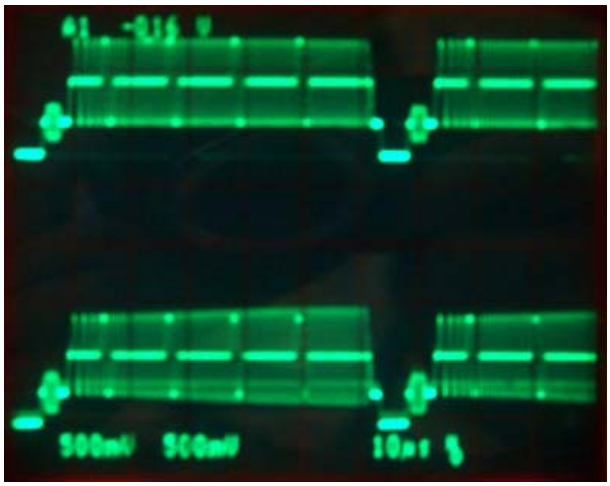


Figure 12. Video DCP at Minimum Setting

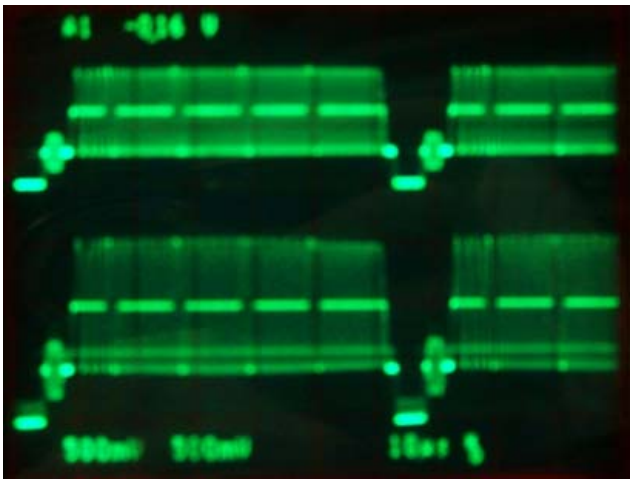


Figure 13. Video DCP at Middle Scale

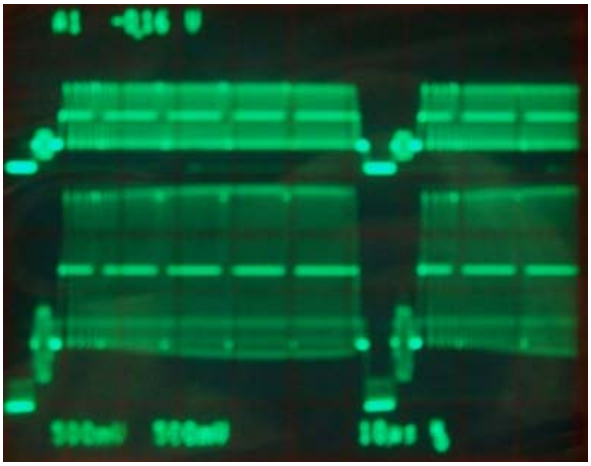


Figure 14. Video DCP at Maximum Setting

Note: Double-loading the input to prevent amplifier clipping.

5.6 Test Results

Figure 12, Figure 13, and Figure 14 show a video scan test pattern used for the input signal. This pattern covers the required bandwidth. The bottom trace is the corresponding output. The envelope shape demonstrates the effect of the design over the desired frequency spectrum: Trace A and B - 500mV/div at 10µs/div. The DCP parasitic capacitance effects the gain to some extent. It is relative flat over the spectrum. This supports non-professional video applications.

5.7 Low-Noise Video Cable Compensation

The typical video coax used is RG-59 for cable compensation peaking without gain control. This is a 75Ω cable that has different losses of different frequencies depending on the different characteristics of the cables. RG-59 comes in low loss, standard loss and hi-loss cable (miniature cable). RF Coax is specifically designed for RF frequencies but has high loss at lower frequencies (under 5MHz) because of the copper clad iron core center conductor.

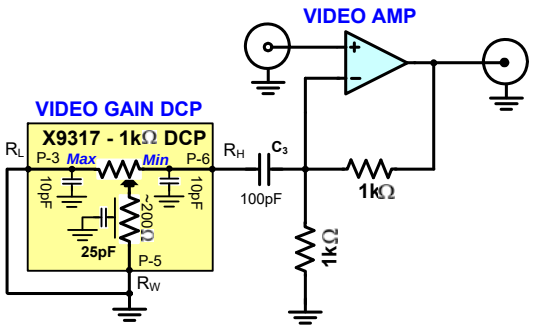


Figure 15. Basic Cable Compensation Network Using a DCP

To correct for cable losses, resulting in losses at higher frequencies, the concept is a simple programmable RC peaking network in the gain leg of the video amplifier. Adjust the gain of the video amplifier to compensate for cable frequency losses and maintain near-flat gain over the required frequency range of 0.1MHz to 5MHz. Using a DCP, to compensate for a range of cable peaking problems. Figure 15 is a basic diagram of this concept. The cable compensation video gain amp is set to a gain of 2 with a 1kΩ resistor from summing node to ground. This circuitry gives AC peaking gain control and a small range of video gain.

Similar to the programmable Video gain circuitry in Low-Noise Video Gain Control, use a series RC network with the DCP replacing the R for a simple solution. Two similar issues to address:

- Capacitive loading of the op amp summing node which can cause the summing node of the Video Op-Amp to oscillate.
- The selection of the series C for the peaking network plus compensate for the DCP parasitic capacitance.

5.8 Capacitive Loading of the Summing Node

As with the programmable video amplifier, the series C isolates from the summing node by placing a resistor in series to the video amplifier (-) input. This 75Ω resistor, shown in Figure 16 as R_9, isolates the fixed capacitance from the summing node. As in the Video Gain DCP, the 75Ω resistor has no impact on the DC gain as it is isolated from ground through the series capacitor C_3. The resistor prevents capacitive loading of the node and prevents the possibility of the op amp going into oscillations.

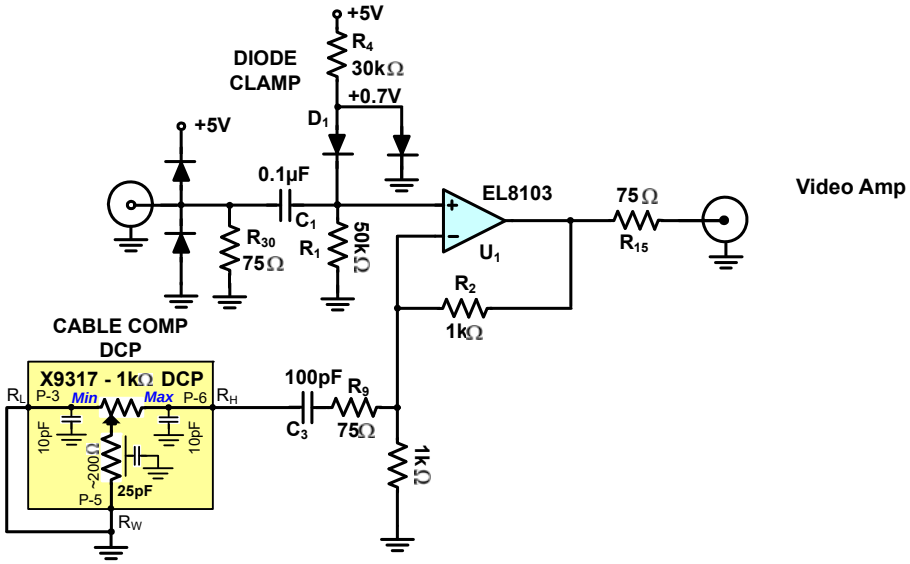


Figure 16. Cable Compensation Circuit

5.9 Selecting the Value of the Series C3 and Dealing with the Parasitic Capacitance

Two issues are addressed:

- A reasonable size for the series C_3 to address the cable losses on the higher frequencies.
- Reducing the effect of the DCP R_H capacitance on the series R9C3 network.

Using a 1kΩ DCP in series with 100pF fixes the 3dB point (see Figure 16). RH capacitance is typically 10pF. When one capacitor is 10 times larger than the other, the larger capacitor dominates, allowing the smaller capacitor to be ignored for all practical purposes.

Using a 100pF cap in series with the 1kΩ DCP gives a starting point. Figure 17 is the iSim simulations of the circuit as shown in Figure 16, where the green line is the op amp with a gain of 2, no cable compensation (wiper at minimum). The blue line is with the maximum Cable Comp (wiper at maximum), only the wiper resistance, 200Ω, in series with the 100pF to ground. *Note*: The simulation model does not take into account any parasitics; they validate the ability of the basic circuit to program the peaking to meet the requirement.

5.9.1 Low-Noise Video Cable Compensation with DCP Simulation and Actual Test Results

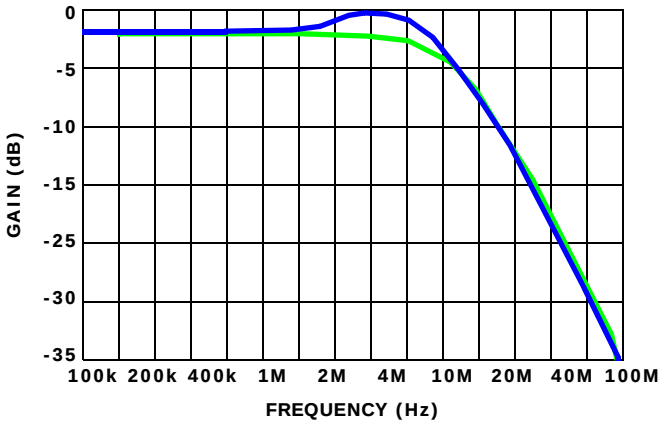


Figure 17. Cable Compensation DCP At Minimum [Green] And Maximum [Blue]

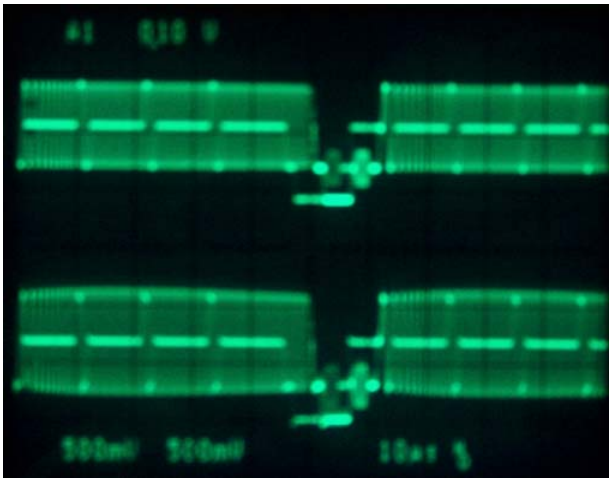


Figure 18. Cable Compensation DCP at Minimum

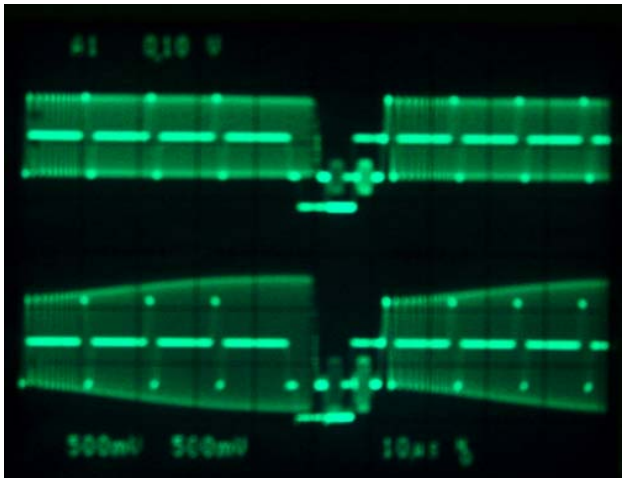


Figure 19. Cable Compensation DCP At Maximum

The iSim simulation model lacks a complete parasitic model, but it does show the cable compensation peaking at 4MHz.

In summary for Figure 18 and Figure 19, the top trace is a video scan test pattern used for the input signal. This pattern covers the required bandwidth. The bottom trace is the corresponding output. The envelope shape demonstrates the effect of the design over the required frequency spectrum.

Note: The envelope shape, over the 0.1MHz to 5MHz sweep range, shows the results of the cable compensation network of the DCP at minimum and maximum settings. The maximum setting (Figure 19) results in high frequency peaking.

The Cable Compensation (Figure 16), DCP is capacitive coupled to the peaking circuit, which is used to adjust the RC time constant and therefore, the gain peaking.

5.10 Comment on Video Coax

Video coax comes in a variety of types from very low loss to typical loss to high loss. Different cables with different losses change the length that this design can compensate. This also change the cable compensation required.

RF coax with copper-clad iron-core center wire has more DC resistance and more loss at low frequency and can affect performance with video. Special cable compensation is needed with RF coax for the added DC loss.

Note: To correct for DC Cable losses, the video gain change is normally small.

5.11 Video Cable Compensation DCP Comments

- This design uses input or output coax cables from 250 feet up to about 1000 feet long depending on the quality of the coax cable used.
- Coax Cable losses are not linear [~6dB/octave] over the entire video frequency span. Because the sync tip is most susceptible to this problem, selectively tune the cable compensation network might be required. Use band selective peaking in conjunction with the overall cable compensation network, to both tune the overall performance and to match the specific cable used.

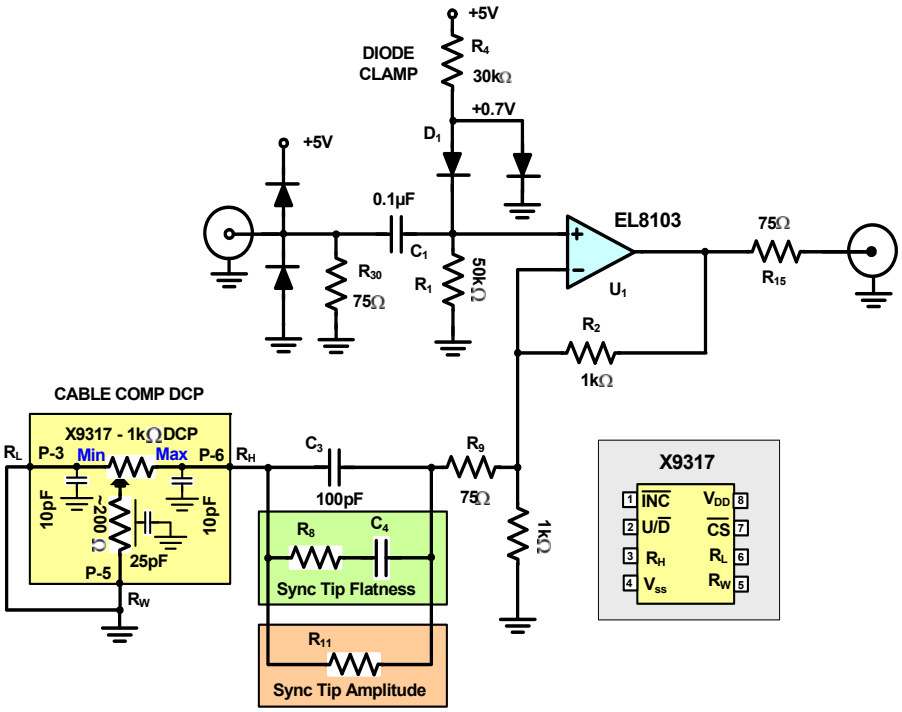


Figure 20. Cable Compensation with Selective Sync Tuning

5.12 Improving Sync Tip Flatness and Amplitude

To improve the sync tip amplitude (see Figure 20), adding R_{11} in parallel with C_3 acts as band pass that boots to recover the lost amplitude on the Sync Tip at the required frequency. For the flatness, use a series low pass filter RC network in parallel with C3 to flatten out the Sync Tip. The Cable Comp network C_3, C_4, R_8, R_9, and R_{11} is dependent on the coax cable used. The values are usually determined by quantitative testing. Next are some ranges to correct the impact of the cable on the sync tip (The values are set with max cable length on the input and the AC DCP is set for max compensation).

- The R_{11} in the range of 1kΩ to 10kΩ is set for sync tip amplitude.
- The C_4 ~100pF to 200pF and R_8 ~1kΩ to 4kΩ are set for sync tip flatness.
- The C_3 and R_9 are set for 5MHz amplitude but R_9 should not be <75Ω as the DCP R_W resistance is typically 200Ω.

6. Combination – Programmable Video Gain with Cable Compensation

Different coax cables have different loss at different frequencies. A simple solution is to combine the Combination – Programmable Video Gain with Cable Compensation with the Low-Noise Video Cable Compensation. Use this combination to compensates a variety of coax cables with good results.

Minor changes occur with each combination when combined and are listed as follows (see Figure 22):

- Cable Compensation network – Video Gain DCP network replaces the 1kΩ gain resistor and also the Sync Tip Amplitude resistor R_{11}.
- Video Gain network – Eliminate the 22pF to ground on the Programmable Video Gain DCP and replace it with the Cable Comp DCP network.
- Use this design with input or output coax cables from 250 feet up to about 1000 feet long depending on the quality of the coax cable used. Using maximum Video DCP and Cable Comp DCP settings with 1V video input can cause noticeable clipping of the HF portion of the video signal. If unacceptable clipping occurs, use more of the coax on the input and less on the output, or use better coax and do not use both DCPs at maximum settings with 1V video input. Video test signals can cause clipping, but real video seldom does; therefore, when no good alternatives exist, maximum DCP settings provide the best option.

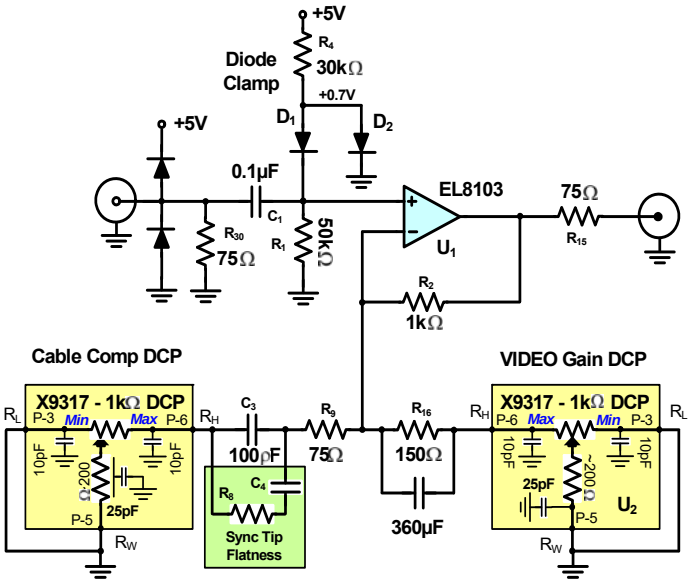


Figure 21. Complete Video Gain with Cable Compensation

Figure 22 through Figure 26 show the results of the design shown in Figure 21 with the two DCPs at different settings.

6.1 Test Results Using Figure 21

A video scan test pattern provides the input signal. The complete DCP video gain control yields good video signal quality while maintaining the all important sync tip flatness. The value of this design controls the gain and independently compensate for cable loss using a simple up/down push button DCP for control.

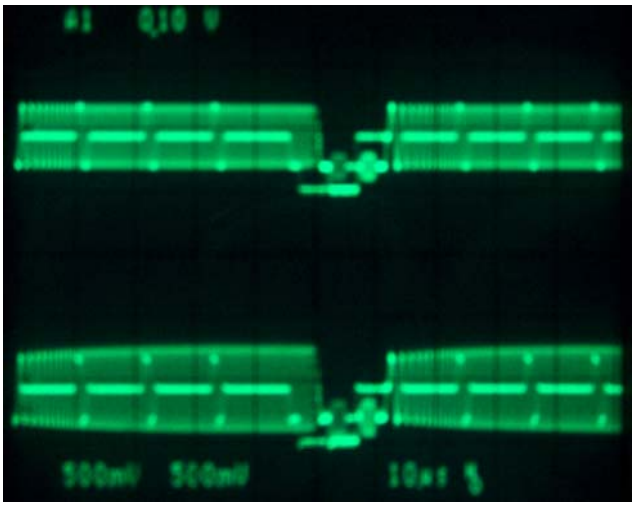


Figure 22. Cable Comp at Minimum – Video Gain DCP Minimum

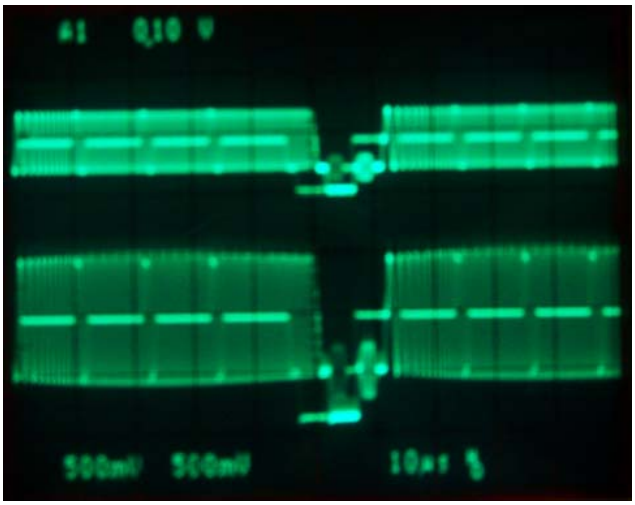


Figure 23. Cable Comp at Minimum – Video Gain at Middle DCP Settings

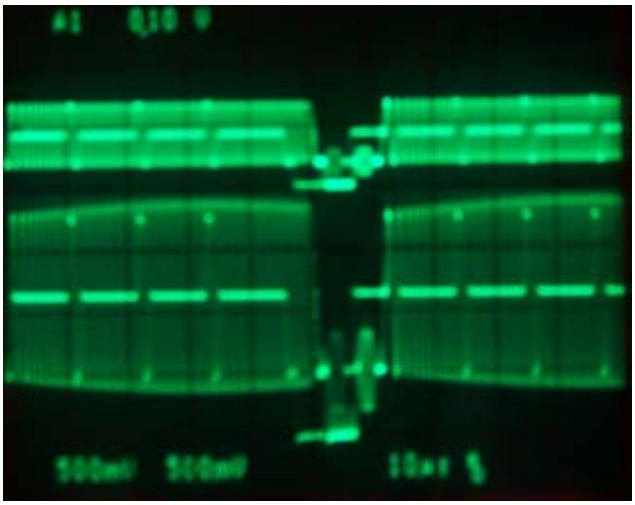


Figure 24. Cable Comp at Minimum – Video Gain at Maximum DCP Settings



Figure 25. Cable Comp at Maximum – Video Gain at Minimum DCP Settings

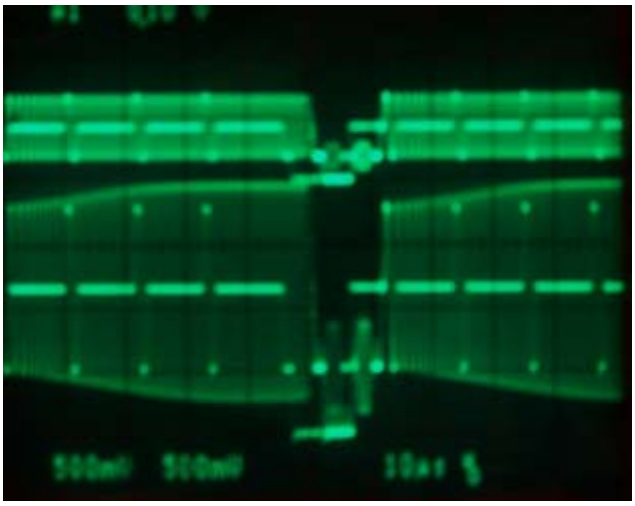


Figure 26. Cable Comp at Maximum – Video Gain at Maximum DCP Settings

7. Revision History

Revision	Date	Description
1.00	Oct 30, 2026	▪ Applied latest template ▪ Added Revision History section
0.00	Jan 18, 2011	Initial release.

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