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Automatic Digital Cable Compensation for Long Cat-5 Cables

Successful transmission of data down long Cat-5 cables will require different cable compensations based on the cable characteristics per unit length to extend the usable signal length. RS-485 drivers provide a good square wave into the Cat-5 cable. However, at the end of a long cable, the output looks more like a series of RC dampened waveforms. The rise/fall times at the beginning of the cable are much faster and slow down further down the cable as the RLCs of the cable attenuate the signal. Often, the rise/fall times are so long that they will not reach the required levels for detecting the data at the end of a long cable. This application note will address a series of networks to reduce Common Mode Voltage (CMV) and automatically compensate for high frequency cable losses and small signal level.

Key Objectives

- Generate the maximum signal level at the received end of a long Cat-5 cable by:
  - Using proper termination and reduction of the CMV
  - Bypassing the input offset network to recover high frequency signal loss
- Correct for the amplifier input offset to maximize the CMV range for large signals
- Limit the input signal swing from saturating the amplifier, thus, maintaining the amplifier's maximum bandwidth and minimum response time
- Protect from the possibility of excessive voltages (ESD) developing on the long cable and damaging the circuitry at both ends
- Automatically detect small signal and automatically adjust the amplifier gain
- Automatically detect slow low rise time edges and peak their rise time

Overview

We design this network to be a point to multipoint optimized for the maximum data rate over the longest cable distance possible while supporting a maximum number of receiver nodes. This paper will cover the steps and issues related to a point to multipoint long distance transmission and the common mode voltage induced due to long cable runs. Following the design discussion, we will expand our discussion to cover modifications to the design, supporting point to point and ground differences that result in CMV.

The automatic digital cable compensation circuit is designed to yield the maximum digital data rate over the maximum length of Cat-5 cable with automatic adjustments. The concept is to use a wide band amplifier for the receiver, as well as the cable compensation comparator. The op amp selected for this example is the EL5175, which has a wide bandwidth and is designed to extract the difference signal from noisy environments, such as receiving signals from twisted-pair lines or any application where common mode noise injection is likely to occur. We selected a standard RS-485 transmitter (ISL3159) as the source of the digital data as it will drive the twisted pair differential. This application note will address the numerous issues with long distance digital transmission down twisted wire pairs and suggest solutions.

Basic Block Diagram (Figure 1)

Figure 1 addresses the necessary blocks we discovered to extract the maximum signal level received at the end of a very long Cat-5 cable. Maximizing the signal starts with:

- Both ends properly terminated to minimize reflections and maximize the receive signal amplitude. We will also allow for multiple receivers without loading the RS485 transmitter beyond the maximum loading allowed by the EIA-RS485 standard.
- The DMIR (Differential Mode Input Range) of the selected receiver (EL5175) is ±2.3V (4.6V) and the RS-485 is capable of supplying +5V.
  - Therefore, we will need to scale the RS-485 input.
  - The divider needs to be shunted to -5V Input Offset circuitry to prevent the EL5175's input from being driven beyond the maximum CMV specification.
- Cat-5 cable will attenuate high frequencies more than lower frequencies. Small high frequency signals can be adversely impacted by the CMV network. We can reduce the impact of the scaling circuitry by using a small bypass capacitor in the AC Recovery circuitry to bypass the resistive divider and thus, pass-through the high frequency edges without attenuation.
- The EL5175 is used as a comparator to recover slow rise and fall times but with it's unique input structure. This input structure allows us to control the gain without impacting the input impedance.
- Preventing the EL5175's inputs from being driven into saturation. Doing so would result in a slow saturation recovery time, thereby lowering the overall bandwidth.
  - We will use an input limiter to prevent the input signal from approaching the input saturation levels.
- ESD protection must be placed at both ends to prevent damage from possible static discharge.
- Limit the output in order to insure that the output does not saturate. The auto feedback circuit will detect large output swings and change the gain, keeping the output in the linear region.

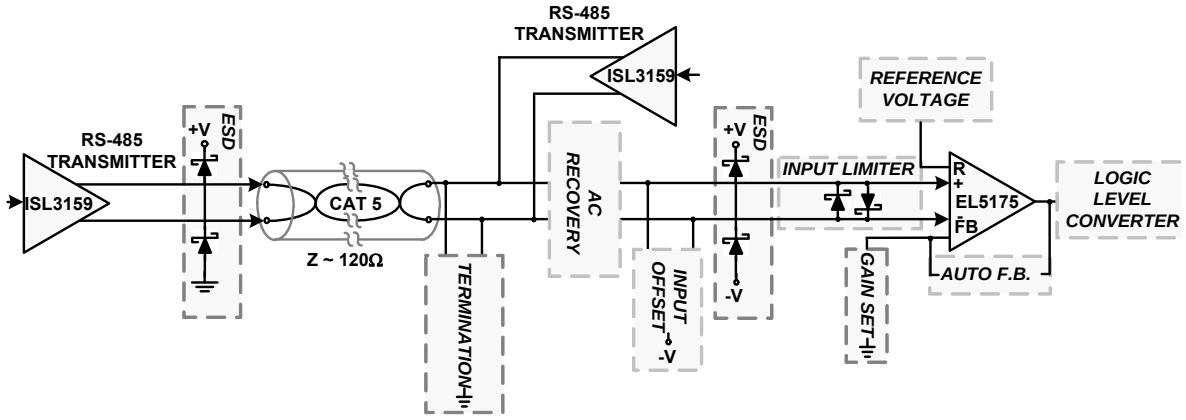

FIGURE 1. BASIC BLOCK DIAGRAM

- Setting the gain of the EL5175 will gain the V_{REF} and V_{IN} equally. The DC gain = 1 + R_F/R_G. The input is driven from an RS-485 differential driver where the differential +V is a logic 1 and -V is a logic 0. We need to set the gain when the minimum logic 1 or 0 differential V_{IN} is present on the input; the output will go to the respective voltage level for the Logic Level converter and will properly detect a logic 0 or 1.

Details of the Point-to-Multipoint Input Network

Cable Terminations (Figure 2)

We have a cable termination what will appear to the RS-485 as a 0.6mA load. We have a maximum of +7CMV, and each input will see about 2kΩ input loading. Yet, we also want to reduce the common mode 60Hz noise that might be picked up along the long cable run. If we use two resistors across the twisted wires and have the common point AC-coupled to ground, we can design the input network to appear as a 4k differential input load and decouple 60Hz noise as well.

Selecting the capacitance to ground is somewhat arbitrary but you must remember, the smaller the impedance to ground, the more 60Hz attenuation but the larger the capacitor needed. We selected to have two 2kΩ resistors with their common point to a capacitor to ground. So you have a resistance across the wire pair of 4k and have 1k impedance to ground. To compute the capacitor value use Equation 1:

$$X_C = \frac{1}{2\pi fC} \quad \text{(EQ. 1)}$$

Where: F = 60Hz, X_C = 1,000Ω

$$C = \frac{1}{2*3.1415*60Hz*1,000} = 2.6\mu F\,min \quad \text{(EQ. 2)}$$

We choose 4.7µF since the value is not critical and larger is better.

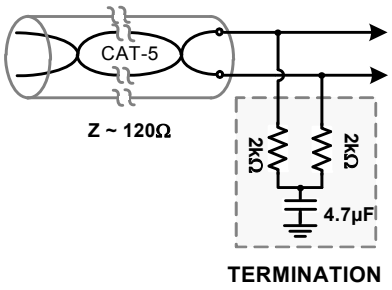

FIGURE 2. CABLE TERMINATION

More detailed discussion on the design of the input termination network to support point-to-multipoint RS485 operation can be found in “Other Consideration” on page 9.

Input Offset (Figure 3)

We selected the EL5175 because it is a ±5V supply op amp with a common mode voltage of -4.3V to +3.3V. We will use a differential mode input range (DMIR) of ±2.3V in this design. The input signal would typically be from a RS-485, which will drive a 3V to 5V differential signal above ground. The RS-485 differential output has its zero point at midway between the 0V and 5V, or 2.5V. Using a simple resistive divider network on the input will bring the common mode zero point to ground. The 10kΩ series and 20kΩ to -5V presents a 1/3 voltage attenuator to the differential signal. Tying the bottom of the 20kΩ resistors to -5V provides the offset of -2.5V to the input signal, which moves the common voltage point down to the local ground.

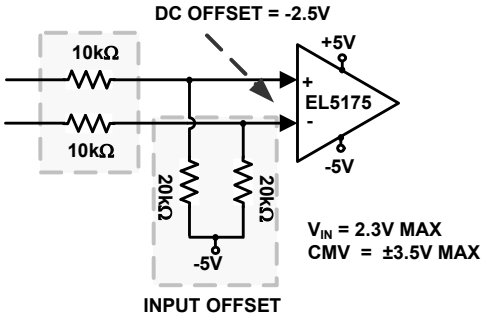

FIGURE 3. INPUT OFFSET

AC Recovery (Figure 4)

Cat-5 cable will attenuate higher frequencies more so than lower frequencies. To insure small signals are not attenuated further by the offset network's resistive divider, we place a 1000pF bypass capacitor around the two 10kΩ series resistors. The 1000pF will pass more of the HF edge onto the input of the op amp without attenuation. The DC zero point is set to ground by the resistive network, yet the high frequency component will be above ground. We will have to protect the input from going into saturation.

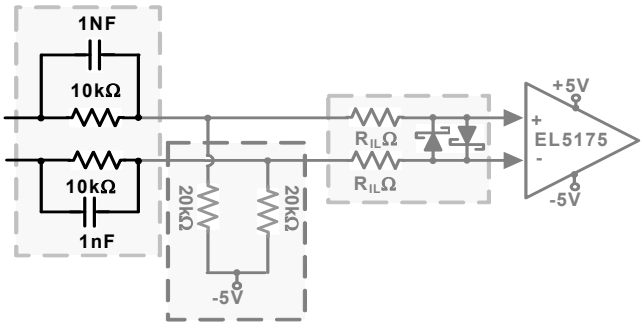

FIGURE 4. AC RECOVERY/PEAKING CIRCUIT

Input Limiter (Figure 5)

We need to prevent the EL5175 inputs from being overdriven and drive the op amp in saturation. Doing so will slow the response time of the EL5175 or maybe damage the op amp. A simple diode clamp on the input will prevent overdriving the inputs. We use two fast Schottky diodes, each one back-to-back across the input. Using fast Schottky diodes will clamp the input to one diode forward biased junction level. Thus, limiting the input swing to about ±0.3V (Schottky V_{FB} is 0.3V) and prevent overdriving the op amp input. Remember, we are using this op amp fundamentally as a comparator to regenerate the digital signals.

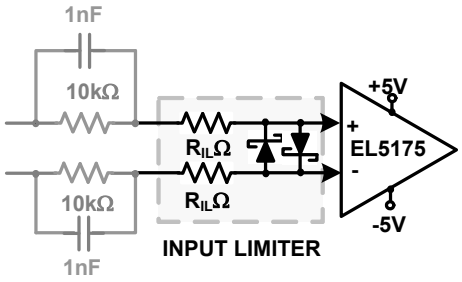

FIGURE 5. INPUT LIMITER

Reflection Control

This circuit is designed to be very sensitive to RS-485 differential input signals. Reflections from multi node applications which have receiver nodes close to the driver will cause reflections along the transmission line. These reflections could be detected as signal by other receivers on that same transmission line. This is a big problem with 'T' type stubs on the transmission line or when the driver is not at the end of a transmission line.

You need to consider the transmission line characteristics in order to understand the need for the series resistors in the Input Limiter network. The objective is to generate the largest input to the op amp and yet still meet the other requirements while not changing the input impedance of the network. The rule of thumb for speed of a signal down copper is 1ns per foot of wire. Also, the Cat-5 has a typical DC resistance of about 20Ω per 1,000 feet.

If the input signal has a fast rise time edge (as with digital signals), the rise/fall edge contains high frequency components. A good first order approximation of the bulk of the frequency energy is shown in Equation 3:

$$F = 0.35/t_R \quad \text{(EQ. 3)}$$

where:

t_R is the slew rate in V/s

Thus, for a high slew rate of 2V/ns, the bulk of the energy contained in this edge is around 175MHz. The diodes will present a short to the incoming edge when the voltage is greater than 0.3V. This short will cause a large reflection. This reflected edge will transmit back down the cable to the termination at the other end and be reflected back again. Once again, the AC recovery will place the reflected signal on the input to the op amp/comparator.

The round trip time is 2x the cable length times 1ns/ft. For sake of discussion, we assume the pulse width is 1µs and the cable is 600 ft., therefore the round trip time would be 1.2µs (assume speed to be ~1ns/ft.). The reflected edge will appear as a positive pulse 1200ns after the incident pulse has returned to 0V. Thus, the EL5175 could detect a false signal and translate it to logic output.

AC Impedance Termination (Figure 6)

Since we are driving the cable with a RS-485 driver, we need to terminate the receive end of the cable for the high frequency pulse edges to reduce reflections. The incoming digital pulse will see the entire input termination network. The AC impedance needs to be 100Ω to 120Ω to these high frequency edges. What does the network look like to these edges?

The critical impedances are at high frequencies. There are a few elements of the overall input circuitry that can be omitted from the input AC impedance calculations. The peaking circuit with its 1000pF bypass will act as a short and short-out the 10kΩ series resistors as denoted in Figure 6 as <10Ω. At high frequencies, the -5V supply is an AC ground. The cable is terminated at the input to the EL5175 by two back-to-back Schottky diodes and can be represented as a 300mV AC source. So, for large HF signals, the input circuitry will appear as shown in Figure 6.

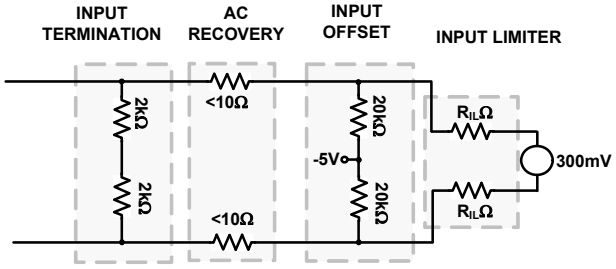

FIGURE 6. AC IMPEDANCE TERMINATION NETWORK

Computation of the Input Limiter Resistors - R_{IL}

Looking in differentially is 4kΩ in parallel with $2R_{IL}$. For this discussion, we assume this input network impedance needs to look like ~120Ω across the input to properly terminate the Cat-5 cable. Also the two 20ks are to AC ground do not enter into the differential calculation for RL. We also want to insure the maximum signal amplitude is developed at the input to the EL5175.

$$120\Omega = (|4k\Omega||2R_{IL}|) \quad \text{(EQ. 4)}$$

$$R_{IL} = 62\Omega$$

The HF large signal impedance model would appear as 120Ω across the output of the Cat-5 cable.

ESD Protection to (Figures 7 and 8)

Long cable can develop static charge, and if not addressed, can cause electrical failure at either end of the Cat-5 cable. We selected to use fast Schottky diodes to clamp the differential wire pair at the input to +5V and ground.

Yet, using this more classic ESD configuration for a unipolar device, as shown in Figure 7, caused a problem to the unipolar EL5175. When the Cat-5 cable is disconnected and the circuitry is powered up or down, the lower ESD diode would go into forward conduction with current flowing from ground, through the lower ESD diode to the input divider network to -5V. This forms a simple voltage divider of 10kΩ and 20kΩ to the input of the op amp.

If we leave the diodes at the input of the cable, we limit the CMV to ±5V, as the diodes will clamp at ± 5V. Yet, we can still have good ESD protection for the active components and maintain the maximum CMV of +7V to -4V by moving the ESD protection to the input of the Limiter as shown in Figure 8..

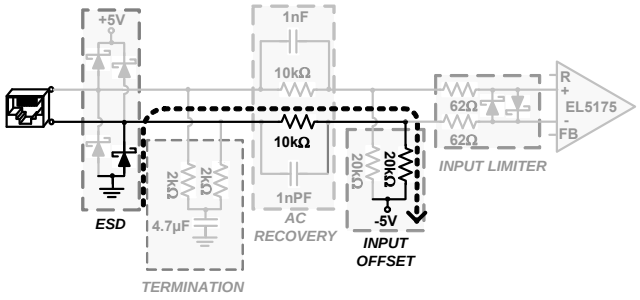

FIGURE 7. CLASSIC ESD STRUCTURE

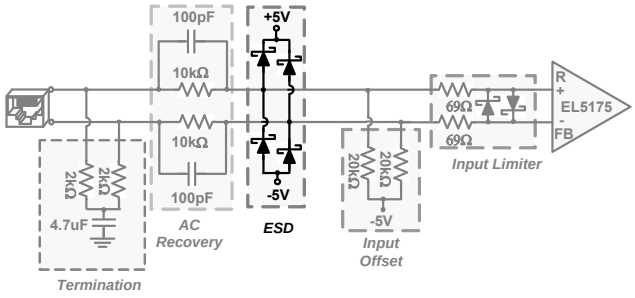

FIGURE 8. FINAL ESD STRUCTURES

Complete Input Network (Figure 9)

At this point, we have the signal properly terminated and ESD protected at the receiver. We have reduced any common mode low and high frequency elements. The input zero point has been adjusted to ground while allowing high speed low level edges to bypass the input voltage divider. We have also insured the EL5175's inputs are not driven into saturation while reducing the side effect of the input limiter's impedance, generating reflected waves.

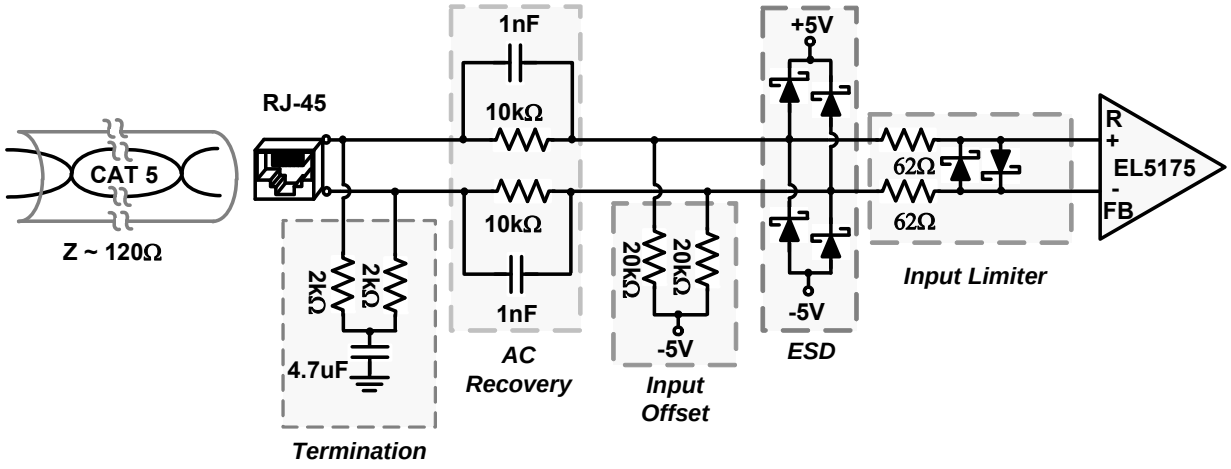

FIGURE 9. COMPLETE INPUT NETWORK

Details of the Output Network

Auto Gain Adjust (Figures 10 and 11)

We need to automatically detect small signal and adjust the amplifier gain, as well as automatically detect slow low rise time edges and peak the rise time. The objective is to sense the output level and change the gain so the EL5175 gains up the small signals but limits the large signals, keeping the output from saturation. We first need to determine the setting for the VREF pin. Since the output of the EL5175 will be driving the RS-485 receiver section of the ISL3159 (used as a logic level converter), we need only to set the gain. We do not need to offset small signals since the ISL3159 will detect inputs over a wide DC range, above and below ground. Therefore, we will ground the VREF pin.

Gain

We need to select a large enough gain to amplify small signals but keep the gain within an acceptable range, not so large to be prone to oscillations. Also, a gain of 100 would keep the RF feedback resistor below 100kΩ while keeping RG at a reasonable size. This is a good starting point and we can refine it later, if needed.

VREF is at ground, and then the formula simply becomes Equations 5 and 6:

$$V_{OUT} = (+5mV) \times 100$$
$$V_{OUT} = +0.5V \quad \text{(EQ. 5)}$$

$$V_{OUT} = (-5mV) \times 100$$
$$V_{OUT} = -0.5V \quad \text{(EQ. 6)}$$

The differential inputs for a logic 1 and 0 are +0.5V and -0.5V respectively and are well within the ISL3159 input operational limits. A voltage sensing feedback network is needed to keep the EL5175 out of saturation to insure the fastest response time needed to maximize the data rate. The simplest network uses an output voltage sensing feedback resistor controlling the gain and keeping the output from saturating.

Using two transistors, as shown in Figure 10, the Auto Gain Limiter, will limit the upper and lower output voltage levels. Using an NPN and PNP turning on when V_{OUT} is approaching the positive and negative limits respectively will act as a voltage controlled variable resistor across a fixed resistor, which will establish the DC gain over a wide range of inputs. Once the corresponding output voltage just below saturation level is reached, the appropriate transistor will lower the gain, limiting the output voltage. Using a PNP with its base at one VBE drop below the upper saturation limit and a NPN with its base at ground is a simple but effective way to keep the output from going into saturation.

By using the two transistors, NPN and a PNP and bias the base of the PNP using two resistors in series, we experimented with the turn-on threshold of the PNP, in this case we started at 2.0V on the base of the 2N3906.

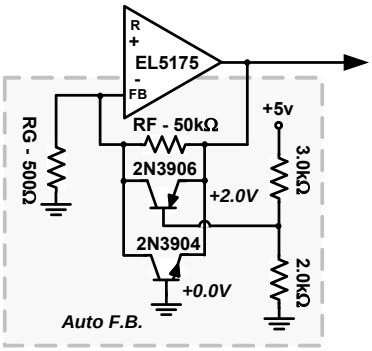

FIGURE 10. AUTO GAIN LIMITER

Positive Limiter

Placing the PNP (2N3906) across RF and biasing the base at 2.0V, when the EL5175 output reaches about 2.4V, the PNP will start turning on, lowering the effective value of RF. If the output reaches about 2.6V, RF feedback will be reduced so the output will be held by the base voltage plus the VBE of the

PNP to 2.6V. Below V_{OUT} = 2.0V, RF will control the EL5175 output.

Negative Limiter (Figure 10)

Place the NPN (2N3904) across RF and bias the base at 0.0V. When the EL5175 output reaches about -0.4V, the NPN will start turning on. When the output reaches about -0.6V, the RF feedback will be reduced so the output will be held by the base voltage plus the forward drop VBE or -0.6V. Above VOUT = 0.0V, RF will control the output.

Simplified Limiter (Figure 11)

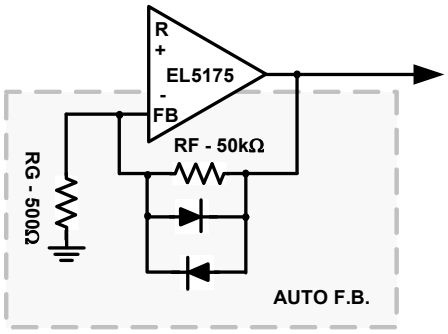

FIGURE 11. SIMPLIFIED AUTO GAIN LIMITER

Experimentation showed that the threshold was not critical to the data rate. Therefore, we could eliminate the transistors and bias resistor by placing two back-to-back signal diodes across the RF (50kΩ) resistor and obtain similar results. This lowers the cost and simplifies the layout. The final schematic has the diodes in place of the transistors as shown in Figure 11(Simplified Auto Gain Limiter).

Rise Time Peaking (Figure 12)

We need to consider how to improve the signal rise times, which will be impacted by the long Cat-5 cable distributed RLCs. Improving the rise time will require a frequency controlled gain where we gain up the edge slew. Basic Cat-5 cable rise time (under the conditions of V_{IN}) is 5ns slew from 10% to 90% of V_{IN} and V_{OUT} 0% to 50% of V_{IN}.

1000ft ~ 200ns Rise Time to 50%

5000ft ~ 1500ns Rise Time to 50% (EQ. 7)

When digital signals are transmitted down long distances on twisted wire cable (such as Cat-5 cable), the rise time or fall time of the digital signals are slowed as a function of cable length. Slow edges can be peaked by simply setting up an RC network that would change the gain to a higher gain during the initial edge reception. Doing so would peak the EL5175's output rise time for slow edge rates as shown in Equation 8.

Output Rise Time = Input Rise Time/Gain (EQ. 8)

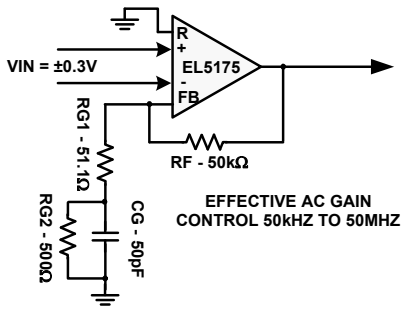

FIGURE 12. RISE TIME PEAKING CIRCUIT

Using a simple bypass capacitor, C_G, in parallel with R_G will change the gain by changing the effective value of R_G. C_G will look like a short at the start of the slew. However, if we just short R_G to ground, the gain will be infinite. To keep the circuit stable and not ringing, an AC gain of about 1000 would be a reasonable trade-off during the peaking window. A gain of 1000 would require R_G to be about 50Ω. Therefore, if we use a 500Ω resistor bypassed with a 50pF capacitor, the parallel combination, in series with 50Ω, will yield an AC gain of about 1000. We use the same 51.1Ω resistor as used in other parts of the design. The AC gain peaking circuit is AC-coupled to prevent excess offset on the output of the EL5175 amp.

AC gain computations during the initial slew of the input signal are shown in Equation 9:

$$\text{AC Gain} = 1 + 50\text{k}\Omega/51.1\Omega \quad \text{(EQ. 9)}$$

where: AC Gain = 980

Summary

The complete network addressing these numerous issues is shown in Figure 13. We have developed a complex input termination network as a summation of solutions to numerous issues extending the useful digital signal length of Cat-5 cables to about 4kft at 1Mbps data rate. By proper selection of simple passive components, we have optimized the input impedance. By using simple back-to-back silicon diodes, we have automatically adjusted gain to expand the range of low level input signals and sped up slow rise time edges.

If you only need point-to-point bi-directional, half duplex RS-485 serial data communications, all you need to do is duplicate the right side of the circuitry described here at both ends of the Cat-5 cable. You will need simple digital controls to select the receiver and the transmitter. If you only need unidirectional data, the RS-485 Transmitter ISL3159 in the top center can be omitted.

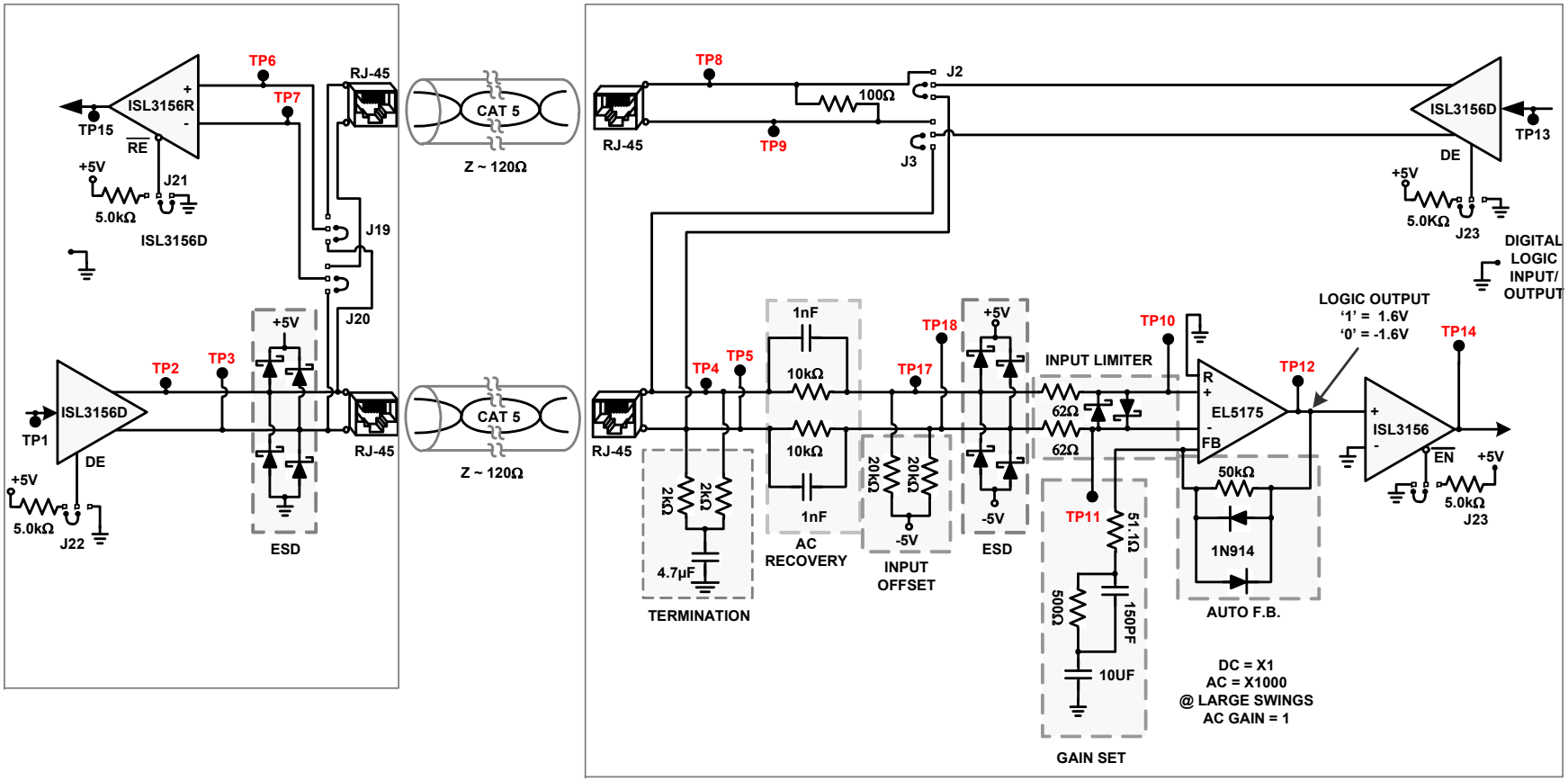

FIGURE 13. COMPLETE POINT TO MULTIPOINT RS485 TRANCEIVER WITH POWER SUPPLIES

Point to Point Test Results

Figure 14 is an EYE diagram for 1Mbps at a Cat-5 cable length of 4k feet with the threshold at 0.8V and 2.0V.

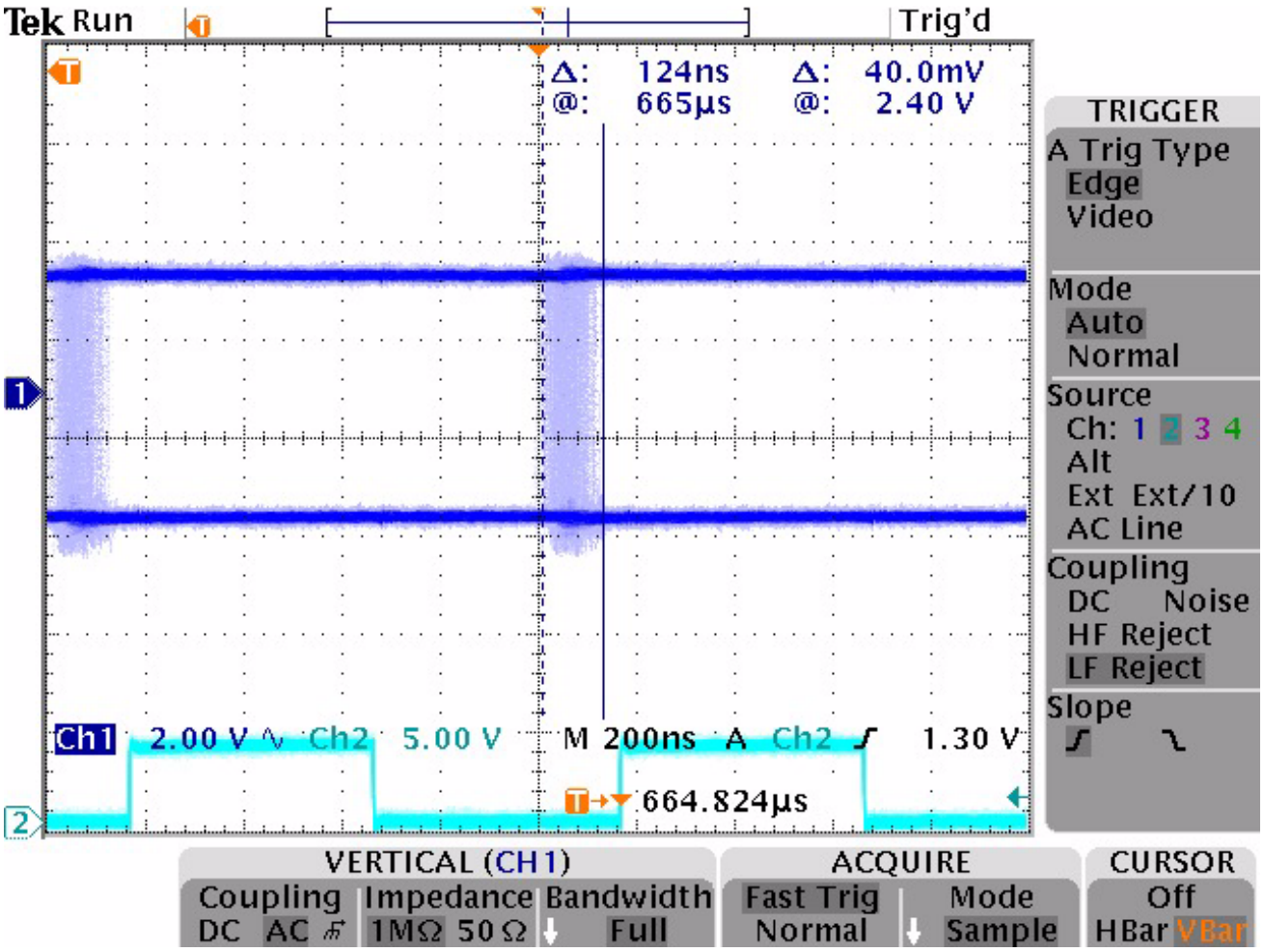

FIGURE 14. 1MBPS @4kft AND JITTER UNDER 15%

Figure 15 is an EYE diagram for 500kbps with Cat-5 cable length of 1mile and the threshold at 0.8V and 2.0V.

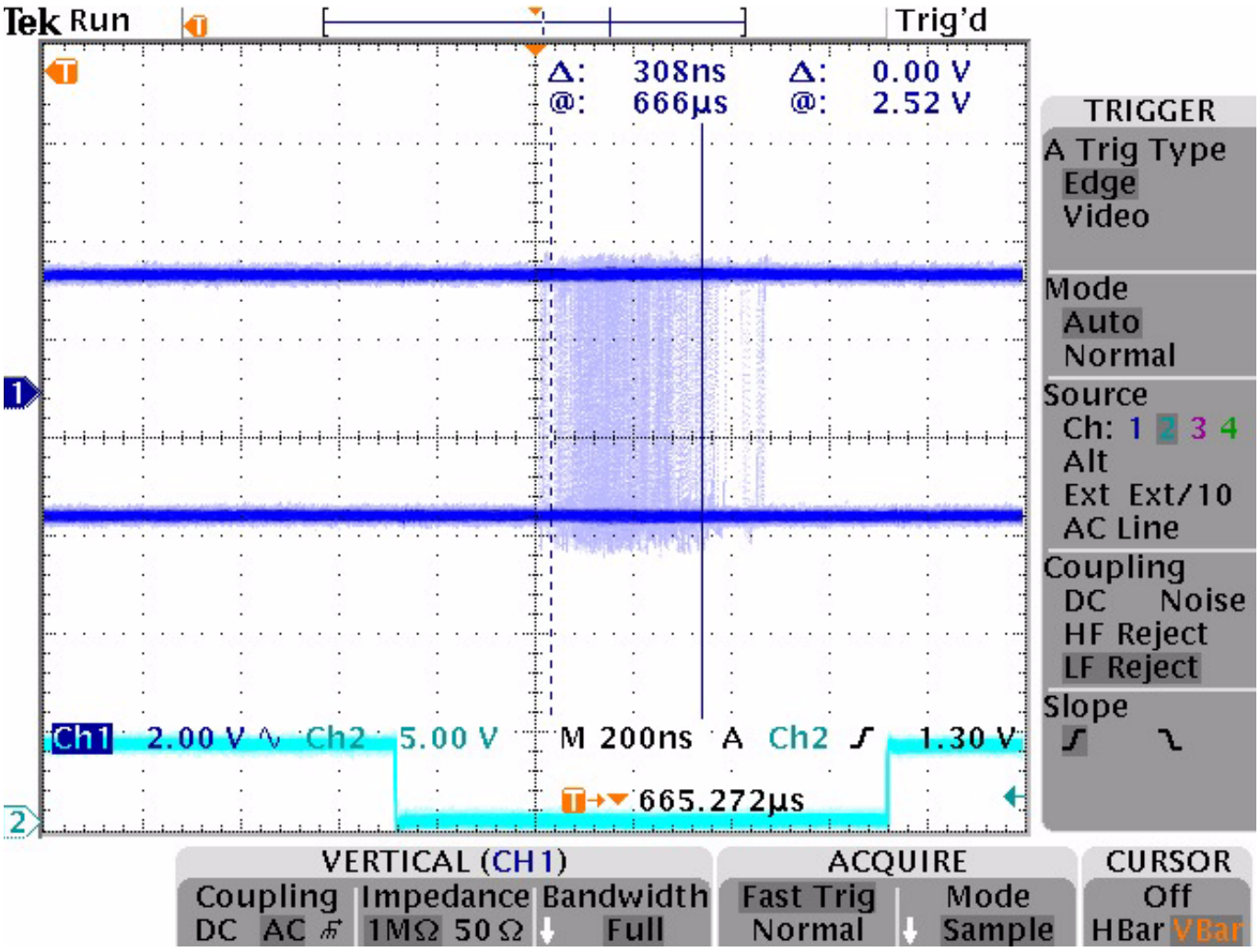

FIGURE 15. 500kBPS @1MILE

Other Consideration

Circuit Implementation

We added a simple ±5V on-board supply to take advantage of POE (Power Over Ethernet). Thus, this circuitry can be used as a repeater with an additional identical circuit at the receive end. The limit to the number of repeaters is the sum of the noise for the circuits. The noise will be the RMS sum of the each series circuits.

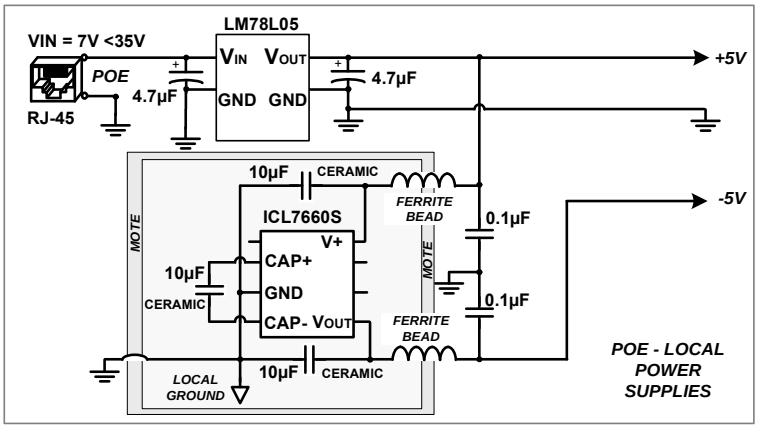

FIGURE 16. POE TO ±5V SUPPLY

Consideration for the Layout for the ±5V Power Supply

POE to ±5V Supply (Figure 16)

To reduce additional noise on the ground plane, the ICL7660S needs to be isolated. The noise from the ICL7660S was reduced using two techniques.

- First, we use ferrite beads on the input from the +5V regulator, and on the output of it's -5V. These beads will help isolate the switching noise the charge pump will generate.
- Second, isolate the ICL7660S ground noise file by cutting a mote in the ground plane around the ICL7660S and making an electrical connection to the board ground at a point furthest from the EL5175 and it's I/O power pins.

Point-to-Multipoint RS-485 Loading

The RS-485 specification deals primarily with common mode loading, you do need to consider differential loading to determine which would have the greater loading effect on the RS-485 transmitter.

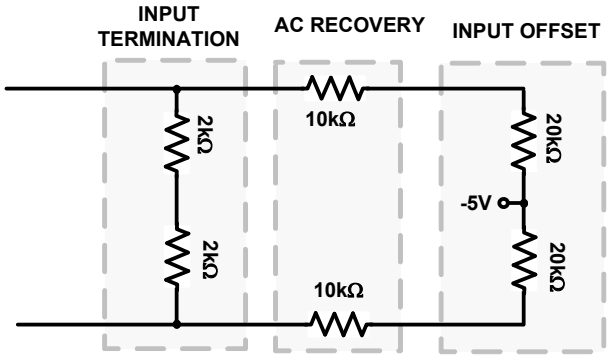

FIGURE 17. EFFECTIVE COMMON MODE INPUT NETWORK

Computing the input common mode RS-485 unit load, for this design is shown in Equation 10:

$$7\text{Vinput CMV} + (-5\text{V})/10\text{k}\Omega + 20\text{k}\Omega \,||\, 20\text{k}\Omega$$

$$7\text{V}/20\text{k}\Omega = 0.6\text{mA} \qquad \text{(EQ. 10)}$$

Since RS-485 Max Common Mode Current is 32mA (1mA*32 loads)

Therefore: 32mA/0.6mA ~ 53 loads

The RS-485 differential mode unit load maximum is equivalent to 54Ω. This circuit design loads the line with 4kΩ||40kΩ and for all intensive purposes, the load is just a 4kΩ across the line.

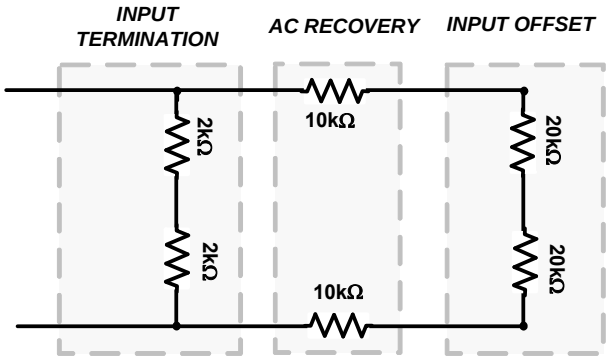

FIGURE 18. EFFECTIVE DIFFERENTIAL INPUT NETWORK

Thus, we can hang about 53 nodes on the line before reaching the maxim differential load allowed.

Summary

You can see the Common Mode Unit Load is the predominate limitation to the number of these designs you can drive from one RS-485 driver and remain within the loading specification.

CMV Reduction

The CMV generally consists or three parts:

First, is the electromagnetic induced voltage

Second, is the electric field coupling into the cable, which we refer to as a soft CMV sources as loading will reduce the voltage level.

Third is the difference in the grounds from end-to-end of the cable, which refer to as fixed or hard CMV. Loading has little effect on hard CMV.

Yet, hard CMV is usually a lower voltage level than soft CMV. Under light loads, soft CMV can be much larger then the hard CMV but can be reduced to low levels with heaver loads. The CMV input range for this circuit is +7V to -4V for the combination of all CMV sources. Although this is lower than normal RS-485 specification, the heaver CMV loading will often result with the lower CMV levels

Appendix - Cat-5 Point-to-Point Digital Transmission (1Mps @ 1Mile)

Unlike the previous Point-to-Multipoint termination, we do not need to be concerned about multi-to-point loading of the transmitter. We need to focus on an optimum termination structure to insure the maximum range. So, we can focus on how to insure the optimum single termination network.

Cable Terminations

Cat-5 cable impedance is typically 100Ω. We want to not only terminate the cable but offer some common mode noise attenuation at both ends. The overall input network should have an AC impedance of 100Ω. Typically, we would use two 51.1Ω resistors in series across the cable, this will appear as a 100Ω termination to the differential signal. Yet, we have to correct for an input offset by adding resistors on the input, impacting the input impedance.

At this point lets first work on the Input offset then work backwards to the input termination network. Determining the input offset network will dictate what we need for the input termination network. The final adjustment to 100Ω AC input impedance will be done at the input limiter network.

Input Offset (Figure 19)

We selected the EL5175 because is a ±5V supply op amp with common mode voltage of -4.3 to +3.3. We will use a symmetrical ±3.3V for CMV range and a differential mode input range (DMIR) of ±2.3V in this design. The input signal would typically be from a RS-485 which will drive a 3V to 5V differential signal above ground. The RS-485 differential output has its zero point at midway between the 0V and 5V, or at 2.5V. Using a simple resistive divider network on the input will bring the common mode zero point to ground. The 1kΩ series and 2kΩ to -5V presents a 1/3 voltage attenuator to the differential signal. By tying the bottom of the 2kΩ resistors to -5V provides the offset of -2.5V to the input signal which moves the common voltage point down to the local ground.

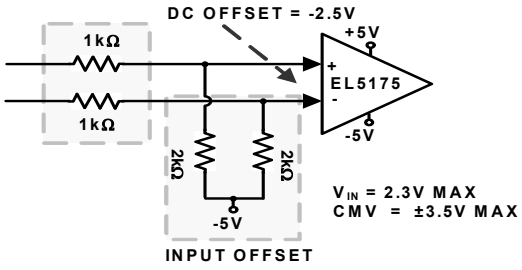

FIGURE 19. INPUT OFFSET

ESD (Figure 20)

Long cable can develop static charge and if not addressed, can cause electrical failure at either end of the Cat-5 cable. The ISL3159 is a unipolar 0 to +5V output so we selected fast Schottky diodes to clamp the differential wire pair to the +5V and ground rails. We connected the ESD to +5V and ground vs the more classic configuration of ±5V to overcome the CMV problem when the Cat-5 cable is disconnected with the circuitry powered up. When the input Cat-5 cable is disconnected the lower ESD diode would go into forward conduction, causing the CMV input to the EL5175 be driven to -3.1V. This is well within the lower CMV limit of -4.3V. If we had connected the lower ESD diode to -5V, then when the cable is disconnected, the input would have gone to -5V, beyond the -4.3V CMV limitation.

These added ESD diodes will greatly reduce the possibility of an ESD-induced failure. The ESD structure should be implemented at both ends to protect the transmitter as well as the receiver. If cables can be exposed to higher energy ESD, you should consider additional surge protection devices.

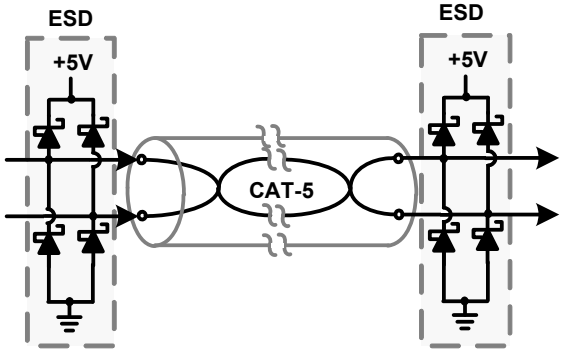

FIGURE 20. ESD PROTECTION NETWORK

AC Recovery (Figure 21)

Cat5 cable will attenuate high frequencies more so than lower frequencies. To insure small signals are not attenuated further by the offset network's resistive divider, we place a 1nF bypass capacitor around the two 1kΩ series resistors. The 1nF will pass more of the HF edge on to the input of the op amp without attenuation. The DC zero point is set to ground by the resistive network, yet the high frequency component will be above ground. We will have to protect the input from going into saturation.

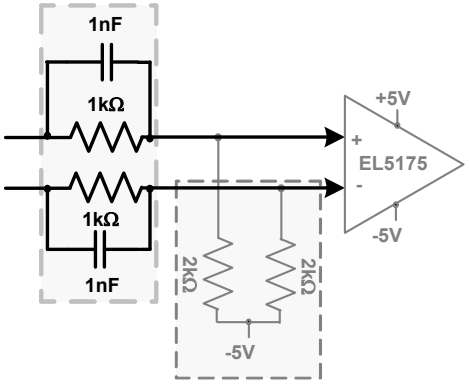

FIGURE 21. AC RECOVERY

Input Limiter (Figure 22)

We need to prevent the EL5175 inputs from being over driven and drive the op amp in saturation or maybe even damage the op amp. A simple diode clamp on the input will prevent overdriving the inputs. We use two fast Schottky diodes, each one back to back across the input. Using fast Schottky diodes will clamp the input to one diode forward biased junction. Thus, limiting the input to about ±0.3V (Schottky VFB is 0.3V) and preventing over driving the op amp input. Remember we are using this op amp fundamentally as a comparator to regenerate the digital signals.

You need to consider the transmission line characteristics to understand the need for the series resistors in the Input Limiter network. The objective is to generate the largest input to the op amp and yet still meet the other requirements and not change the input impedance of the network. The rule of thumb for speed of a signal down copper is 1ns per foot of wire. Also, the Cat-5 has a typical DC resistance of about 20Ω per 1,000 ft.

If the input signal has a fast rise-time edge, as with digital signals, the rise/fall edge contains high frequency components. A good approximation of the bulk of the frequency energy is as shown in Equation 11:

$$F = 0.35/tR \quad \text{(EQ. 11)}$$

where: tR is the slew rate in V/s

Thus, for a high slew rate of 2V/ns, the bulk of the energy is contained in this edge is around 175MHz. The diodes will present a short to the incoming edge when the voltage is greater than 0.3V. This short will cause a large reflection. This reflected edge will transit back down the cable to the termination at the other end and be reflected back again. Once again the AC Recovery will place the reflected signal on the input to the op amp/comparator.

The round trip time is 2x the cable length x 1ns/ft. We assume the pulse width is 1µs and the cable is 6,000 ft., then the round trip time would be 1.2µs. The reflected edge will appear as a positive pulse 200ns after the incident pulse has returned to 0V. Thus the EL5175 could detect a false signal and translate it to logic high.

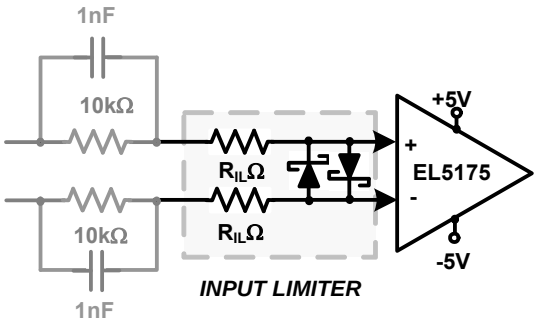

FIGURE 22. INPUT LIMITER

Determining the Input Termination Network (Figure 23)

We would normally use two 50Ω resistors is series across the input twisted pair lines. Yet, we have an AC impedance of 2kΩ as a result of the offset circuitry. A good starting point is to use the simple rule of thumb 10:1 not to impact the offset network. If we use 1/10th of the 2kΩ to AC ground, we would start with two 200Ω resistors in series with the common point to AC ground.

200Ω will not impact the input offset but is large enough to develop an adequate input levels for small incoming signals from the Cat-5.

This series connection gives us a common balance point with equal impedances to the differential cable. This point will have any common mode noise present. We can attenuate common mode noise by shunting it to ground. Long cables are susceptible to moderate level low frequency noise pickup such as AC line noise. To attenuate this low frequency common mode noise, we use a 1kΩ resistor to ground. Addressing the high frequency common mode noise, we use a 0.1µF to shunt the HF common mode noise around the 1kΩ resistor to ground. This method of common mode attenuation will not affect the differential cable termination impedance.

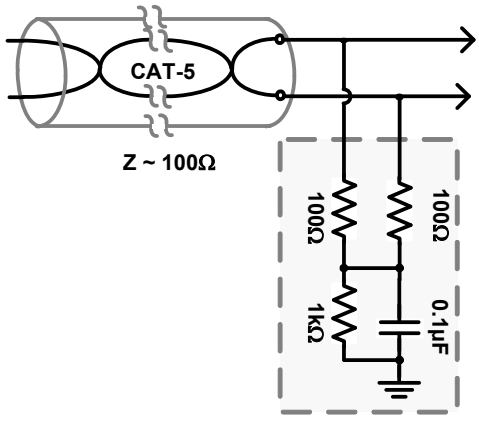

FIGURE 23. INPUT TERMINATION

How to compute R_{IL} for 100Ω Input Termination

The entire receiver network needs to appear as a 100Ω to 120Ω termination across the twisted wire pair for large high frequencies signals. Also, we need to keep the common mode reduction, DC offset and small signal amplitude peaking networks to insure the optimum digital signal recovery.

For this discussion we will use 100Ω for the cable impedance. If we do not compensate the overall network to appear as 100Ω, we will have large reflections causing multitude of problems. If we select a 4:1 ratio at the input, we can lower the Input Limiter series resistance value. By placing a resistor in series with the input limiter, the diode short now will appear as a 138Ω termination resulting in a small 38Ω mismatch that will be corrected in the other circuitry. When the input to the amplitude signal is less than 300mV the input termination will

be increased and thus increase the input signal amplitude. At low levels and slow rise times reflections are not a problem. So, for large HF signals, the input circuitry will appear as in Figure 24:

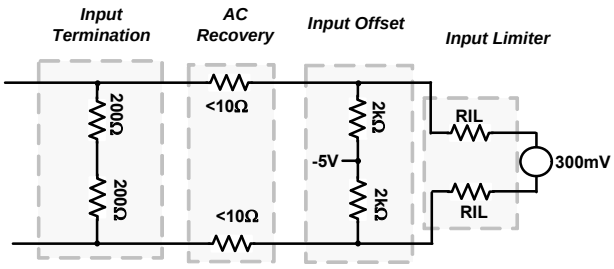

FIGURE 24. EQUIVALENT INPUT IMPEDANCE NETWORK

Equivalent Input Impedance (Figure 25)

Looking in is 400Ω across the input and in parallel with $2R_{IL}$. The 4k are common impedance and using the rule of thumb (10:1), the impact of the 4k can be ignored. This input network impedance needs to look like 120Ω across the input to properly terminate the Cat-5 cable. We also want to insure the maximum signal amplitude is developed at the input to the EL5175.

$$120\Omega = (400\Omega \parallel 2R_{IL}) \quad \text{(EQ. 12)}$$

where: R_{IL} = 69Ω

The HF large signal impedance model would appear as 100Ω across the output of the Cat-5 cable.

EL5175 - Cat-5 Cable Disconnected Considerations

INPUT 'OPEN CABLE' OFFSET, (FIGURE 25)

What happens when the input cable is disconnected and the circuit is set up as an RS-485 receiver mode or both ends of the cable are in receiver mode? The inputs to the EL5175, theoretically under ideal conditions, will be a delta of 0V. Having the input to the network floating, my induce conditions where the EL5175 output will oscillating. We need to fix the input to a level to prevent any possible instability.

We need to offset one of the input legs enough but not so we exceed the CMV limits of the EL5175. Since the lower leg diode to ground places the lower leg at -0.3V and we have a series 1kΩ and 2kΩ resistor to generate about 1.57mA current to -5V. A simple method is to place a small 10Ω resistor in series with negative input leg of ESD diode to ground. The EL5175 will have about -16mV differentially across it's input. Later on, you will find that a negative differential input will generate a -0.6V on the EL5175 outputs. Thus, we have the EL5175 in a known state.

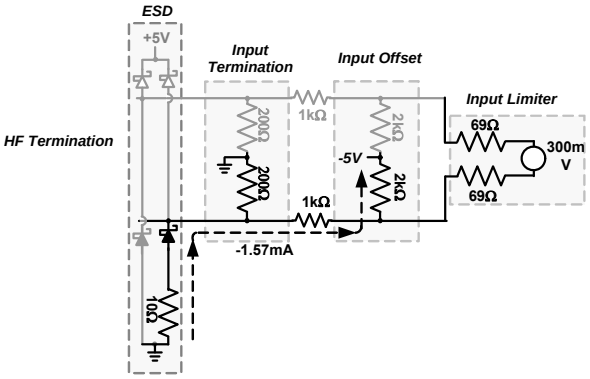

FIGURE 25. INPUT OPEN CABLE OFFSET

Complete Input Network (Figure 26)

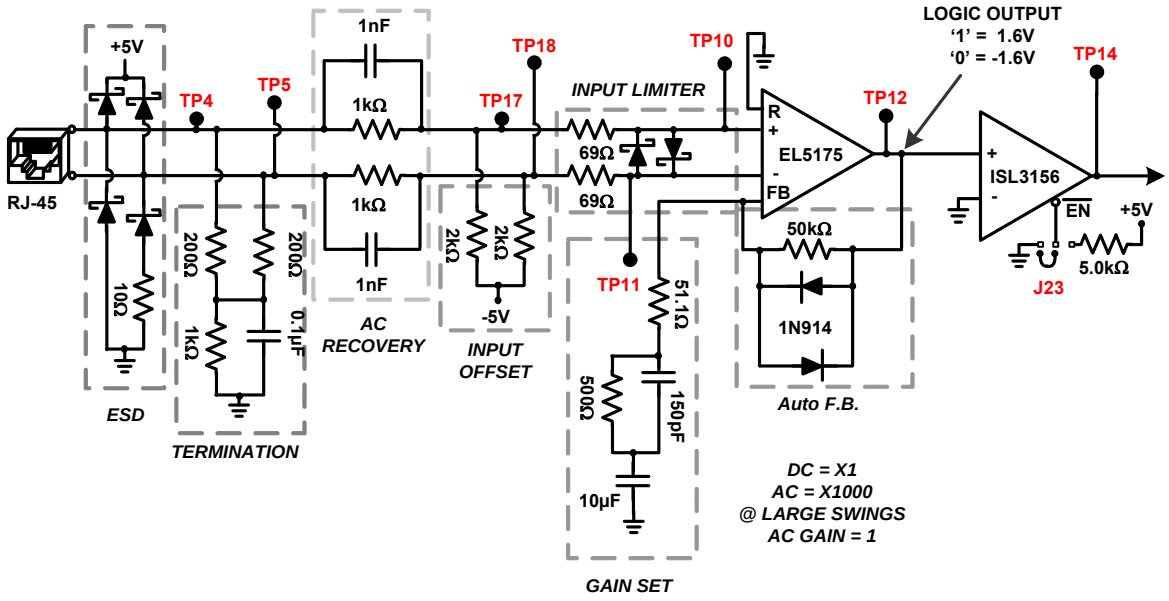

FIGURE 26. COMPLETE POINT-POINT INPUT NETWORK

Now we have the signal properly terminated and the ESD protection for the receiver. We have reduced any common mode low and high frequency elements. The input zero point has been adjusted to ground while allowing high speed low level edges to bypass the input voltage divider. We have also insured the EL5175's inputs are not driven into saturation while reducing the side effect of the input limiter's impedance generating reflected waves.

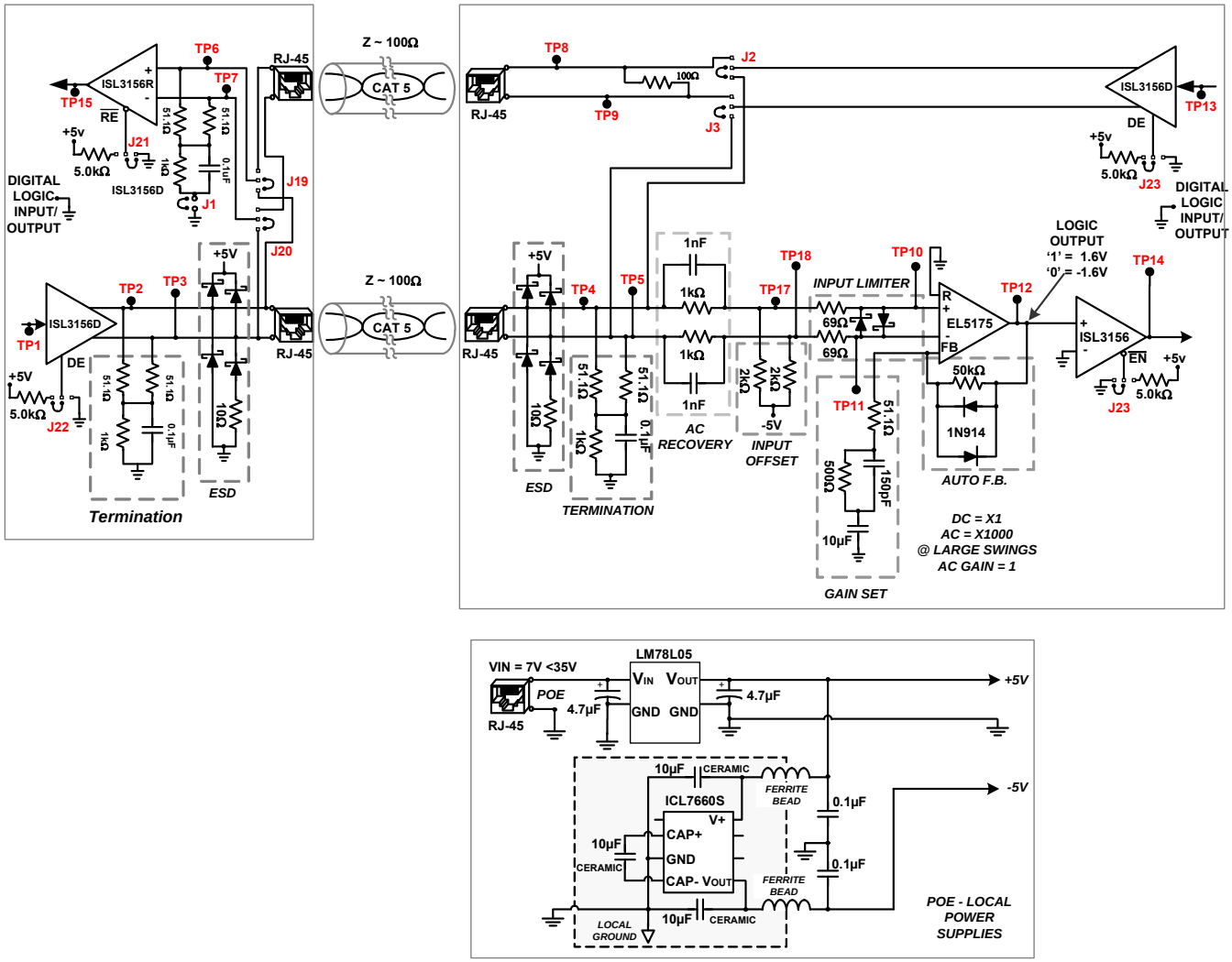

FIGURE 27. COMPLETE POINT-TO-POINT RS485 TRANSCEIVER DESIGN

Summary

If you need the maximum distance, Point-to-Point design will support up to 1 mile at 1MBbps with 15% Jitter. If you need to have point to multipoint, then you are limited to 4kft at 1Mbps. Yet, in both cases, if you can tolerate higher levels of jitter, you can push the distance out without any special jitter recovery circuitry.

An applications where this would be very useful is in security cameras. You can make use this application note and a second wire pair for two way digital controls. Also, making us of POE, you can use this design to extend the range but noise and jitter are additive and will be the limiting factor.

Point to Point Test Results

Figure 28 is an EYE diagram for 1MHz at a Cat-5 cable length of 3,245 feet with the threshold at 0.8V and 2.0V.

Figure 29 is that of an EYE diagram at the output for a 1MHz digital input viewed at 5,248 ft. Note: This design is able to support a 1MHz digital signal with only 15% jitter at a distance of >5000 ft.

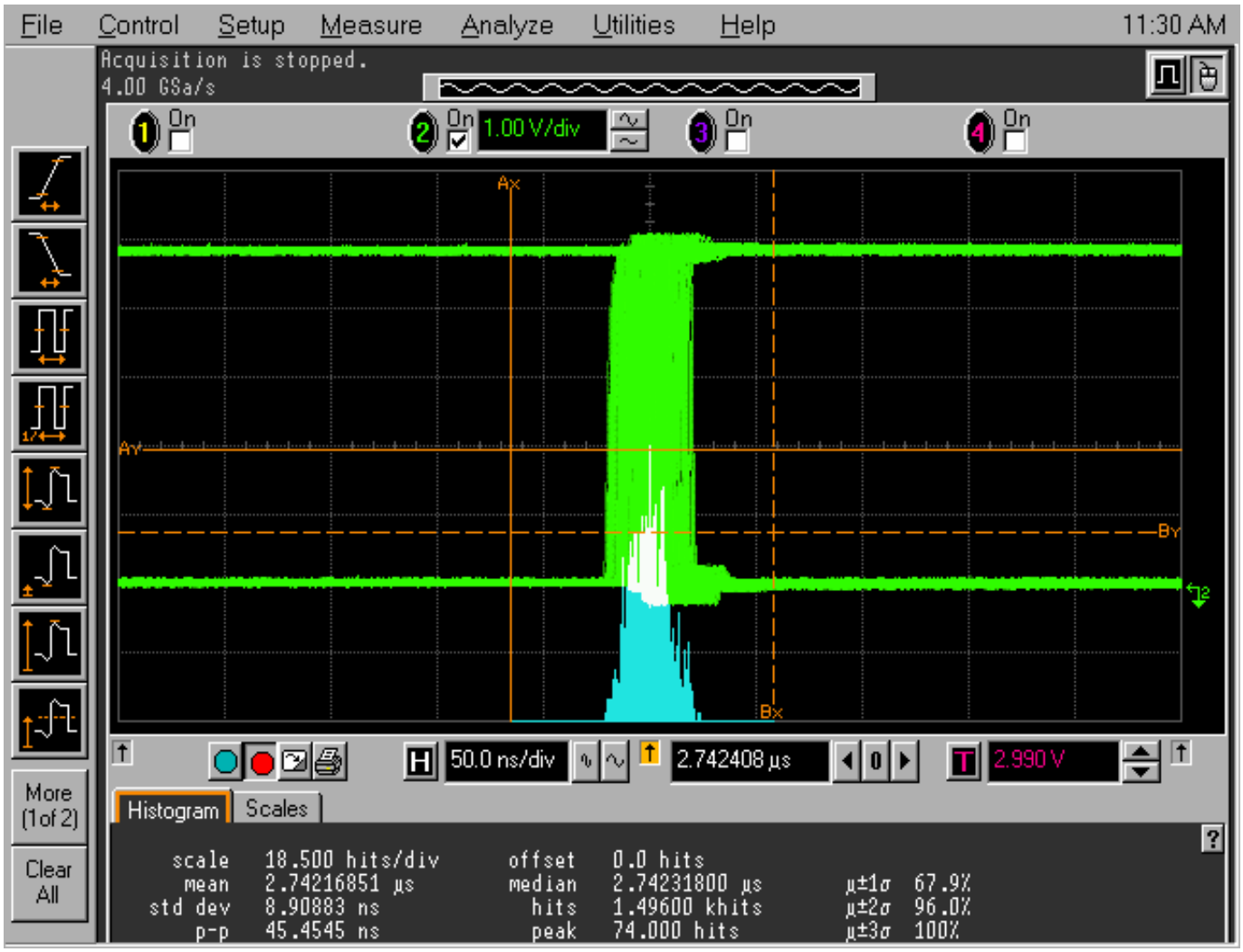

FIGURE 28. EYE DIAGRAM - 1HMz @ 3245 FEET

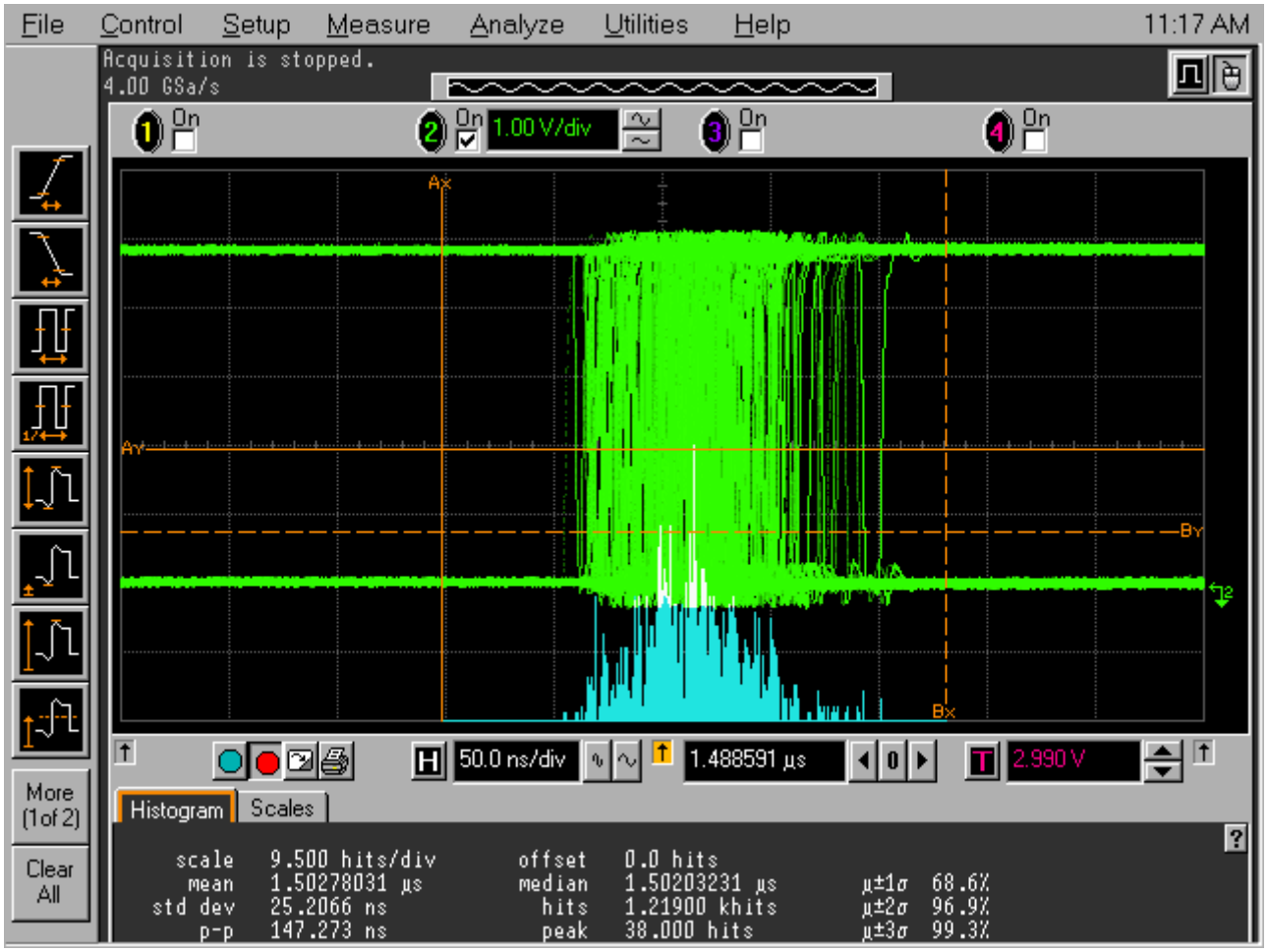

FIGURE 29. EYE DIAGRAM - 1HMz @ 5248 FEET

PCB Layout and Top/Bottom Layers

The PCB layouts are for the point-to-point solution but can be easily adapted for use in a point-to-multipoint application without needing a layout change, just component value changes:

Change from Point-to-Point to Point-to-Multipoint

1. Remove R_{11} (1kΩ on the input to ground).
2. Change the value of C3 from 0.1µF to 4.7µF.
3. Change the input termination resistors, R_{12} and R_{13}, from 51Ω to 2kΩ.
4. Change the Input Offset Network, R_{17} and R_{28} from 2kΩ to 20kΩ.
5. Change the Input Limiter network, R_{19} and R_{20} from 69Ω to 62Ω.
6. Moved the four ESD diodes to just after the RG-45 Cat-5 cable connector.

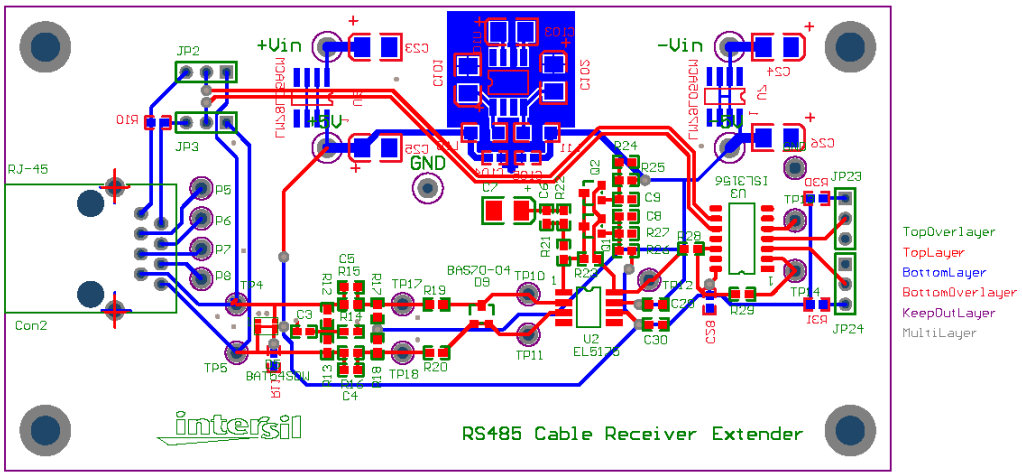

FIGURE 30. PCB LAYOUT SILK SCREEN TOP LAYER

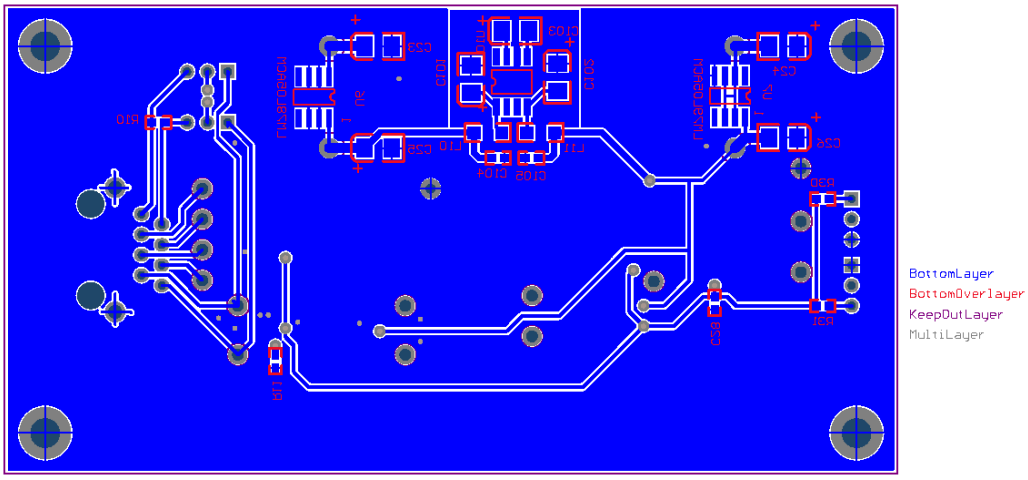

FIGURE 31. PCB BOTTOM LAYER

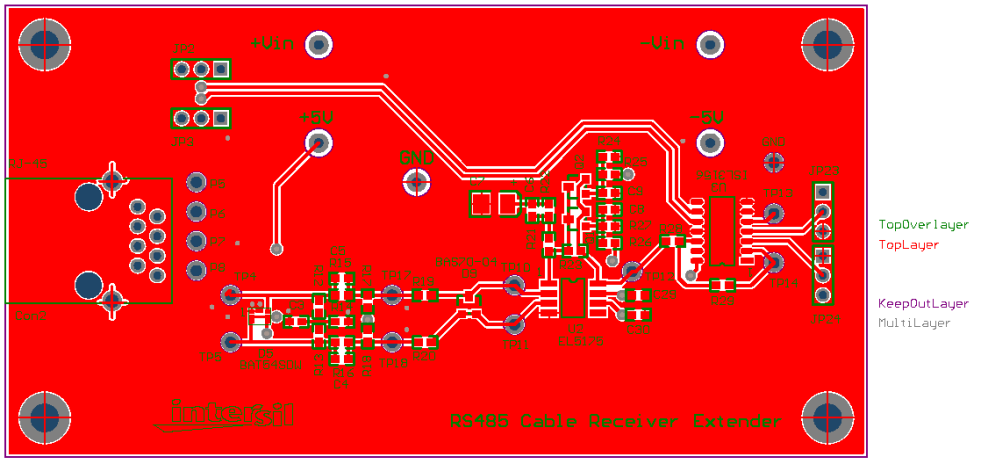

FIGURE 32. PCB TOP LAYER

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