A Primer on Renesas Digitally Controlled Potentiometers (XDCPs)

Introduction

This application note provides the fundamentals of the operation and application of Renesas digitally controlled potentiometers (XDCPs).

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1. Operation and Application

Figure 1 shows the schematic symbol of the potentiometer is a three-terminal variable, resistance-like device.

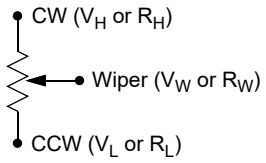


Figure 1. Schematic Symbol of the Potentiometer

There are two types of potentiometers: mechanical and electronic. The terminals of the mechanical potentiometer are called CW (clockwise), CCW (counter clockwise), and wiper. The corresponding names or designations for the terminals of the electronic version are VH or RH, VL or RL, and the wiper VW or RW. The mechanical potentiometer is a three-terminal device, and the electronic potentiometer is an integrated circuit with a minimum of eight terminals.

The Renesas digitally controlled potentiometer (XDCP) is an electronic potentiometer that controls the wiper position using digital control signals. The electronic version of the potentiometer has memory to store the wiper settings and data.

The XDCP is a system-level control device performing a component-level function.

Figure 2 shows the block diagram of a typical XDCP.

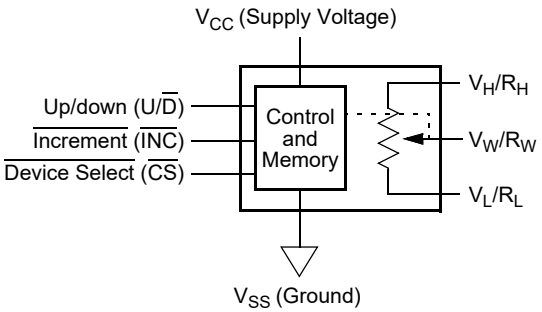


Figure 2. Block Diagram of the Digitally Controlled Potentiometer

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The CMOS implements the control and memory section of the device and is biased with a 3V or 5V digital or logic supply. Three different serial buses can control the device; (1) three-wire, (2) two-wire similar to I^2C, and (3) serial peripheral interface (SPI). The control signals for the three-wire bus are up/down, increment, and device select. The up/down control input is a level-sensitive signal that establishes the direction of the movement of the wiper. The wiper moves on the falling edge of the increment control input in the direction established by the up/down signal. The device select control input is an address line that enables or disables the device. The control inputs for the two-wire bus are clock (SCL), a bidirectional serial data line (SDA), and address lines (ADDR). The control inputs for the SPI bus are clock (SCK), serial in (SI) and serial out (SO) data lines, and address lines (ADDR). This application note explains the protocols of the two-wire and SPI serial interfaces.

Figure 3 shows the implementation of the integrated circuit of the digitally controlled potentiometer. Polycrystalline resistors connect in series between the RH and RL terminals, and solid-state switches implemented by nMOS or CMOS transistors connect at each end of this resistor array and between the resistors. The switches are equivalent to a single-pole, single-throw switch. One end of all the switches are tied together and are connected to the wiper terminal. Only one switch is closed at a time connecting a node in the series resistor array to the wiper. The resistors are polycrystalline silicon deposited on an oxide layer to insulate them from the other circuitry.

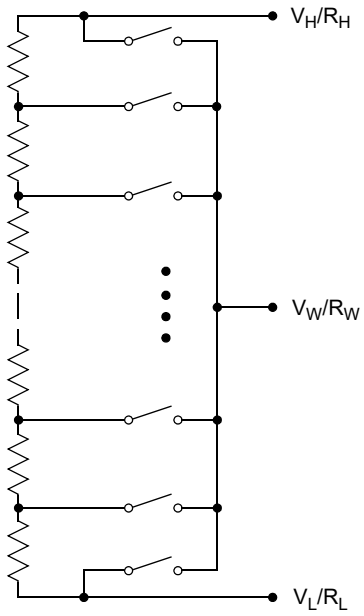


Figure 3. Implementation of the Electronic Potentiometer

The potentiometer can be used in application circuits as either a three-terminal device or a two-terminal device. The most common way to use the potentiometer as a three-terminal device is as a voltage divider circuit (Figure 4). Positive and/or negative voltages are connected across the potentiometer. As the wiper goes from one voltage limit to the other. the wiper is moved from the low-to-high terminals. In many applications, this circuit can be substituted for a digital-to-analog converter because it performs a digital-input, analog-output function.

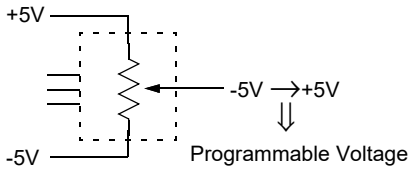


Figure 4. Three-Terminal Configuration and Application

The XDCP can be used as a two-terminal variable resistor. Figure 5 shows the configuration where the potentiometer functions as a variable resistor and varies the current through the LED because the voltage across the potentiometer is relatively constant.

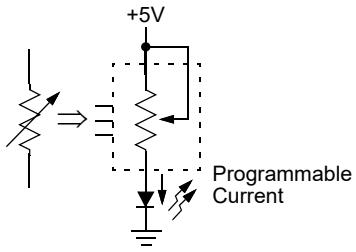


Figure 5. Two-Terminal Configuration and Application

The two basic applications illustrate the use of the digitally controlled potentiometer in a digital-to-analog voltage circuit and in a digital-to-analog current circuit.

Figure 6 expands the block diagram of the XDCP to include the internal registers and data paths. The output of the volatile wiper counter register (WCR) determines the position of the wiper by closing a switch connecting the wiper terminal to a point in the resistor array. For the XDCPs with a two-wire or SPI bus, there are four nonvolatile data registers (R0 to R3) that can be used to store data or additional wiper settings. The wiper counter and data registers can be programmed from the bus or can transfer data between the registers through the instruction set of the device. Data register R0 stores the wiper setting for the power-up sequence. Each XDCPs with a three-wire interface has only one internal nonvolatile register per potentiometer that stores the wiper setting for restoration during the power-up sequence.

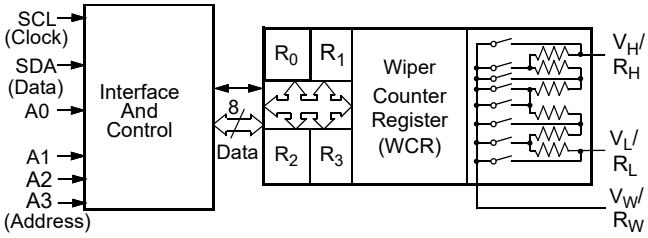


Figure 6. XDCP System Control and Registers

The XDCPs with a two-wire (I^2C) or SPI serial bus have an instruction set. Figure 7 lists the instructions and Figure 8 shows the bit structure. The instructions control the flow of data internally or through the bus, the increment/decrement feature, and some specialized commands. The global transfer command transfers data between registers in devices with multiple potentiometers and the write in progress (WIP) instruction monitors the completion of the nonvolatile write process.

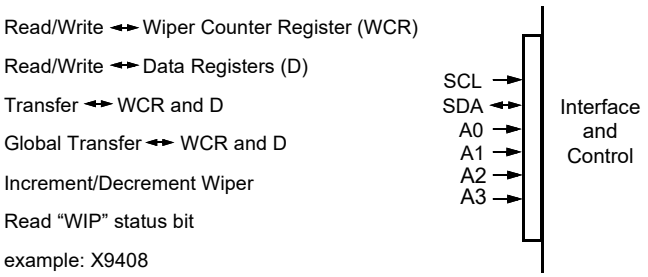


Figure 7. Instruction Set

Write Wiper Counter Register (WCR)

S T A R T	device type identifier				device addresses				S A C K	instruction opcode				wiper addresses				S A C K	wiper position (sent by master on SDA)								S A C K	S T O P
	0	1	0	1	A 3	A 2	A 1	A 0		1	0	1	0	0	0	P1	P0		0	0	W P 5	W P 4	W P 3	W P 2	W P 1	W P 0		

Figure 8. Bit Structure

Renesas digitally controlled potentiometers come with active devices like operational amplifiers and comparators. Figure 9 shows the block diagram of the dual-potentiometer, dual-op amp device.

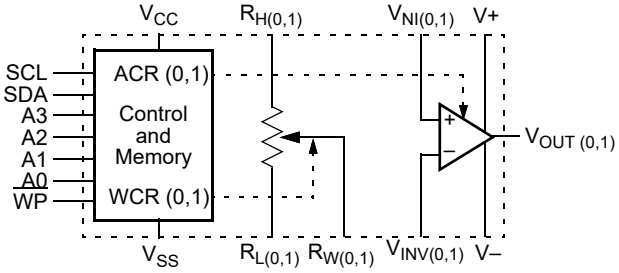


Figure 9. Potentiometer and Operational Amplifier

The terminals of both the potentiometer and the op amp are brought out to accommodate all possible configurations. The externally connected analog supplies, V+ and V-, power the op amp. The WCR programs the location of the wiper of the potentiometer, and the Analog Control Register (ACR) programs features of the operational amplifier.

The analog datasheet parameters reflect the limitations of the digitally controlled potentiometer. The key analog datasheet parameters are number of taps, end-to-end resistance, maximum voltages on the potentiometer pins, wiper resistance and current, power rating, resolution, noise, linearity, and temperature coefficient. Table 1 lists the datasheet parameters and their values for a typical XDCP.

The number of taps in a potentiometer varies from 16 to 256 and reflects the resolution of the device or its ability to select one of n tap positions. The end-to-end resistance (RH to RL) of the potentiometer is R_{TOTAL} and comes in 1k¾ to 1M¾ values. The voltage VCC, 3 to 5V, provides the voltage biasing for the digital control and memory section and V+ and V- provide the voltage biasing for the analog section. The voltages $V_{TERMINAL}$ are the maximum voltages, ±5V to +15V, that can be applied to the potentiometer pins in their application. Wiper resistance, nominally 40W, models the resistance RDS(on) of the MOSFET switches used to connect the wiper terminal to a node in the resistor array. The wiper current spec, 1mA to 3mA, limits the maximum amount of current allowed through the wiper switches. Absolute linearity describes the difference between the actual and expected wiper voltage when the device is used as a voltage divider, and is accurate within one least significant bit or minimum increment (MI). Relative linearity describes the tap-to-tap accuracy that is 0.2 of an LSB or MI. The potentiometer has a maximum power rating between 10mW and 50mW. Two parameters describe the temperature dependence of R_{TOTAL} and the resistances in the series array. R^{TOTAL} TC (temperature coefficient) is a nominal 300ppm/°C and the ratiometric TC is within 20ppm/°C.

While the datasheet parameters reflect the performance limitations of the digitally controlled potentiometer, there are a large number of circuit techniques that minimize these limitations. Renesas application notes and technical briefs describe these techniques and are available on the Renesas website. These publications describe numerous possible applications.

2. Analog Characteristics

Unless otherwise stated, specifications apply over the recommended operating conditions.

Table 1. Analog Datasheet Parameters

Symbol	Parameter		Limits				Test Conditions
			Min.	Typ.	Max.	Units	
R_{TOTAL}	End-to-End Resistance		-20	-	+20	%	
	Power Rating		-	-	50	mW	25°C, each pot
I_W	Wiper Current		-3	-	+3	mA	-
R_W	Wiper Resistance		-	40	100	Ω	V_{CC} = 5V, I_W = ±1mA
			-	150	250		V_{CC} = 2.7-5.5V, I_W = ±1mA
Vv+	Voltage on V+ Pin	X9410	+4.5	-	+5.5	V	-
		X9410-2.7	+2.7	-	+5.5		
Vv-	Voltage on V- Pin	X9410	-5.5	-	-4.5	V	-
		X9410-2.7	-5.5	-	-2.7		
V_{TERM}	Voltage on any V_H or V_L Pin		V-	-	V+	V	-
-	Noise		-	-140	-	dBV	Ref: 1kHz
-	Resolution[1]		-	1.6	-	%	-
-	Absolute Linearity[2]		-1	-	+1	MI	$V_{w(n)(actual)} - V_{w(n)(expected)}$
-	Relative Linearity[3]		-0.2	-	+0.2	MI[4]	$V_{w(n+1)} - [V_{w(n)} + MI]$
-	Temperature Coefficient of R_{TOTAL}		-	±300	-	ppm/°C	-
-	Ratiometric Temp. Coefficient		-	-	20	ppm/°C	-

1. Individual array resolution.
2. Absolute linearity determines the actual wiper voltage versus expected voltage as determined by the wiper position when used as a potentiometer.
3. Relative linearity determines the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
4. MI = RTOT/63 or (VH – VL)/63, single pot.

3. Revision History

Revision	Date	Description
1.00	Nov 6, 2026	▪ Applied the latest template ▪ Added Revision History section
0.00	Jun 7, 2005	Initial release

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