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Designing with Intersil Digitally Controlled Potentiometers (XDCPs)

Introduction

The use of Intersil's nonvolatile digital potentiometers (XDCPs) can simplify and/or solve many mixed signal design problems. However, in some applications, a deeper understanding of XDCP technology may be required during the design process. In this note, additional information is provided relating to resolution, wiper noise, temperature coefficients, wiper current limitations, wiper leakage current, terminal voltage limitations, independent linearity, frequency response, hysteresis, reliability failure rates, and logarithmic tapers. A summary of available XDCPs and associated parameters is also included to aid the designer in choosing the correct device. Using the information and tips provided, a designer should be able to overcome most design problems that could be encountered.

Resolution

Simply put, the resolution of a potentiometer is a measure of the difference between adjacent tap positions. In a ratiometric application, this would correspond to a voltage step, whereas in resistive applications, the resolution more closely corresponds to an incremental resistance. A theoretical resolution can be defined as a measurement of the sensitivity to which the output ratio may be adjusted and is equivalent to the reciprocal of the number of taps (neglecting tap zero) expressed as a percentage. The precision with which this can be set is often called the adjustability or setability. On standard XDCPs, either 256, 124, 32, or 16 taps are available to the hardware designer, providing resolutions of 1.01%, 1.59%, and 3.23% respectively. These resolutions are approximately constant from tap to tap (though the relative linearity is more conservatively specified to be 20%) and the potentiometer exhibits monotonic behavior as the wiper is moved. With quad devices (i.e. X9241A), internal cascading can be implemented with software commands, allowing up to 253 taps (0.39% resolution). On the newer generation XDCPs, even higher resolutions will be possible using dual 128 tap and dual 256 tap devices. However, with standard XDCPs, extremely high resolutions are already possible with external hardware or the use of certain software schemes (See Intersil application note AN43 “Software Implements a High Resolution Nonvolatile Digital Potentiometer”). A similar analysis will hold for XDCPs connected as rheostats, however it should be noted that there will always be a small MOSFET channel resistance in series with the wiper terminal, due to the NMOS wiper transistor switch, which limits the minimum possible resistance in those applications. This wiper resistance can even manifest itself to a lesser extent in ratiometric applications by adding a term to the voltage divider expression. A simple formula to determine the channel resistance of these long channel wiper transistors (operated in the triode region) is given in *Eq. (1)*, along with the conditions for the triode region of operation in *Eq. (2)*.

(EQ. 1)

$$R_{DS} = \left[\left(\frac{\mu\varepsilon}{t_{OX}}\right)\left(\frac{W}{L}\right)(V_{GS} - V_t)\right]^{-1}$$

(EQ. 2)

$$(V_{GS} - V_t) > V_{DS} > 0$$

It can be seen from *Eq. (1)* that the MOSFET channel resistance is inversely proportional to VGS. Since the source of the transistor is connected to the wiper terminal (which can have a varying voltage), the gate voltage of the wiper transistor in an XDCP must be maintained at a high enough voltage to guarantee operation in the triode region. Internally, this is accomplished with another charge pump (which generates between 10V and 18V depending on tap position and device). With appropriate substitutions, this resistance can be estimated from *Eq. (3)* with VW as the wiper voltage in volts and T in degrees Celsius, using the parameters from the chart in Figure 4 of this note.

(EQ. 3)

$$R_W = [K_1]V_W + K_2$$

Nominally, this resistance is 40Ω, but it increases as temperature increases and has been measured to be as high as 90Ω over the industrial temperature range (-40°C to +85°C). The voltage drop across this wiper transistor is equal to V_{DS} and can be approximated for various wiper currents using *Eq. (4)*, which is an equation for IDS of a MOSFET operated in the triode region.

(EQ. 4)

$$I_{DS} = \left(\frac{\mu\varepsilon}{t_{OX}}\right)\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{(V_{DS})^2}{2}\right]$$

Using some substitutions based upon Intersil process and design parameters, this equation reduces to the expression in *Eq. (5)*, where V_{DS} is in units of volts.

(EQ. 5)

$$I_{W(mA)} = (49.5 - 3.3V_{DS})(V_{DS})$$

Resolutions can also be expressed in terms of dynamic range (DR). At approximately 6dB/bit, a 100 tap XDCP has an equivalent DR of 39dB. Similarly, DRs of 36dB and 30dB exist for the 64 and 32 tap XDCPs respectively.

Wiper Noise

An EEPROM cell requires a high voltage to initiate Fowler-Nordheim tunneling, the phenomenon upon which much of

the industry bases its EEPROM technology. In order to generate such voltages (as high as 18V), Intersil devices use an internal charge pump. There are other aspects of Intersil's process that also require the use of charge pumps (e.g. to provide a negative substrate bias for the IC die). For each charge pump, there must necessarily be an associated oscillator. It is these oscillators which contribute high frequency noise to signals on the wiper of the potentiometer. However, with knowledge of the cutoff frequency and internal oscillator frequencies of a particular XDCP, this effect can be minimized.

The most direct solution is to add a first order lowpass filter to the wiper terminal in order to attenuate all of these unwanted frequencies. Since there is a wiper resistance (*Eq. (1)*) associated with every XDCP, simply connecting a capacitor between the wiper and V_{SS} will implement a passive RC filter. This wiper resistance varies due to loading and temperature, so a more accurate way of connecting an RC lowpass filter is to add a known resistance in series with the wiper and use that value for calculating the size of the wiper capacitor. Using *Eq. (6)* and the information in Table 1, the appropriate value for the capacitor can be determined for either technique.

(EQ. 6)

$$f(Hz) = \frac{159 \times 10^3}{RC}$$

The units for *Eq. (6)* are Hz, Ω, and µF. Typically, a low cost, 20% monolithic capacitor of appropriate size connected between the wiper terminal and V_{SS} is sufficient to significantly attenuate the charge pump noise contribution. For example, with a X9C103, which has a
-3dB frequency of 300KHz and an oscillator frequency of 2.5MHz, an approximate wiper capacitor is calculated to be between 0.013µF and 0.0016µF, assuming a wiper resistance of 40Ω. By choosing a 0.013µF capacitance, the wiper noise would be attenuated by -23dB compared to an unfiltered wiper. Unrelated to the charge pump are other inherent noise sources common to all CMOS devices. In particular, XDCPs exhibit both thermal and flicker noise components. Overall, Intersil specifies a noise for an XDCP which is equivalent to 1µV per square root Hz. An estimate of the total wiper noise from all sources in the XDCP can be obtained from *Eq. (7)*

(EQ. 7)

$$\text{noise amplitude}(\mu V_{p-p}) \leq (6.6\mu V_{p-p})[\sqrt{f}]$$

Where f (in Hz) is the bandwidth of interest for signals on the wiper, the result is a magnitude of peak to peak noise superimposed on the wiper voltage.

Temperature Coefficients

Often, the performance of a circuit over temperature is a crucial design consideration. For this reason, Intersil XDCPs contain a unique compensation scheme to minimize the resistive drifts due to temperature variations. The principle here is similar to the operation of circuitry in a low drift voltage reference. In those references, different active devices (Zener diodes, BJTs, MOSFETs, etc.) have differing parameter drifts over temperature. By combining those that have negatively sloped drifts with those that have positively sloped drifts, in the right configuration, an output voltage drift can be held “flat” over the temperature range of interest. Though XDCPs, utilize an entirely different implementation (i.e. there are no active elements), the principle is the same. This can be very important when a highly accurate bias voltage needs to be maintained over extreme temperature swings. In *Eq. (8)*, the standard definition for a temperature coefficient is given in equation form.

(EQ. 8)

$$TC(ppm/°C) = \left[\frac{(R_1 - R_2)}{R_1(T_2 - T_1)}\right](10^6)$$

The temperature coefficient expresses a resistive drift in parts per million per degree centigrade, where R_1 is the resistance at reference temperature T_1 and R_2 is the resistance at the test temperature T_2. For XDCPs, the ratiometric temperature coefficients are good (at 20-30 ppm/°C) due to the resistor ladder structure, however the end-to-end resistance temperature coefficients are typically an order of magnitude or more higher.

Wiper Current Limitations

An important specification on XDCPs is the 1mA wiper current limit. However, the motivation behind this specification is primarily historical. On Intersil's older NMOS processes, the 1mA limit was required due to electromigration concerns with the metallization process. This was an industry wide reliability concern that sparked considerable research several years ago. For semiconductor devices, high currents, coupled with small cross-sectional areas for aluminum metal lines, can lead to early device failures due to the migration of the Al ions. These failures often occur as open circuits (and occasionally short circuits) on the IC itself. Since the electromigration issue relates to long term reliability, the concern here is to avoid continuous operation in a mode that could lead to a failure, consequently DC current levels are of primary concern. An expression for the predicted mean time before a failure is given by *Eq. (9)*.

(EQ. 9)

$$MTBF = \frac{1}{J^2}\exp\left(\frac{-E_a}{kT}\right)$$

This Arhennius relationship expresses how strongly related electromigration failures and current densities are on a chip. The exponential dependence upon temperature is exhibited as well. The constant of proportionality can be determined by experimentation, assuming an average E_a of 0.44eV. Notice that a tripling of current density anywhere that electromigration exists will reduce the MTBF nine-fold! Though these effects have not been entirely eliminated, good design as well as the use of several fabrication tricks have made electromigration less problematic than it once was. In order to make the newer CMOS parts as compatible as possible to existing NMOS parts, this 1mA limit, which has always been related to long term reliability, was also adopted. Though Intersil now adds copper ions to the aluminum metallization to improve reliability, this 1mA limit has been retained. A more realistic, yet still conservative DC wiper current limit for the CMOS devices would be on the order of 3.5mA.

When larger currents must be controlled, many techniques can be used to boost the current supplied by a given wiper voltage. A straightforward and practical example would use the buffering voltage follower op amp configuration in Figure 1. If the current gain of the op amp is too small, then additional gain stages could also be added on the output of the op amp. A wiper capacitor is shown here to diminish wiper noise on the op amp input. However, there are many other possible circuits to accomplish current gains for the XDCP wiper currents.

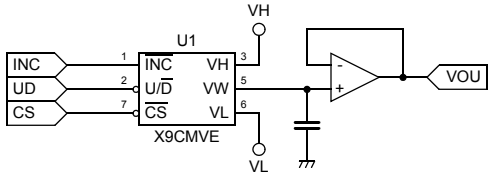

FIGURE 1. VOLTAGE FOLLOWER TO INCREASE OUTPUT CURRENT

Wiper Leakage Current

On XDCPs which have differing f_{OSC1}, f_{OSC2}, and f_{OSC3} oscillator frequencies (See Table 1), slight voltage changes can appear on the wiper terminal depending on the whether $\overline{CS}$ is asserted or not (or whenever a nonvolatile store is being performed). This has often been misinterpreted as a DC leakage current, however, this is not the case. The phenomenon that is actually being observed is the body effect, an inherent MOSFET mechanism which modulates a transistor's threshold voltage whenever the voltage between the bulk and the source is not exactly zero (i.e. $|V_{BS}| \neq 0$). Since the bulk (substrate) potential of an XDCP die is charge pumped down to a negative substrate voltage (V_{BB}), fluctuations in this substrate voltage will alter V_{BS}, thus changing the threshold voltage as well. *Eq. (10)* shows this relationship.

(EQ. 10)

$$V_t = V_{t0} + \gamma\left[\sqrt{(\phi_s + |V_{BS}|)} + \phi_s\right]$$

Here, g is a process parameter that is generally between 0.5 and 2 for any particular semiconductor manufacturer. This effect can cause $\Delta VW \approx 5mV$ to 10mV in the worst case scenarios. Returning $\overline{CS}$ to the previous level will remove DVW from the wiper as well.

Terminal Voltage Limitations

Occasionally there is a need for a higher or lower tolerance on the terminal voltages of an XDCP. On typical devices, the limit is ±5V with respect to V_{SS}, however on the X9312, a range between V_{SS} and +15V is allowed. The issue limiting the terminal voltages has to do with specific breakdown mechanisms in the MOSFET structure. As the wiper decode logic attempts to maintain a steady voltage across the gate and source of the transistor, any increase in the voltage at the source must result in an increase of the voltage applied at the gate. Beyond a certain level, PN junction breakdown occurs. By limiting the voltages allowed at the source, as well as preventing the decode circuitry from generating excessive voltages, this breakdown can be avoided. Unfortunately, this limits the voltages allowed on the terminals (V_H and V_L). Since expansion of this range is limited by design and process considerations, external techniques must be employed to accomplish this task. Figure 2 shows a simple configuration that can generate an output voltage with a larger swing than that from an individual XDCP. In this circuit, current gain can also be realized depending on the output of the op amp. Also, another technique is shown for reducing wiper noise. Here the capacitor is attached across the input terminals of a non-inverting op amp scheme.

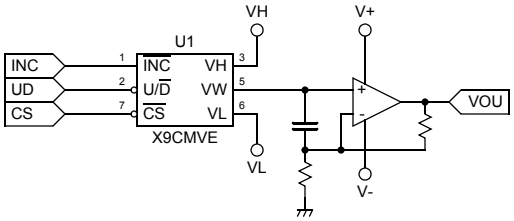

FIGURE 2. OP AMP CIRCUIT TO INCREASE OUTPUT VOLTAGE RANGE

Independent Linearity

With potentiometers, independent linearity is defined to be the maximum deviation from ideal behavior, expressed as a percentage of the voltage applied across the terminals. With XDCPs, similar information can be obtained using the absolute

linearity specification. For this measurement, Intersil refers to a minimum increment (MI) unit that is defined in *Eq. (11)*.

(EQ. 11)

$$\frac{V_H - V_L}{\#TAPS - 1} = 1\ MI$$

Converting this absolute linearity specification (*Eq. (12)*) into an independent linearity, it is seen that all 100 tap XDCPs exhibit a 1.01% independent linearity.

(EQ. 12)

$$V_{W(actual)} - V_{W(expected)} \leq \pm 1\ MI \leq \pm 1\ LSB$$

From these definitions, equivalent INL (integral non-linearity) and DNL (differential non-linearity) can be determined for XDCPs. The INL is 1 LSB and the DNL is 0.2 LSB.

Frequency Response

The frequency response of any XDCP will be limited by the response of its RC time constant. Intersil characterizes a typical -3dB point ($^1/_2$ power point) for a given end-to-end resistance by taking measurements when the wiper is set to a mid-range tap position. Due to variations in the end-to-end resistance of a given device (Intersil specifies ±20% on this parameter) and the likelihood that useful circuits will require tap settings outside of mid-range, the frequency response of an XDCP will show some variance. However, for any fixed tap position, this -3dB point exhibits little dependence on fluctuations in V_{cc} and sub or temperature.

For tap positions other than mid-range, estimations for the frequency response can be carried out assuming between 90pF and 110pF for the total wiper capacitance to ground. Remember that the end-to-end resistance will vary from device to device, thus, in critical designs the appropriate error margins must be considered. In the case of the logarithmic taper XDCPs, the mid-range tap positions do not correspond to mid-range of the end-to-end resistance.

Hysteresis

One interesting quirk in the behavior of mechanical potentiometers is that there is a sort of “hysteresis” effect on the wiper voltage when changing wiper positions. The potentiometer’s electrical characteristics won’t change until a certain amount of mechanical travel has occurred by the knob. This results in a “lurching” behavior that makes fine trimming rather tedious. With Intersil’s digital potentiometers, this behavior is entirely avoided. Another measure of hysteresis would be the change in output voltage at a certain wiper tap when the wiper is moved to either full scale (or zero scale) and then returned to the original tap position. Since Intersil devices are strictly monotonic and avoid the mechanical behavior of traditional potentiometers, any movement of the wiper will result in a change to the wiper voltage and for any movement from an initial tap position to other tap positions and back to the initial tap position, it can be observed that XDCPs exhibit no hysteresis effects (i.e. the wiper returns precisely to the same voltage).

Reliability Failure Rates

With or without a knowledge of the number of transistors on a die, an MTBF can be calculated to determine the average lifetime of an IC. For the X9CMME family of XDCPs, internal qualification data has yielded an MTBF of 2154 years based on the number of failures (0 out of 353) during a 1000 hour dynamic life test at 150°C. This data could also be expressed as 53 FITs at 55°C for a 60% upper confidence limit. The number of FITs is equivalent to the number of failures per billion device hours (See Intersil reliability reports RR-520 and RR-515 for a more complete explanation of the FITs parameter). This data helps predict the reliability of the standard logic on an XDCP, but similar results would be obtained for the charge pump and EEPROM cell circuitry. However, some electromigration failures might occur on the resistor chain before anything else on the IC fails, particularly if the 1mA limit is not strictly observed. The exact lifetimes for various wiper current loads are not explicitly known, however similar results will be obtained in a reliability analysis for any of Intersil's XDCPs.

NMOS and CMOS XDCP Differences

Intersil introduced the first XDCPs in 1984 using an NMOS technology. When these devices were replaced by CMOS designs, an extra standby current mode was added that allowed for the power savings benefits of CMOS circuitry. To implement this extra mode, a NOR gate was added between the $\overline{CS}$ and $\overline{INC}$ inputs. When the output of this NOR gate is HIGH, the wiper transistor decoder is enabled and the wiper position can be moved. Consequently on power-up, if both of these pins are held LOW, then the wiper position will be recalled from the EEPROM and the wiper will move one additional position depending on the state of the U/$\overline{D}$ pin. Subsequent movements require that the output of this gate see a rising edge, thus either $\overline{CS}$ or $\overline{INC}$ must be “clocked” in order for the wiper to be moved any further. This behavior can cause the power-up wiper positions to be off by one tap position if precautions are not taken. The standby power mode is available on all CMOS XDCPs. Another difference that exists between the NMOS wiper and CMOS wiper XDCPs is the length of time it takes to de-select the previous wiper position and select the new wiper position, when changing taps. Because the switching of these FETs works in a “make-before-break” mode, the use of NMOS wiper XDCPs in certain audio configurations may require extra precautions to avoid audible “clicking” sounds on the speaker while the wiper position is being adjusted. The differing device technologies are summarized in Table 2 along with several other pertinent parameters.

Logarithmic Tapers

With some XDCPs, the option to have a logarithmic taper instead of a linear taper exists. The logarithmic version of the X9313 is the X9314. Currently, these devices are available in 1kΩ, 10kΩ, and 50kΩ end-to-end resistances. A typical logarithmic response is shown in Figure 3.

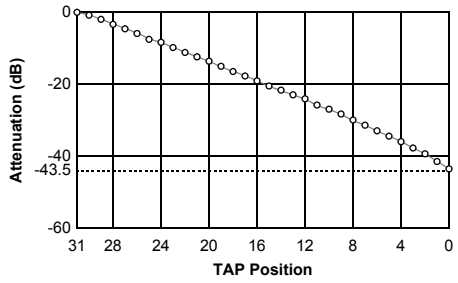

FIGURE 3. TYPICAL LOGARITHMIC TAPER RESPONSE OF AN X9514 OR X9314

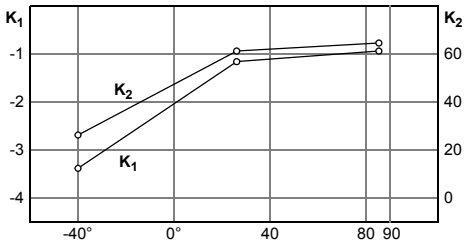

FIGURE 4. K1 AND K2 FOR USE IN EQUATION (1.3)

TABLE 1. XDCP PARAMETER SUMMARY (F_{OSC1} = $\overline{CS}$ LOW, F_{OSC2} = $\overline{CS}$ HIGH, F_{OSC3} = DURING NONVOLATILE STORE)

XDCP	F_{OSC1}	F_{OSC2}	F_{OSC3}	F_{-3DB}[1]	TAPS	V_H, V_L	R_{TOT}
X9C10[2]	2.5 MHz	2.5 MHz	2.5 MHz		100	±5V	1kΩ
X9C103[2]	2.5 MHz	2.5 MHz	2.5 MHz		100	±5V	10kΩ
X9C503[2]	2.5 MHz	2.5 MHz	2.5 MHz		100	±5V	50kΩ
X9C104[2]	2.5 MHz	2.5 MHz	2.5 MHz		100	±5V	100K
X9311Z[3]	5.0 MHz	5.0 MHz	5.0 MHz		100	+10V	1kΩ
X9311W[3]	5.0 MHz	5.0 MHz	5.0 MHz		100	+10V	10kΩ
X9311U[3]	5.0 MHz	5.0 MHz	5.0 MHz		100	+10V	50kΩ
X9311T[3]	5.0 MHz	5.0 MHz	5.0 MHz		100	+10V	100kΩ
X9312Z	2.5 MHz	2.5 MHz	5.0 MHz		100	+15V	1kΩ
X9312W	2.5 MHz	2.5 MHz	5.0 MHz		100	+15V	10kΩ
X9312U	2.5 MHz	2.5 MHz	5.0 MHz		100	+15V	50kΩ
X9312T	2.5 MHz	2.5 MHz	5.0 MHz		100	+15V	100kΩ
X9313Z	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	1kΩ
X9313W	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	10kΩ
X9313U	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	50kΩ
X9313T	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	100kΩ
X9314W	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	10kΩ, logtaper
X9315Z	N/A	N/A	5.0 MHz		32	+5V	1kΩ ext. voltage
X9315W	N/A	N/A	5.0 MHz		32	+5V	10kΩ ext. voltage
X9511Z	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	1kΩ
X9511W	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	10kΩ
X9514W	2.5 MHz	0.8 MHz	5.0 MHz		32	±5V	10kΩ, logtaper
X9221Y	2.0 MHz	2.0 MHz[4]	5.0 MHz		64	±5V	2kΩ, dual
X9221W	2.0 MHz[4]	2.0 MHz[4]	5.0 MHz		64	±5V	10kΩ, dual
X9221U	2.0 MHz[4]	2.0 MHz[4]	5.0 MHz		64	±5V	50kΩ, dual
X9241Y	2.0 MHz[4]	2.0 MHz[4]	5.0 MHz		64	±5V	2kΩ, quad
X9241W	2.0 MHz[4]	2.0 MHz[4]	5.0 MHz		64	±5V	10kΩ, quad
X9241U	2.0 MHz[4]	2.0 MHz[4]	5.0 MHz		64	±5V	50kΩ, quad
X9241M	2.0 MHz[4]	2.0 MHz[4]	5.0 MHz		64	±5V	combo, quad
X94xx family	N/A	N/A	5.0 MHz		64-256	±5V	SPI and I^2C ext. voltage

1. For more information on frequency response, see “Frequency Response Characteristics of Intersil’s Digitally-Controlled (XDW) Potentiometers” in Intersil’s Design Engineering Bulletin 26.
2. On older X9CMME devices, f_{OSC2} is 0.8MHz.
3. Obsolete part.
4. No $\overline{CS}$ on part, parameter is active at all times, except during nonvolatile stores.

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1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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