X4C105 NOVRAM Features and Applications

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Introduction

Have you ever experienced a power failure during a "save to disk" operation, then wondered, "Is my file saved correctly?" Have you had the need to track a critical process where a power glitch can cause the loss of status and result in production loss? Are you using a microprocessor or microcontroller and need some outputs for controlling external circuitry? If these outputs can remember their last state and configure the circuitry very fast, even before the processor initializes, would that be useful? For these, and many other applications, the X4C105 is the device to choose.

Features

The low voltage X4C105 combines several functions into one device. The first is a 2-wire, 4Kbit serial EEPROM memory with write protection. A Write Protect (WP) pin provides hardware protection for the upper half of the EEPROM against inadvertent writes.

The X4C105 contains a 4bit wide NOVRAM. A NOVRAM is a static RAM with a shadow EEPROM. The static RAM part accesses very quickly, with reads and writes taking 150nS maximum. During a power fail condition, the contents of the static RAM are saved to the shadow EEPROM. When power is restored, the EEPROM is recalled to the static RAM. The static RAM provides a convenient way to save fast changing status bits that must remain true in the event of a power failure.

During a power fail or brown out condition, a low voltage detect circuit activates a /RESET pin when Vcc drops below 3V. This signal also blocks new read or write operations to minimize EEPROM corruption and initiates a NOVRAM AUTOSTORE.

The value contained in the four NOVRAM bits also appear on four separate output pins to allow continuous control of external circuitry, such as ASICs. These outputs can serve as DIP switch replacements or can "pre-configure" the hardware, prior to microprocessor initialization.

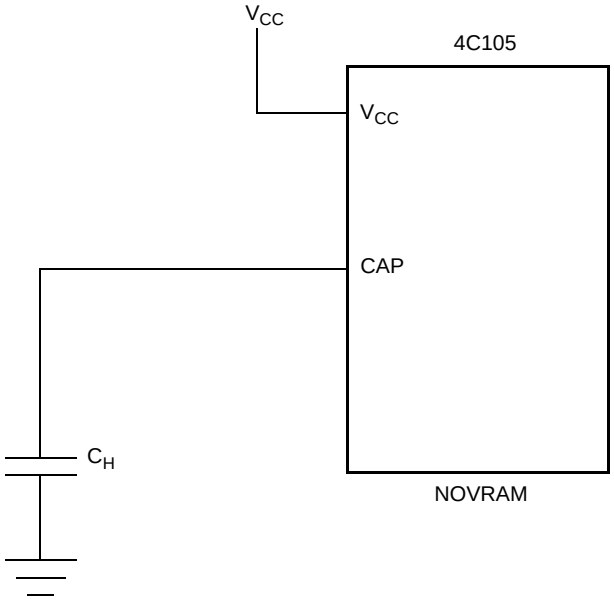

FIGURE 1. CAPACITOR SWITCH CIRCUIT

How Autostore Works

The X4C105 includes an Autostore feature that utilizes an external capacitor to supply enough power to perform the store operation when system Vcc drops below approximately 2.95 volts. Data is automatically stored and is guaranteed nonvolatile for a maximum of 10 years at operating temperature.

The X4C105 was designed to use only a single capacitor to provide the voltage for the NOVRAM backup operation, as shown in Figure 1. This "hold-up" capacitor must be capable of supplying the maximum Autostore current (I_{CC} max.) for the maximum Autostore period (T_{ASTO} max.) as Vcc falls to a level between the Autostore threshold voltage (V_{ASTH} min.) and the Autostore end voltage (V_{ASEND} min.).

The "hold-up" capacitor value (C_H) is calculated using the equation:

$$C_H = \frac{(I_{CC3}\ \mathbf{max})\ (T_{ASTO}\ \mathbf{max})}{V_{ASTH}\ \mathbf{min} - V_{ASEND}\ \mathbf{min}}$$

$$C_H = \frac{\mathbf{(3mA)\ (5mS\ for\ NOVRAM*)}}{\mathbf{2.8V - 2.0V}} \simeq \mathbf{43\mu F}$$

* add 5mS more if doing a serial store when power fails

and is derived by taking the integral of:

$$i = C\ \frac{dV}{dt}$$

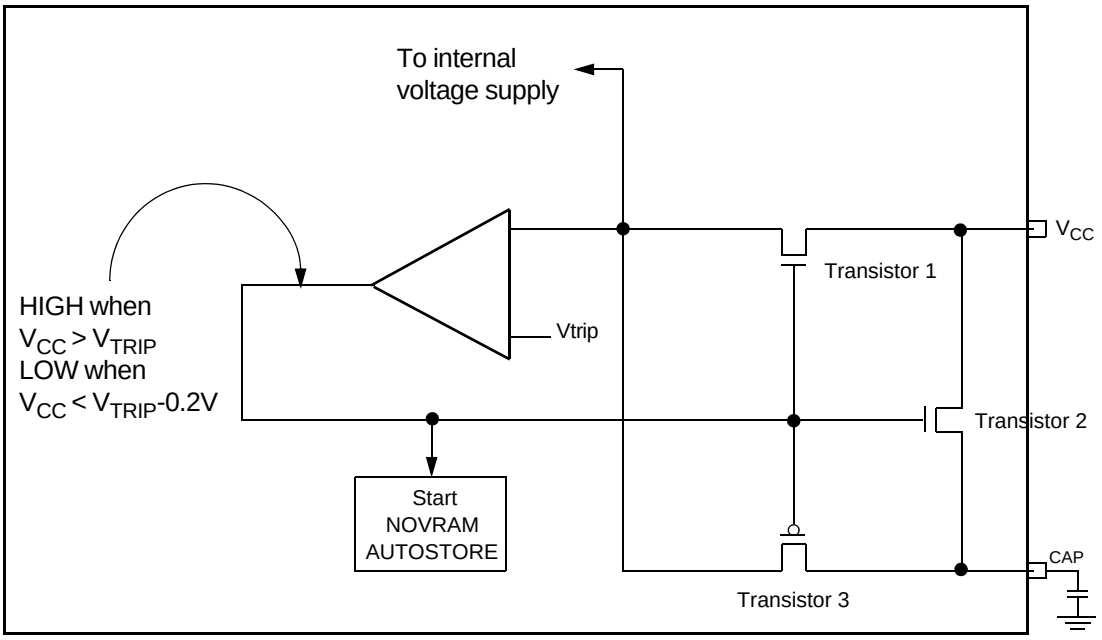

FIGURE 2. LOW POWER SENSE CIRCUIT

How the Low Power Sense Circuit Works

At system power-up, Vcc ramps up and exceeds V_{trip} that is set at between 2.8 to 2.95 volts. The low power sense circuitry creates a high level output signal which turns on transistors 1 and 2, and turns off transistor 3 as shown in Figure 2. While transistor 1 and 2 are ON, power goes to all internal circuits and also charges the external capacitor. When power fails, transistors 1 and 2 are off to prevent the capacitor from discharging into the system circuitry. Transistor 3 is on to supply power from the cap to the device internal circuits.

RAID Server Application

The term RAID (Redundant Array of Independent Disks) first appeared 5 years ago in papers written by Garth Gibson, Randy Katz, and Dave Patterson of the University of California at Berkeley.

The major task for the designer of RAID systems is to assure that data stored in the array can never be lost due to hardware failure. Major users of disk array systems such as banks, airlines, and credit agencies must be certain that they can never lose a disk in such a manner that the data stored on that disk is not recoverable. Even frequent and conscientious backing up of all disk storage does not recover new data that has been written since the last backup cycle was performed. The primary problem with the RAID systems is that if a power failure occurs, and the system's microcontroller volatile system memory is lost, the entire disk array must be scanned upon power-up to reestabilsh configuration and to redefine data locations. A solution to this data reliability problem is the use of the X4C105, CPU Supervisor with EEPROM, NOVRAM and Ports.

First, the X4C105 offers a separate serial 4Kbit nonvolatile EEPROM with write protection capability that can be use to store the system configuration data. When the low power sense circuitry detects the system power fails, no writes are allowed to the serial memory to prevent any data corruption. This will ensure that the system configuration data can be easily recovered after the system power was interrupted to avoid any system's down time.

Second, the X4C105 also has a 4bits NOVRAM utilized parallel interface for fast access. The four NOVRAM bits also appear on four separate output pins to allow continuous control of external circuitry such as monitoring the cache memory within the RAID. In the RAID server application, a 64Mb cache is used to temporarily store the data before it transfers to the hard disk. Just prior to the backup of the cache the hard disk, the microcontroller sets one of the SRAM bits to "1". When the write operation is completed, microcontroller sets SRAM bit back to "0". If there is a power interruption during the write operation, the SRAM bit indicating a backup was in progress will be automatically saved into EEPROM memory. So when the system recovers from power loss, the X4C105 auto-recall of the backup in progress flag indicates that there was an incomplete write operation and the data written into the hard disk has been corrupted. This will prevent the ambiguous "Your data may have been lost" message and prevent unnecessary disk restoration operations.

Dip Switch Control Application

In many systems, printed circuit boards use dip switches or jumpers to allow users to alter settings for different configurations. The X4C105 offers four NOVRAM bits that appear on four separate output pins to allow continuous control external circuitry. For example, the user can preprogram the dip switch control setting using the four NOVRAM bits. Then, every time at power-up the preset values are automatically recalled and the outputs set to the preassigned desired settings. This eliminates the use of the dip switches and allows the user to change the setting from a remote area using a modem.

Re-Write Application

The X4C105 can improve process control systems. For example, a blood analyzer that needs to run through several preprogrammed tests could use the X4C105 NOVRAM to track the progress of the analysis. At each step a reagent is added for a particular test. If power fails the system and can't tell where it was, so must run the test again. By using the 16 NOVRAM states, the equipment knows where it was when power fails and can continue as if there was no interruption. The same could apply to chemical or manufacturing processes. It could even apply to software operations.

Conclusion

The X4C105 is a highly integrated device that combines CPU Supervisor with EEPROM, NOVRAM and output buffers and latches. The 4Kbit serial EEPROM stores configuration data for calibration. Low power sense circuitry monitors the level of the supply voltage. In the event of power failure, the device signals the microcontroller to shut down before the system locks up. In addition, the NOVRAM performs an autostore to save data into the EEPROM to preserve the condition just prior to power failure.