Variable Pulse Width Variable Frequency Pulse Generator

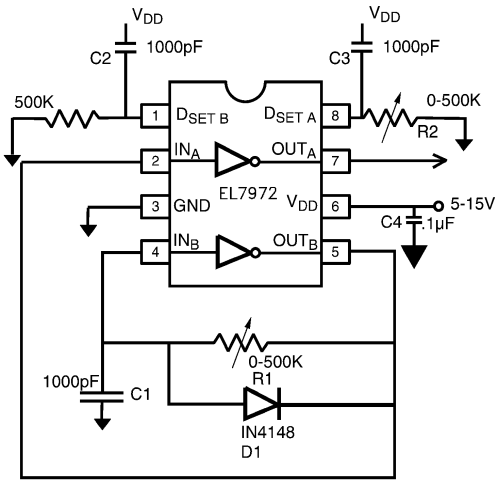
This application uses the “B” driver of the EL7972 as an oscillator to drive the “A” driver. The frequency is set using R1 and C1. The pulse width is set by adjusting R2. Capacitors C2, C3 and C4 are decoupling capacitors. A fixed pulse width output is available at pin 5 while the variable pulse width signal is available at pin 7. For these particular component values a maximum pulse width of 2µs is available at pin 7.

The frequency is approximated by the relation:

$f(Hz) = (1.5)\ V_{DD}(R1)\ (C1)$

The pulse width is approximated by the relation:

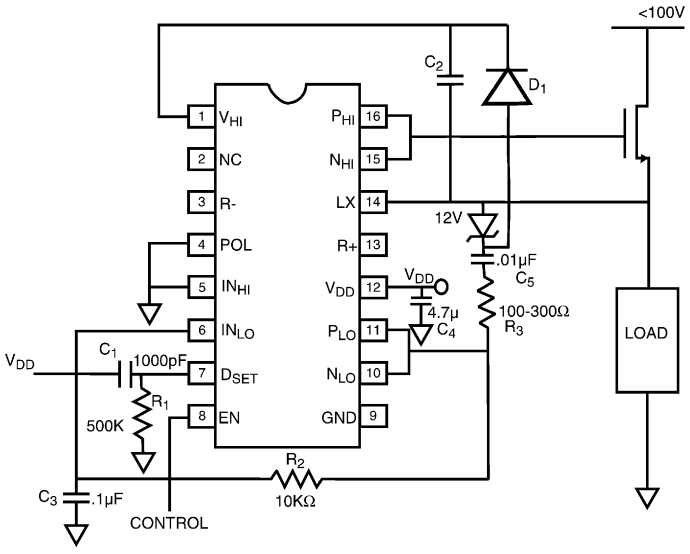
$T_{width}\ (S) = (4.5 \times 10\text{-}6)\ 1 - R2500KV_{DD} - 100ns$



100V DC Stable High Switch

This application uses an EL7761 to drive the gate of an NMOS FET above the FET's source and drain voltage. This circuit would be useful in applications where the load must be energized continuously as in an automobile headlight circuit or a high side switch to a 48V bus in a distributed power application.

The low side driver self oscillates at a frequency determined by its input hysteresis in conjunction with R2 and C3. The output of the oscillator (pins 10 and 11) drive a charge pump which powers the high side drive section of the EL7761. A low voltage at the EN pin shuts the drive to the external FET off as well as shutting down the charge pump oscillator and putting the chip into a low supply current mode. Capacitors C1 and C4 are used to decouple the supplies. V_{DD} must be at least a diode drop higher than the desired enhancement of the external FET. The reverse breakdown of the zener diode should be less than 15V in order to avoid an overvoltage of the high side driver. Depending on the exact nature of the circuit a zener diode is not always necessary.



C_1 - 1000pF ceramic
C_2 - .1µF ceramic
C_3 - .1µF ceramic
C_4 - 1-4.7µF Tant.
C_5 - .01µF ceramic 100V

D_1, D_2 - IN4148
R_1 - 500KΩ 1/4w
R_2 - 10KΩ 1/4w
R_3 - 100Ω - 300Ω 1/4w

100V, Single chip, DC stable high side switch

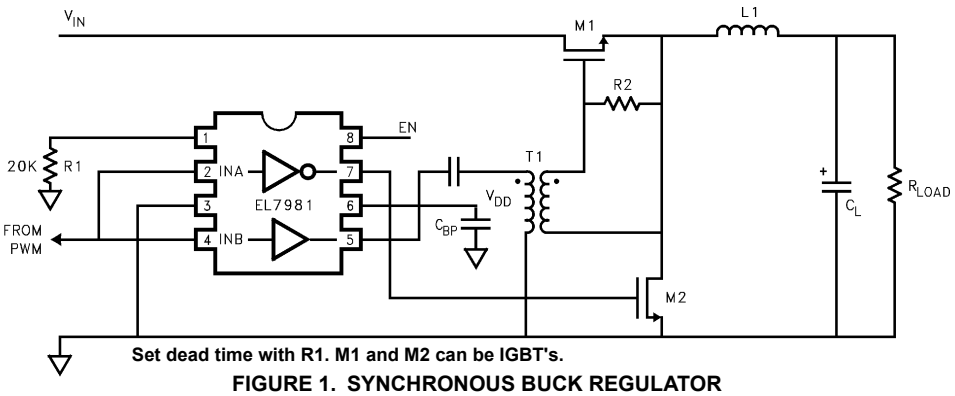
Synchronous Buck Regulator Driver

In this application one driver of the EL7981 is used to drive the main switch of a buck regulator while the other driver drives the synchronous switch. A transformer is used to obtain the high side switching voltage for M1. R1 sets the dead time delay between the on times of M1 and M2. The adjustable delay is perfect for devices with long turn off times such as IGBT's.

Buck Regulator High Side Drive Using the EL7501

These circuits show two ways of using the EL7501 to drive the high side switch in a buck converter application. The first method uses resistors R1 and R2 to bias pin 1 in the middle of the drive voltage swing at pin 4. This allows the use of a single sided PWM drive. The high side voltage is pumped up from the V_{DD} supply.

The second method uses a complementary drive signal at pins 1 and 4 of the EL7501. It derives its high side supply voltage by charging capacitor C1 through resistor R1 and then using the external FET to pump that voltage above the high side supply.



Set dead time with R1. M1 and M2 can be IGBT's.

FIGURE 1. SYNCHRONOUS BUCK REGULATOR

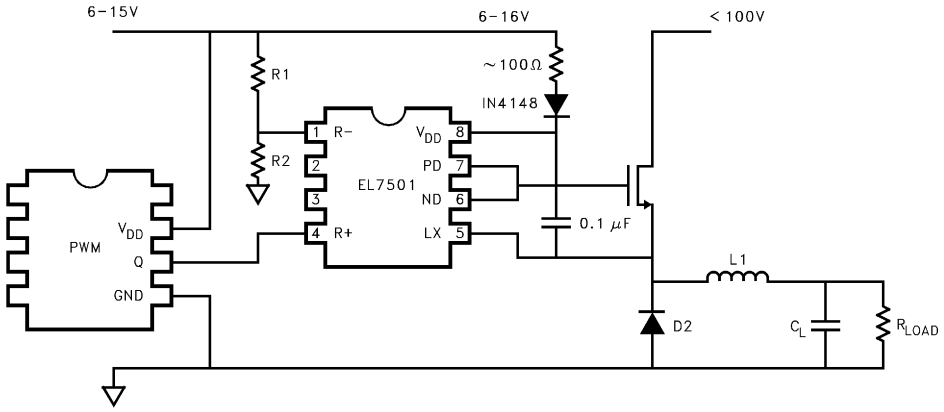


FIGURE 2A. EL7501 BUCK REGULATOR WITH HIGH SIDE DRIVE - FIRST METHOD

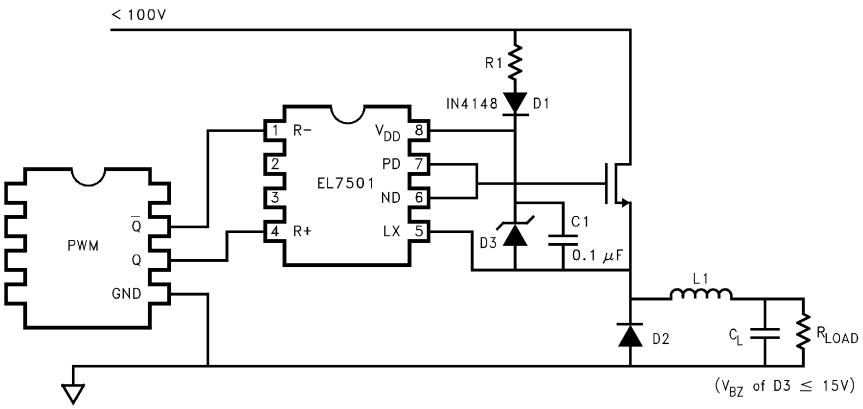


FIGURE 2B. EL7501 BUCK REGULATOR WITH HIGH SIDE DRIVE (ALTERNATE BIASING SCHEME) - SECOND METHOD

Self Powered DC Stable 100V Half Bridge Driver

This circuit uses one driver of an EL7972 to provide low side drive and the other driver as a charge pump oscillator. The output of the charge pump oscillator drives a capacitor diode network to provide high side supply voltage to the EL7501. The EL7501 drives a high side external N-FET. Due to the addition of the charge pump this circuit will work at any driving frequency from DC to >1MHz.

IGBT Half Bridge Driver

This circuit shows the EL7981 being used to drive an IGBT half bridge. The high side IGBT is transformer coupled to the driver. The value of R1 is chosen so that the two IGBT's never conduct at the same time. If the IGBT's have different turn off characteristics then the EL7982 could be used instead of the EL7981. The EL7982 has independent control of each of its driver's rising edge delay.

Self Oscillating IGBT Driver

This circuit self oscillates at approximately 25kHz. The on times of each driver depend on the values of R1, C1, R2 and C2. In order to ensure equal on times accurate component values may need to be used. The resistor, R3, controls the dead time between the on times of both drivers.

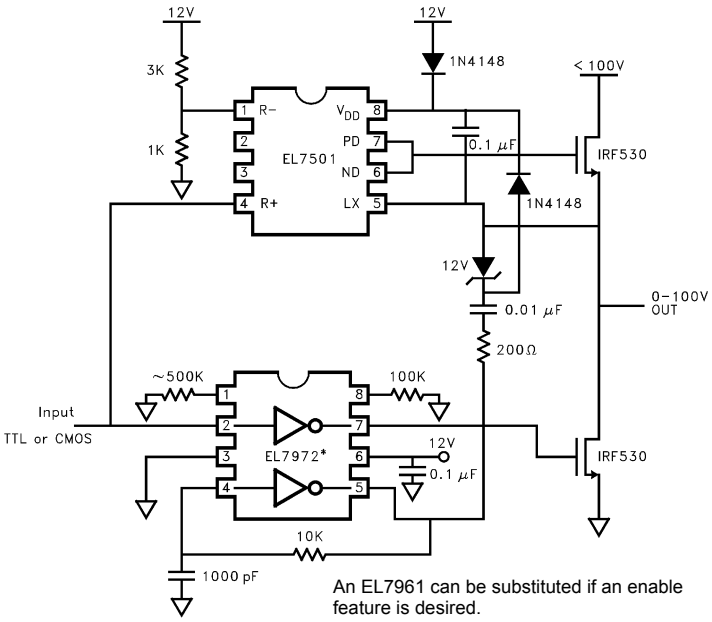


FIGURE 3. DC FUNCTIONAL HALF BRIDGE DRIVER

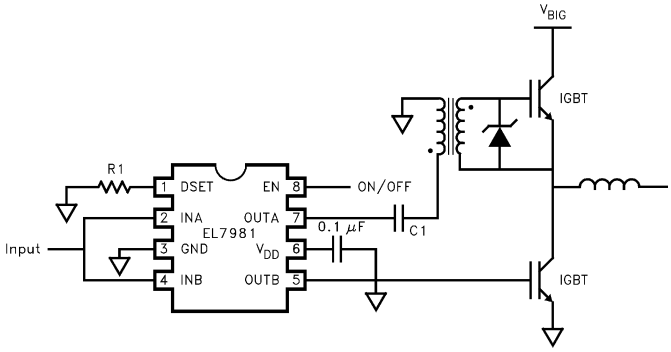


FIGURE 4. IGBT HALF BRIDGE DRIVER

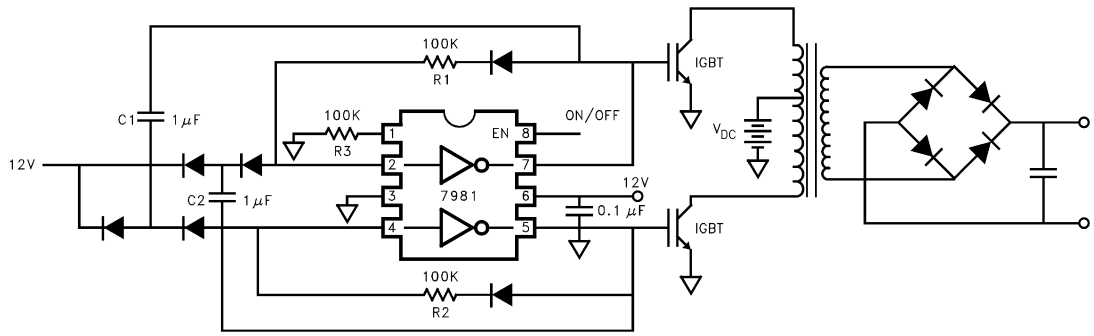


FIGURE 5. SELF OSCILLATING IGBT DRIVER, DC-DC STEP UP (OR DOWN)

40 Watt-12V Step Down Regulator Using a Synchronous Switch

This circuit shows how the EL7761 could be used as a half bridge driver for a step down converter. The circuit switches at 250kHz.

Simple Undervoltage Lockout Circuit

By using a zener diode and a pull down resistor the user can implement a simple UVLO circuit. As V_{DD} increases above the zener voltage the EN pin rises above ground. When EN reaches V_{ton} the chip is enabled. As V_{DD} is lowered such that the voltage at EN falls below V_{toff}, the chip is disabled. The threshold tolerances are as follows:

$1.0V < V_{ton} < 1.6V$

$0.3V < V_{ton} - V_{toff} < 1.0V$

$V_{turn\text{-}on} = V_Z + V_{ton}$

$V_{turn\text{-}off} = V_Z + V_{toff}$

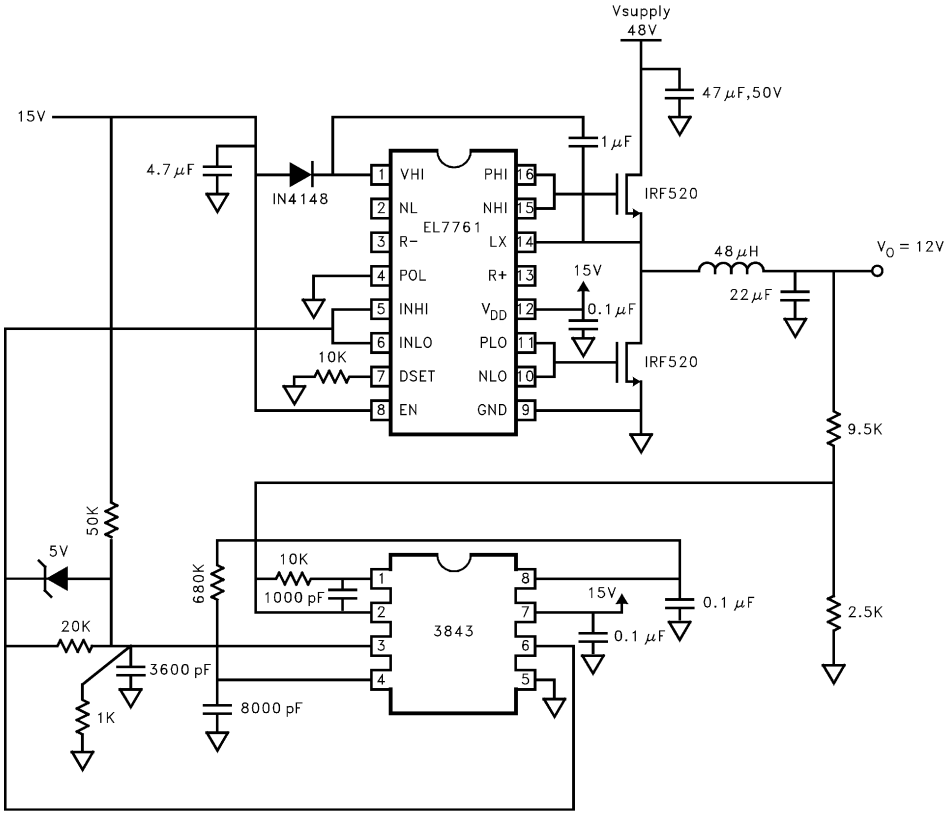


FIGURE 6. 12V STEP DOWN SYNCHRONOUS SWITCHES

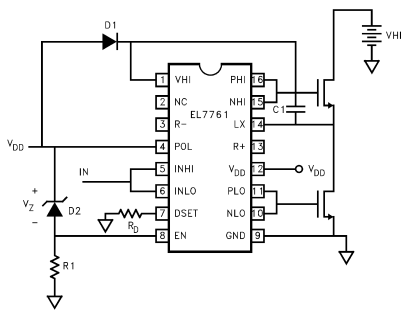
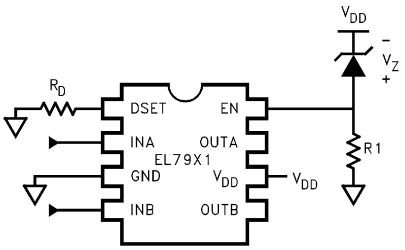


FIGURE 7. SIMPLE UVLO CIRCUIT FOR THE EL7761



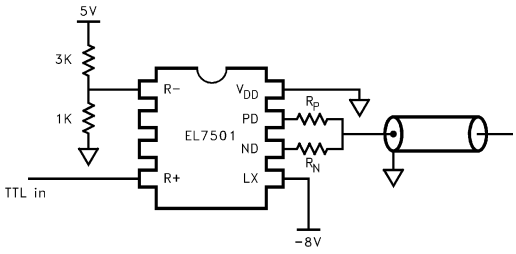
$V_{turn\text{-}on} = V_Z + V_{ton}$

$V_{turn\text{-}off} = V_Z + V_{toff}$

FIGURE 8. SIMPLE UVLO CIRCUIT FOR THE EL79X1

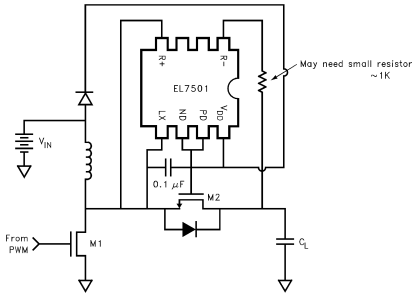
Video Sync Pulse Generator

The EL7501 inputs function outside the power supply rails, allowing a ground referenced TTL signal to control a ground to -8V output swing. The output resistors can be adjusted to tailor the rise and fall times of the circuit.



Synchronous Switch Increases Boost Efficiency

The EL7501 plus a N-FET replaces the catch diode in a boost regulator. When the R+ pin is higher than the R- pin, the FET is turned on, effectively shorting out the parasitic diode of the FET. A small resistor may be added in series with the R- pin in order to “tune” the turn-on delay of the FET.



Resonant Gate Driver

Resonant gate driver can be used to boost the gate voltage swing while increasing driver efficiency. In Figure 9, an EL7501 is configured with (2) external “ring” diodes and resonating inductor L_R. For tutorial purposes, the power MOSFET load was replaced by a 1000pF capacitor (C_L). The “ring” diodes are fast switching diodes capable of withstanding the 1 amp peak current, such as the 1N914. Standard de-coupling techniques are applied with 5V applied to V_{DD}, the circuit delivers +10V to -5V output. In “5V only” systems, sufficient output swing is available so as to eliminate the need for costly “logic level” power FETs, and provides below ground swing for superior turn-off.

Principle of Operation

When the input drops below 2.4V, pin 7 pulls high, allowing current to flow from V_{DD} thru D1 and L_R, thus charging C_L. Initially the full voltage appears across the inductor, but as the current starts to flow, C_L begins to charge. When C_L reaches the supply voltage, current continues to flow as the inductor L_R reverses direction and continues to charge the capacitor beyond the supply voltage. When C_L reaches it's peak, the “ring” diode disconnects, holding that potential across C_L. The peak voltage can be controlled by adjusting the circuit “Q”. Typically this is accomplished by varying the size of inductor L_R, since the “on” resistance of the driver can limit the circuit “Q”. This is governed by the expression:

$Q = \omega LR$

where: $\omega = 1LC$ or $Q = 1R\ LC$

Thus, higher “Q”, and higher voltage swing can be maintained by making L/C large compared to R. (R = 5Ω typ. for the EL7501.)

Similarly, when pin-6 pulls low, the output resonates below ground to provide good turn-off. Since charge is transferred mostly thru the inductor, rather than a resistor efficiency is much higher. The circuit performance is summarized below.

TABLE 1. CONDITIONS: V_{DD} = 5V F_C = 220kHz

(L) INDUCTANCE		V_{OUT} (+)	V_{OUT} -	T_R/T_F
Case 1	1µH	7V	-2.1V	60ns
Case 2	47µH	18V	-12V	300ns

The power consumption was measured for Case 2, at 40mW. Using “resistive” charging a power dissipation/consumption of 200mW is anticipated, thus resulting in a (5) fold improvement in efficiency.

$UV = (1.5)\ R_1 + R_2R_1$

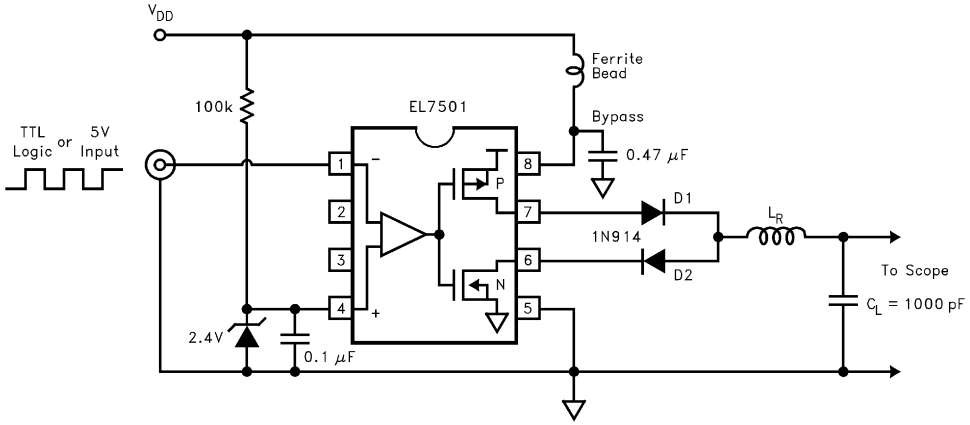


FIGURE 9. RESONANT GATE DRIVER

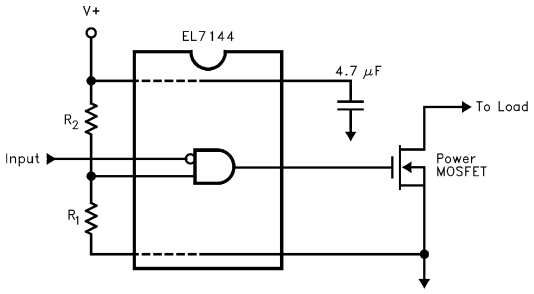


FIGURE 10. MOS DRIVER WITH UNDER-VOLTAGE LOCK-OUT

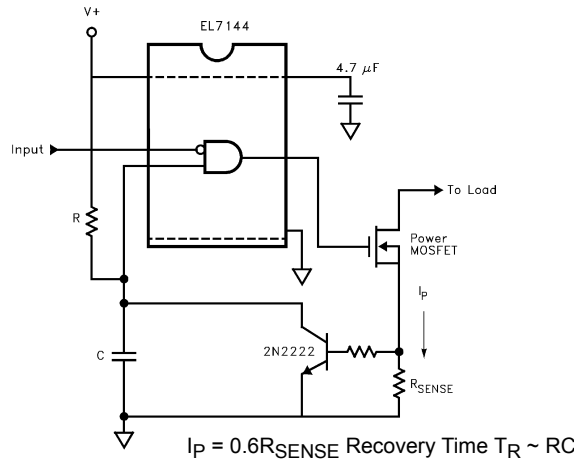


FIGURE 11. OVER-CURRENT PROTECTED DRIVER

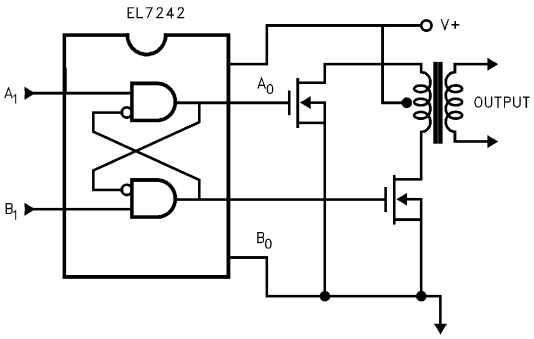


FIGURE 12. MOS DRIVER WITH SIMULTANEOUS CONDUCTION LOCK-OUT

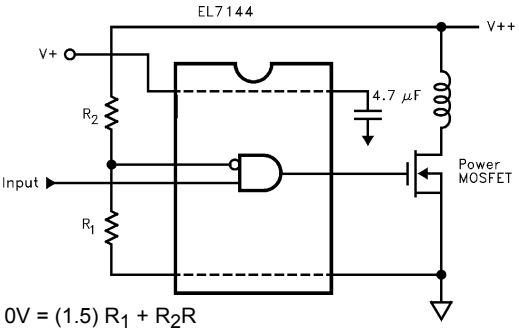


FIGURE 13. MOS DRIVER WITH OVER-VOLTAGE PROTECTION

TABLE 2. TRUTH TABLE

A_1	B_1	A_0	B_0
0	0	0	0
0	1	0	1
1	0	1	0
1	0	1/0	0/1

MOSFET Driver Generates its Own +12V Supply

When you want to drive one power MOSFET, from a 5V or a 3.3V system, generating the one extra +12V supply can involve quite a large number of both active and passive components.

Here is a solution that uses the spare second MOSFET Driver channel to derive its own +12V supply. By using a driver with the drains brought out to separated pins, one can connect an inductor between the N-channel drain and the logic supply, without having the P-channel device connected.

In operation, it works as a standard flyback style switched mode circuit. When the output N-channel device is on, current starts flowing in the inductor, storing energy. When the N-channel device is turned off, the current has to continue flowing, so it flows through the diode D2 to charge up capacitors C1 and C2. As the cycle repeats, the voltage on C1 and C2 rises until the zener diode prevents further voltage rise. This is needed to prevent the drivers' derived supply from exceeding the parts' maximum voltage rating.

Since the objective was to minimize the number of external components and cost, additional components which would allow the circuit to self oscillate and regulate were omitted. The logic system was able to supply a drive pulse waveform to the supply generator. With the 5V system, I was using a 1.5µs pulse every 9µs. This gave a very solid +12.4V, and the system supply current went up by about 11mA. The 3.3V system used a 300kHz square wave, for a similar 12V derived supply, but with nearly 40mA extra supply current. In both systems, when the MOSFET Driver was not being used, it could be “powered down” by simply stopping the pulses to the switching channel.

Any dual MOSFET Driver can be used, but if the drains of the output stage are not separated, there may be some protection and other parasitic devices that may prevent satisfactory operation. In these cases an external fet can be used to drive the inductor, provided a low threshold device is used. By altering the inductor value and the controlling pulses, enough power can be derived for further MOSFET Drivers or other peripheral devices requiring +12V.

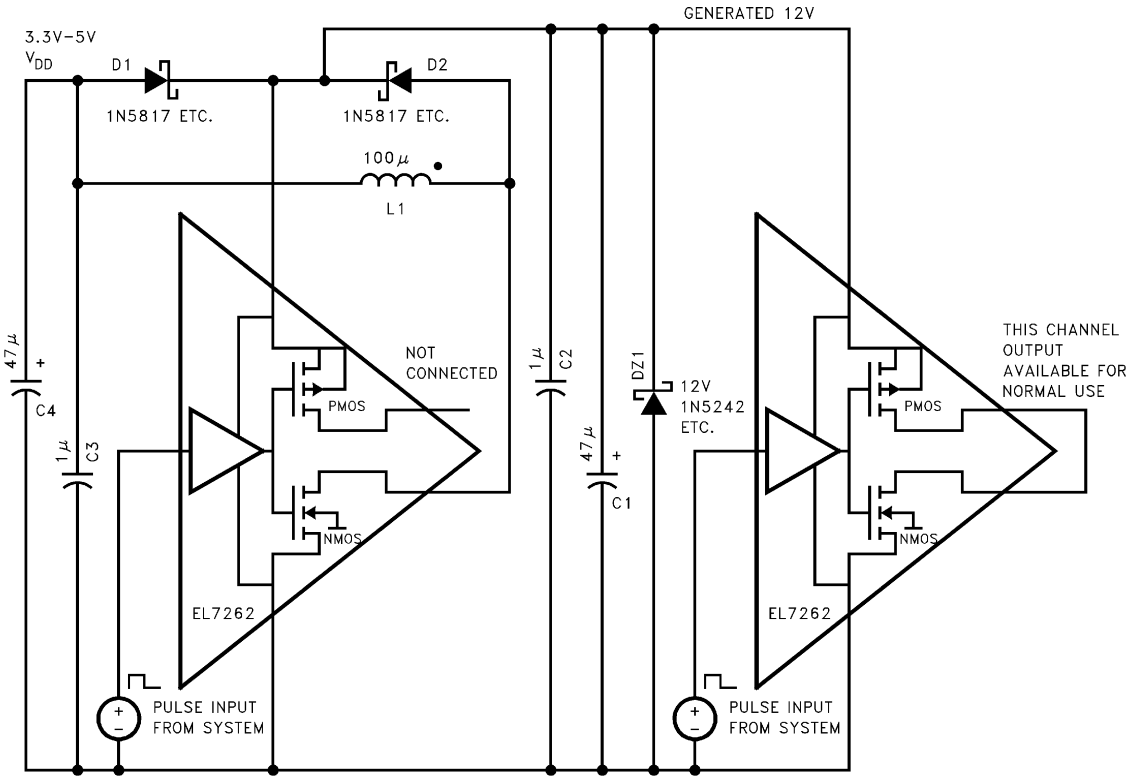


FIGURE 14. SELF CHARGE PUMPING MOSFET DRIVER

Super Inverters

CMOS is often equated with low power, however dynamic losses can be significant, particularly as the frequency of operation increases. Losses can be attributed to the parasitic capacitance on all internal nodes which toggle (described by P = CV2f), and from simultaneous conduction through CMOS gates during switching. Parasitic capacitance is reduced by shrinking feature sizes and using low overlap, self aligned silicon-gate process technology. Simultaneous conduction (shoot-thru) can be controlled or eliminated completely with “super-inverter” technology. A standard CMOS inverter is shown in Figure 15A. Here, with every transition, there is an interval during which both the NMOS and PMOS transistors are conducting and dissipating energy.

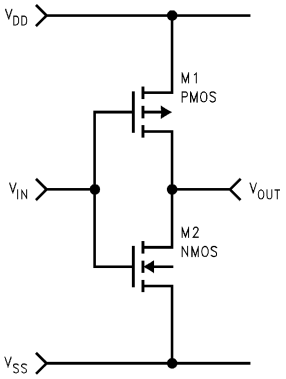


FIGURE 15A. STANDARD CMOS INVERTER

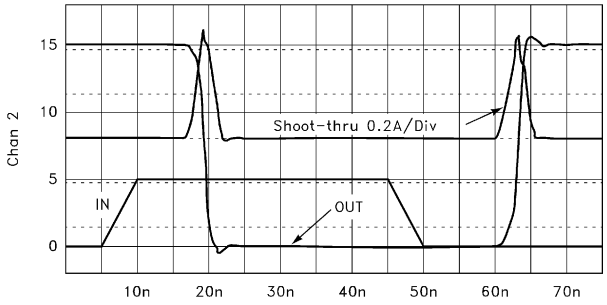


FIGURE 15B. CMOS INVERTER SWITCHING LOSSES

Thus the integral of the instantaneous shoot-thru current, multiplied by the supply voltage and clock frequency describes the power loss.

$P = 2fV\int I_S(t)dt$

These losses can be significant, and are illustrated in Figure 15B. The super-inverter shown in Figure 16A overcomes the “shoot-thru” problem with “break before make” asymmetric drive, thereby controlling or eliminating simultaneous conduction. The designer can trade-off shoot-thru current for added propagation delay. The results demonstrated in Figure 16B represent about a 4× improvement. An added benefit is the reduced power supply bounce resulting from di/dt and stray inductance.

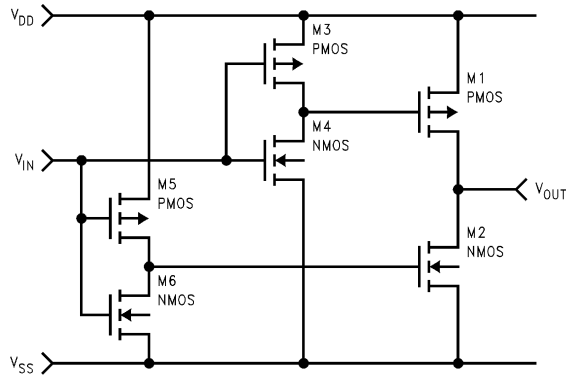


FIGURE 16A. SUPER INVERTER

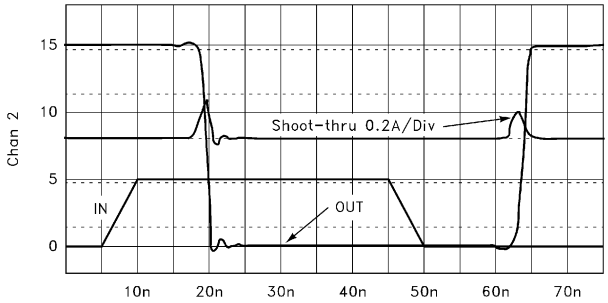


FIGURE 16B. SUPER INVERTER SWITCHING LOSSES

Input Source Follower

To accommodate moderately high source inpedances, a source follower input stage similar to the circuit shown in Figure 17 is used. This eliminates both the “Miller” gate capacitance, and gate to source capacitance seen in typical designs. The “boot-strapping” effect eliminates all but the gate-drain capacitance. This feature allows direct drive from low current logic, without any degradation in performance.

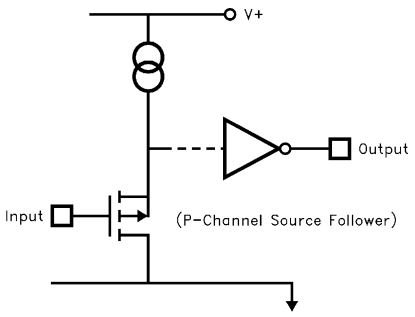


FIGURE 17. LOW INPUT CAPACITANCE SOURCE FOLLOWER

Precision Level Shifting

Generating rail to rail drive from a logic level input is accomplished with a Class AB push-pull amplifier and an internal 1.2V reference. This produces a well controlled threshold with minimal propagation delay. The known switch point can be used to generate under-voltage lock-out protection. Hysterisis is also introduced to boost the noise immunity.

3-State and Gated Inputs

Additional logic functions are also provided to insure greater flexibility. 3-State control is often useful in “Bridge” and “Bus” applications. Gated inputs can be used for chip enable/shut-down, latching, and various other functions.

Overall Performance

The resulting CMOS Drivers offer both functionality and performance. Figure 18 shows the switching characteristics into a 1000pF load. Rise time, fall time, and delay are all matched to minimize pulse distortion, and are less than 20ns. Figure 19 illustrates the waveform integrity at 5MHz, into 1000pF.

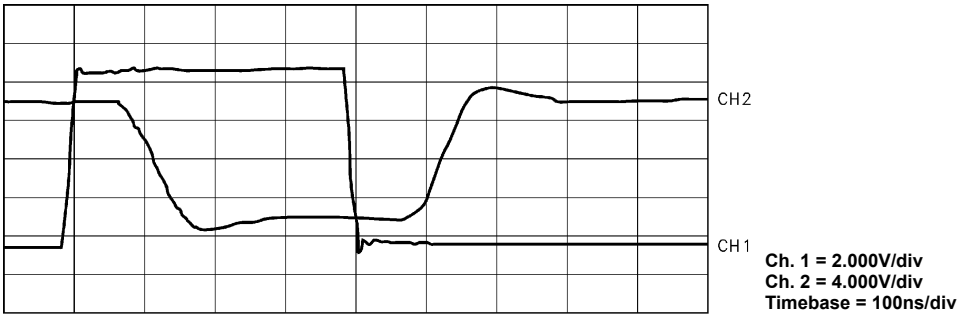


FIGURE 18. STEP RESPONSE INTO 1000pF LOAD

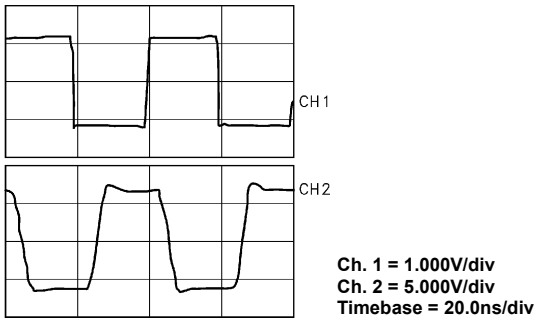


FIGURE 19. 5MHz OUTPUT INTO 1000pF LOAD

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