AN1079
Rev 0.00
August 2003

ISL38601M-CD PRISM GT™ IEEE 802.11b/g miniPCI Wireless LAN Radio Description

Introduction

The Intersil ISL38601M WLAN radio is a complete wireless high speed Network Interface Card (NIC) utilizing the Intersil PRISM GT Direct Sequence Spread Spectrum (DSSS) Wireless Transceiver chip set in a miniPCI implementation. It provides a complete PRISM GT reference design evaluation platform consisting of hardware and software for system providers or integrators requiring wireless communications capability and is well suited for integration into computer platforms running various operating systems.

A complete PRISM GT WLAN reference design package (ISL38601M-CD) or an evaluation kit (ISL38601M-EVAL) have been made available. The ISL38601M-CD reference design package includes all the documentation needed for large scale manufacturing of the ISL38601M NIC including: Cadence/Allegro layout files, Printed Wiring Board (PWB) Gerber files, Cadence/Concept schematic files, a costed Bill of Materials complete with component sourcing, assembly and mechanical drawings, a Manufacturing and Engineering test plan and a copy of the FCC application for equipment authorization. Customers who license the reference design also receive password access to Intersil's Premier Web site for the most current updates on hardware and software.

The Evaluation kit (ISL38601M-EVAL) includes two WLAN miniPCI cards conforming to Intersil's PRISM GT reference design, Microsoft Windows® driver, Local Area Network evaluation software, Test Utilities software and documentation necessary to perform a complete evaluation of the WLAN NIC. The reference design supports the IEEE 802.11g network specification for DSSS signaling, providing data rates of 1, 2, 5.5 and 11Mbps CCK as well as 6, 9, 12, 18, 24, 36, 48 and 54Mbps OFDDM.

Figure 1 shows a block diagram of the reference radio design. This radio has been designed to conform to the proposed IEEE 802.11g standard.

This application note details the RF and analog design of these cards giving a detailed description of the receive and transmit signal processing.

Ordering Information

PART NUMBER	DESCRIPTION	CARDS/SET
ISL38601M-EVAL	WLAN Evaluation Kit	2
ISL38601M-CD	Reference Design	N/A

Overview

The IEEE 802.11 specification is a standard for wireless connectivity for fixed, portable, and moving stations within a local area.The IEEE 802.11 specification actually consists of several standards. This radio conforms to the IEEE 802.11g standard. The 802.11 standard describes the services required by a compliant device to operate within an "*ad hoc*" or "infrastructure" network, as well as dealing with the issues related to mobility within those networks. Spread spectrum techniques are used to tolerate mobility and multipath effects. They are also a requirement for compliance with FCC, ETSI and those of other regulatory authorities when operating within the Industrial, Scientific, and Medical (ISM) frequency band.

An *ad hoc* communications network is created quickly and informally for a temporary time period. An infrastructure network usually requires more planning so that wireless stations can communicate over longer distances through Access Points (AP's), and may also communicate with existing wired LANs using portals.

The 802.11 standard describes Media Access Control (MAC) procedures. The principal method of communication is the Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) protocol. Using this protocol, each station senses the communications medium (RF channel), and does not transmit until the channel is clear. This avoids collisions and minimizes the retransmission of subsequent packets.

The standard also supports the operation of a station within a wireless LAN that may coexist with several overlapping wireless LANs. To accomplish this, a scheme of channelization and spread spectrum techniques is used. Direct Sequence (DSSS) and Frequency Hopping (FHSS) spread spectrum techniques are supported by the standard and both operate in the 2.4 to 2.4835GHz frequency band (the unlicensed ISM band). An infrared technique is also supported for indoor applications.

The standard has also specified the requirements and services that enable private and secure communications to occur.

Wireless LAN Configurations

For ease of use in evaluating these cards, an *ad hoc* network for peer to peer communications can be created. An *ad hoc* network is usually created for a specific purpose (such as a file transfer or accessing a database). *Ad hoc* networks simplify the process of creating and dissolving networks for nontechnical users of the network facilities. Two cards form an IEEE 802.11 Independent Basic Service Set (IBSS), the simplest *ad hoc* network. The cards

communicate with each other directly and must remain within radio range. When both cards are on, they immediately “see” each other and the *ad hoc* network is formed without user intervention.

To use the cards in an infrastructure BSS (also called an Extended Service Set) where the two cards may not be in direct radio contact, Access Points (AP’s) are needed. The association between a card (station) and an infrastructure BSS, where communication occurs only between a station and an Access Point and not between stations directly, is dynamic.

The IEEE 802.11 protocols are implemented in the firmware so that file transfers or database access can begin immediately.

Direct Sequence Spread Spectrum Approach

The use of spread spectrum techniques for wireless computer communications is widely accepted because of its robustness against multipath effects and interference from intentional or unintentional radiators. The use of spread spectrum techniques in the ISM frequency band also allows products to be deployed without the need for an FCC license.

The two main methods by which spread spectrum communications can be achieved are Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS). This wireless LAN PC card uses the DSSS technique. DSSS transmission has the best performance in terms of multipath immunity and jamming rejection. In an office environment, jamming sources are likely to be unintentional such as emissions from microwave ovens. Even though unintentional, they pose a threat to the communications network. Direct sequence techniques are superior to frequency hopping systems in this case because FHSS gains its immunity to jamming by avoiding the location of a single tone jammer (such as other FHSS users). When collisions occur, data is lost. With a DSSS system, the despreading function in the receiver gives immunity to jamming by spreading the interfering energy by the Pseudo Random Number (PN) code over the whole bandwidth. This selective despreading attenuates the jammer power while ampliifying the desired signal.

In the office environment, multipath effects may degrade network communications. Direct sequence techniques offer better protection than slower frequency hopping systems in the presence of multipath interference. With frequency hopped systems, if the hopper jumps to a frequency where a null resides, then data is lost until the next hop. Multipath signals can be thought of as a special case of unintentional jamming. In the DSSS approach, nulls resulting from multipath fading only eliminate a fraction of the signal power since the bandwidth in the DSSS case is very large. A significant amount of energy still remains in the signal and effective despreading still occurs. The probability of burst errors is reduced significantly.

An often overlooked factor when comparing IEEE 802.11 compliant DSSS and FSSS implementations, is the achievable data rate. A frequency hopping occupied bandwidth of 3MHz as specified by the FCC acts as a limitation when using data rates beyond approximately 6Mbs. A similar bandwidth limitation has not been imposed when using the direct sequence implementation.

802.11g Modulation Modes

There are three different modulation modes utilized in 802.11g radios: Legacy 1 and 2Mbps, Complementary Code Keying (CCK) and Orthogonal Frequency Division Multiplexing (OFDM). These are more fully described in the subsequent paragraphs. The radios support the following 12 data rates:

- 1Mbps (BPSK modulation)
- 2Mbps (QPSK modulation)
- 5.5Mbps (CCK modulation)
- 6Mbps (OFDM with BPSK carrier modulation)
- 9Mbps (OFDM with BPSK carrier modulation)
- 11Mbps (CCK modulation)
- 12Mbps (OFDM with QPSK carrier modulation)
- 18Mbps (OFDM with QPSK carrier modulation)
- 24Mbps (OFDM with 16QAM carrier modulation)
- 36Mbps (OFDM with 16QAM carrier modulation)
- 48Mbps (OFDM with 64QAM carrier modulation)
- 54Mbps (OFDM with 64QAM carrier modulation)

Note that each OFDM constellation type supports two different data rates. This is due to the change in the degree of rate coding between the two formats. For example the 6Mbps BPSK mode uses rate 1/2 coding whereas the 9Mbps mode uses rate 2/3 coding.

Legacy 1 and 2Mbps and CCK Modulation

IEEE 802.11g radios are fully backward compatible with the well established IEEE 802.11b standard. The 802.11b standard uses CCK modulation to achieve a maximum data rate of 11Mbps. It also supports the legacy data rates of 1Mbps BPSK and 2Mbps QPSK modulation. More information on the CCK high data rate standard may be found in Application Note AN9850, “Complementary Code Keying Made Simple” [10], which may be found on the Intersil Web Site.

OFDM Modulation

Orthogonal Frequency Division Multiplexing (OFDM) modulation is an impressive solution to the problems of high speed data transmission and indoor propagation characteristics. A maximum data rate of 54Mbps is achieved using this sophisticated modulation technique.

The high speed data rate is divided into 52 lower data rate subcarriers, distributed over a 20MHz spectrum. Interference

between adjacent subcarriers is minimized by using the principles of orthogonality and Inverse Fast Fourier Transform (IFFT). Simultaneously, OFDM extends the symbol time and provides a guard time to solve the majority of the inter symbol interference (ISI). The principle of orthogonality is used to compress many subcarriers into a smaller bandwidth while ensuring that individual subcarriers are mutually independent.

802.11 OFDM permits data rates that exceed what is possible with a single carrier in a given bandwidth. The cost is increased spectrum occupancy and quite complex signal processing.

List of Test Instruments

The following instruments may be used for conducting tests on the wireless LAN PC card.

INSTRUMENT	MANUFACTURER	MODEL
Spectrum Analyzer	Agilent (Hewlett-Packard)	8595E
Power Meter	Giga-tronics	8541B
Signal Generator	Agilent (Hewlett-Packard)	8648C
Frequency Counter	Agilent (Hewlett-Packard)	53181A (012 Option)
Digital Scope	Tektronix	TDS 3054
Logic Analyzer System	Agilent (Hewlett-Packard)	16500B
General-Purpose Digital Multimeter		
Computer with a Cardbus32 Connection Slot (2 required)		
3V Cardbus32 Extender Card	Sycard Technology	PCCextend 135 Cardbus Extender www.sycard.com
Vector Signal Analyzer	Agilent Hewlett Packard)	E8408A
Coaxial RF Test Probe	Murata	MXGS83RK3000

Block Diagram

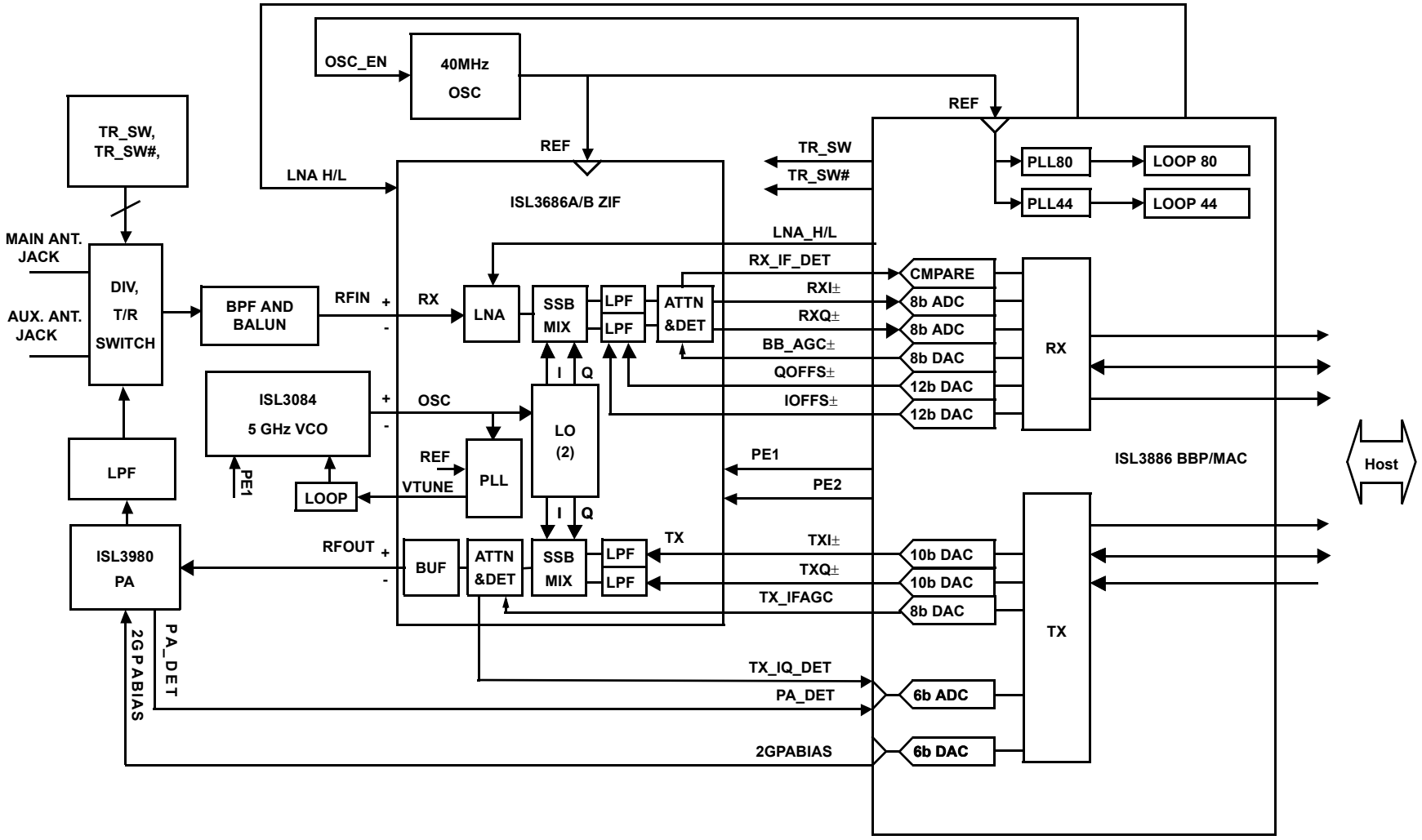

FIGURE 1. ISL38601M WIRELESS LAN PC CARD BLOCK DIAGRAM

Test Point Diagrams

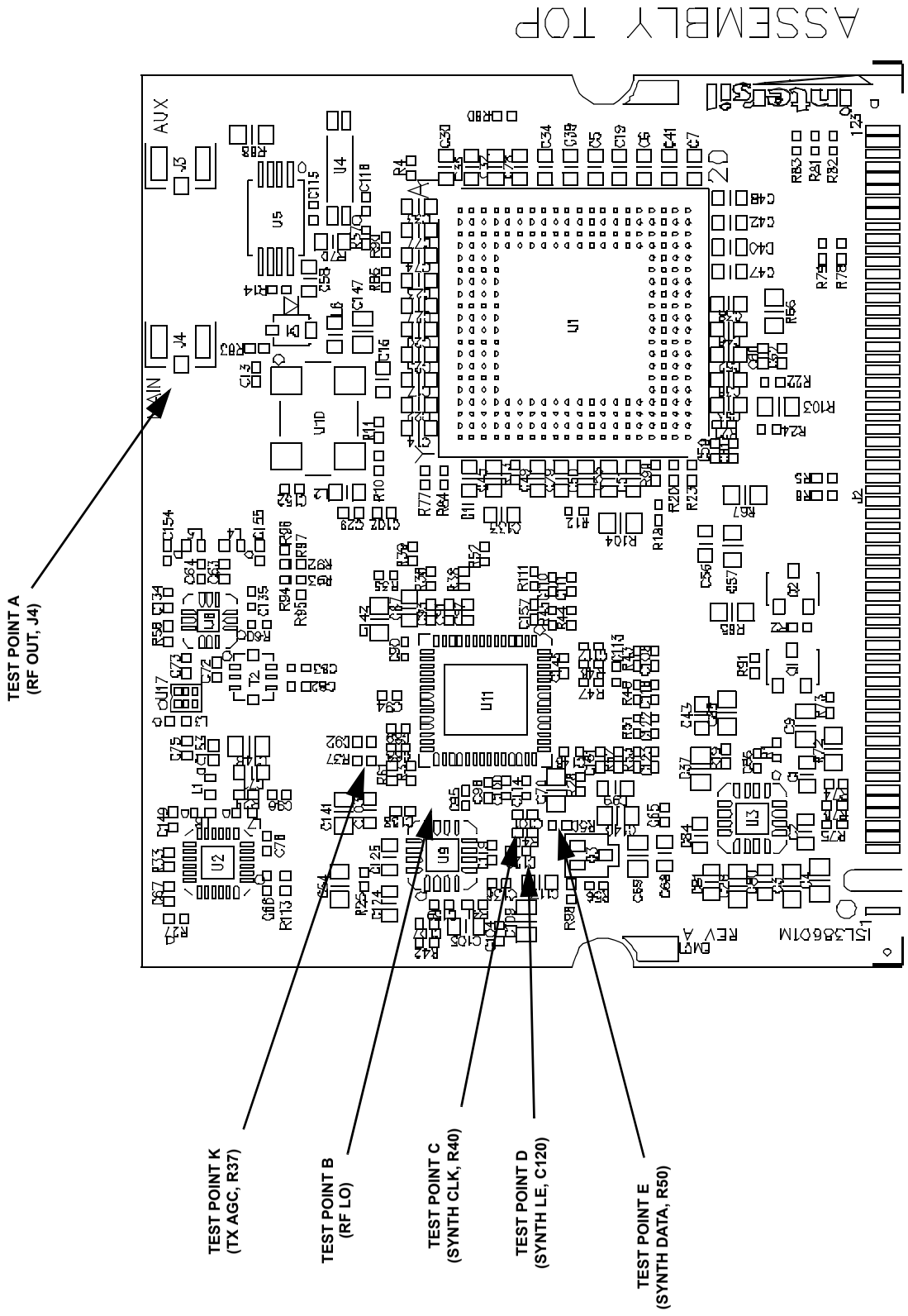

FIGURE 2. WIRELESS LAN PC CARD TEST POINTS (TOP VIEW)

Test Point Diagrams (Continued)

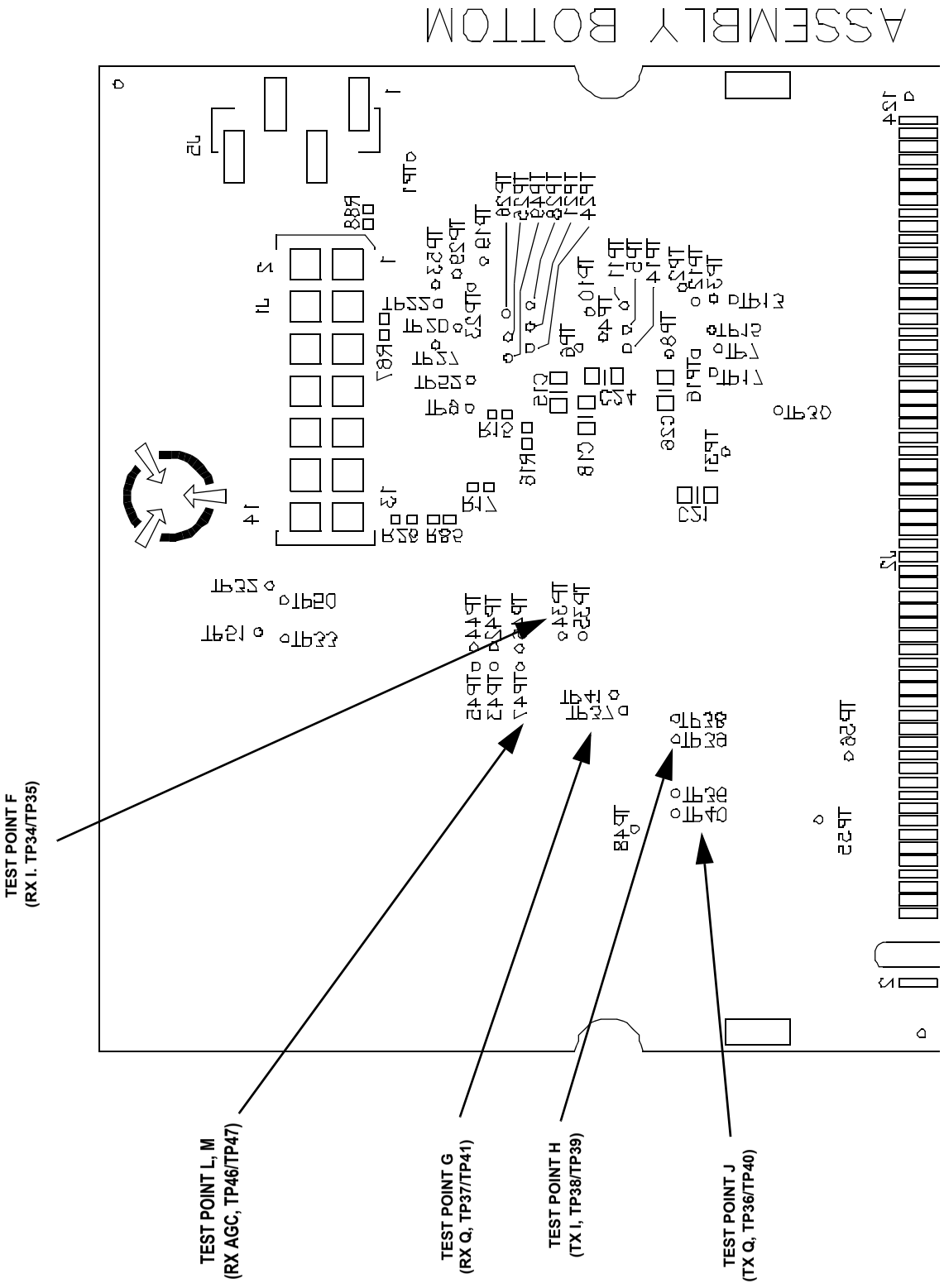

FIGURE 3. WIRELESS LAN PC CARD TEST POINTS (BOTTOM VIEW)

Receive Signal Path

TABLE 1. RECEIVER CASCADED GAIN ANALYSIS

STAGE	GAIN (DB)	CUMULATIVE GAIN (DB)	NOISE FIGURE (DB)	CUMULATIVE NOISE FIGURE (DB)	CUMULATIVE INPUT IP3 (DBM)	INPUT IP3 (DBM)
RF Crosspoint Switch	-0.5	-0.5	0.5	0.5	-17.5	
Bandpass Filter	-2.5	-3.0	2.5	3.0	-17.0	
Down-Converting Mixer + LNA	27	24	4.5	7.5	+3.5	
Entire Receiver: Antenna to Mixer Output		24		7.5		-17.5 (High Gain Mode) 2.5 (Low Gain Mode)

Front End Circuitry

The input signal to the radio is received through either one of the antenna connectors shown in the block diagram in Figure 1. The selection of the antenna is performed through the operations of the ISL3886 BBP/MAC and the RF Crosspoint Switch, U11. The use of the diversity switch helps to overcome the effects of multipath fading and antenna pattern nulls.

The received signal from the selected antenna is then fed to a bandpass filter/balun, U14, which effectively prevents out-of-band interfering signals from degrading the performance of the receiver. The input impedance of this filter is 50Ω unbalanced whereas the output is 100Ω balanced in order to correctly drive the differential receive input of the ISL3686A, ISL3686B Zero Intermediate Frequency (ZIF) chip, U7. The ZIF chip serves as a direct down conversion transceiver. It contains a Low-Noise Amplifier (LNA), a Quad Up/Down Converter, Synthesizer, Low-Pass Filter (LPF) and a Baseband AGC Receiver Amplifier (RX Amp), as well as a Transmitter Amplifier (TX Amp) for the Transmitter Signal Path (to be discussed later).

Low Noise Amplifier (LNA) and Up/Down Converter

The LNA is a fixed gain amplifier and is preceded by a 25dB attenuator controlled by the LNA High/Low pin. The purpose of the attenuator is to reduce the input signal when it approaches the threshold limit of -40dBm, to avoid overdriving the amplifier. Several dB of hysteresis is incorporated in the switching logic to ensure that this attenuator does not keep flipping in and out of the circuit.

After the LNA, the signal proceeds to the quadrature up/down converter, which performs a direct down conversion to baseband. The local oscillator for the down conversion mixers is derived from the ISL3084 RF VCO. The RF LO frequency is phase locked by the synthesizer to the 40MHz clock.

The RF VCO operates at twice the channel frequency. It is divided by two in a Flip Flop circuit to form accurate In Phase (I) and Quadrature (Q) LO signals at the channel frequency. They are therefore offset by ninety degrees in phase from each other and are equal in amplitude. These signals are applied to the I and Q balanced mixers. The other input to the mixers is the 2.412 to 2.484GHz RF signal from the LNA. One mixer therefore generates a balanced in-phase baseband receive signal and the other a balanced quadrature signal. They are designated RXI+, RXI-, RXQ+ and RXQ-.

Receive Amplifier and Automatic Gain Control

These analog differential outputs are fed through separate I and Q Low Pass Filters to establish the bandwidth of the system, attenuate out-of-band signals and prepare the signals for baseband processing. The signals then go through separate I and Q three stage cascaded variable gain amplifiers to raise the signal level to that necessary to drive the ISL3886 Baseband Processor/Medium Access Controller (BBP/MAC) Combo Chip. The gain of these amplifiers is controlled by the Receive Automatic Gain Control (RX AGC) circuitry. The RX AGC compensates for signal amplitude variations and allows for efficient I and Q A/D performance. Once in the BBP section of the BBP/MAC Chip, the in-phase signals enter the 6-bit I ADC and the quadrature signals enter the 6-bit Q ADC.

Baseband Overload Detector (BB_OVLD)

Normally, the LNA is in the high gain state. The Baseband Overload Detector circuit generates an analog voltage which is proportional to the output level of the Quadrature Up/Down Converter. This signal is fed back to the BBP/MAC chip which switches the High/Low Gain (LNA_HL) input of the ZIF to the low gain state if the input signal exceeds -41dBm in order to improve the dynamic range of the receiver (see further discussion under Low Noise Amplifier).

Demodulation Processing, General

There are two separate demodulators in the receiver, one for CCK signals and one for OFDM signals.

CCK Demodulation Processing and Multipath Mitigation

Once digitized in the BBP, the signals are then fed to the CCK demodulator section of the BBP/MAC and then to the I/O circuitry for decoding and descrambling of the data. The packet signals consist of a preamble, followed by a header and then the payload data to be received. The preamble uses Differential Binary Phase Shift Keying (DBPSK) Modulation that is a series of all ones with a known scramble sequence applied to aid in the acquisition process. In BPSK, only one bit is encoded into each data symbol. Each data symbol is multiplied by an 11-bit Pseudo Random Noise (PN) Barker Code sequence to provide the spreading function. The BBP correlates the PN sequence, adjusting its carrier and symbol timing to lock on to the signal and recover the packet data.

The receiver section operates on the RAKE receiver principle, which maximizes the Signal to Noise Ratio (SNR) of the signal by combining the energy of multipath signal components. The RAKE receiver is implemented with a Channel Matched Filter (CMF) using a finite-duration impulse response (FIR) filter structure with 16 taps. The CMF is programmed by calculating the channel impulse response (CIR) and mathematically manipulating the tap coefficients. Thus, the CMF compensates for channel distortion characteristics, such as multipath and optimizes the signal for minimum inter-symbol interference (ISI). Since the calculation of the impulse response is inaccurate at low Signal to Noise or in the presence of strong CW interference, the chip has thresholds programmed into the BBP/MAC registers that are set to substitute a default CMF shape under these conditions.

The RAKE receiver contains 16 correlation “fingers” that are evenly spaced at 1/2 chip intervals. It aligns correlation peaks on the “fingers” and sums them to optimize the SNR in the presence of multipath. The ISL3886 also employs a Decision Feedback Equalizer (DFE) at the output of the RAKE receiver that updates the CMF for the next receive bit. The combination of these two functions, acting in concert, optimizes the SNR of the received signal in the presence of multipath fading while minimizing the ISI of the signal.

Following the CMF and DFE, there are two types of correlators in the BBP/MAC: The first is a parallel matched filter correlator that correlates to the Barker sequence used in the preamble, header, and PSK data modes. These correlators are time invariant matched filters that despread the samples from the chip rate back to the original symbol rate. While despreading the desired signal, the correlator spreads the energy of any non correlating interfering signal, thus providing greater resistance to jamming.

The second form of correlator is the parallel correlator bank used for detection of the CCK modulation (5.5 or 11Mbps modes). At these rates, data is encoded into orthogonal PN sequences according to specific bits of data being transmitted instead of with a fixed Barker Code. Each correlator of the bank searches for a specific pseudo random sequence resulting in two decoded bits for 5.5Mbps and six decoded bits for 11Mbps. The detected output is then processed through the differential phase decoder to demodulate the last two bits of each symbol.

The packet header contains a start frame delimiter (SFD), other signal related data and a Cyclic Redundancy Check (CRC) for data error detection. The MAC processes the header data to locate the SFD, determines the mode and length of the incoming message and checks the CRC. The MAC then processes the packet data and sends it on through the Cardbus32 interface to the host computer. In addition, the host interface allows access to the radio’s memory and BBP/MAC host registers using memory read or write transactions. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

OFDM Demodulation Processing

The OFDM packet header contains two types of sync signals, Short and Long. The Short Sync signal is used for coarse carrier frequency tracking and estimation of the received signal strength. The Long Sync signal is used for fine frequency tracking and channel equalization.

The short and long sync correlators sample the signal for detection. Carrier tracking is based on samples from the correlator. The noncoherent digital AGC also takes its measurements at this stage to set up the gain for the proper backoff going into the FFT.

Once the signal has been acquired and tracking initiated, the time samples are then de-rotated by the carrier tracking loop to remove any effects of transmitter-receiver frequency offset. De-rotation uses a complex multiplication by a rotating vector generated in the carrier Numeric Controlled Oscillator (NCO).

The time samples are trimmed to remove the guard interval leaving 64 samples of complex baseband information out of the 80 that were sent. This step of throwing away 20% of the received signal energy and associated noise and corruption gives the system robust performance against multipath. The signal is transformed from the time domain into the frequency domain by a Fast Fourier Transform (FFT). This step takes 64 complex input samples and produces 64 complex output samples. The desired information is in the 48 of these samples that represents the 48 tones used for carrying the data modulation. Additionally, four of these samples are the pilot tones and they are extracted for carrier and timing tracking.

The 48 data tones and 4 pilot tones are equalized in amplitude and corrected in phase by the equalizer function, which uses the information learned during the training on the short and long sync symbols.

The 48 tones from the FFT are represented by 48 complex numbers generated by the FFT stage. They each represent a modulated set of data bits, each of them is a constellation point which is demapped by using multiple thresholds for the more complex modulations like 64QAM. Once each tone has been demodulated, the 48 sets of bits are reordered into a data symbol.

During the modulation process in the transmitter, data is interleaved on multiple carriers in order to randomize the position of possible data errors and thereby improve the performance of the Forward Error Correction (FEC) algorithm contained in the OFDM protocol. The output of the demodulator must be therefore re-ordered after demodulation in order to remove this interleaving. Following this process, decoding is done by the industry standard Viterbi algorithm. The same scrambler used in the transmitter is used to descramble receive data.

For more detailed information on demodulation processing please see ISL3886 datasheet [2] and also reference [18].

Other MAC Functions

The IEEE802.11g WLAN MAC protocol is implemented in the firmware. It supports basic service set (BSS) and independent basic service set (IBSS) operation under distributed coordination function (DCF). Low level protocol functions such as request to send (RTS)/clear to send (CTS) generation and acknowledgment, fragmentation and de-fragmentation, and automatic beacon monitoring are handled without host intervention. Active scanning is performed autonomously once initiated by a host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers. Additional firmware functions specific to access point applications are also available.

Transmit Signal Path

General

Data from the host computer is sent to the MAC through the miniPCI interface. Prior to any communication, however, the MAC sends a Request To Send (RTS) packet to the other end of the link and it receives a Clear to Send (CTS) packet in return. The MAC then formats the payload data packet (MPDU) by appending it to a preamble and header and sends it to the BBP.

As previously noted, the radio supports 12 different modulation modes:

- The two legacy data rates: 1 and 2Mbps
- The two CCK data rates: 5.5 and 11Mbps
- The eight OFDM data rates: 6, 9, 12, 18, 24, 36, 48 and 54Mbps

As with the receiver, the transmitter supports two modulation processes, one for CCK modulation and the other for OFDM. The legacy and CCK data rates are identical to those contained in the IEEE 802.11b standard and the NIC is therefore fully backward compatible in these modes.

CCK Mode Transmitter

The CCK mode transmitter is designed as a Direct Sequence Spread Spectrum (DSSS) PSK modulator. It supports CCK modulation for 5.5Mbps and 11Mbps, as well as DBPSK for 1Mbps and DQPSK for 2Mbps.

The preamble is always transmitted as the DBPSK waveform, while the header can be configured to be either DBPSK, or DQPSK, and data packets can be configured for DBPSK, DQPSK, or CCK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and makes the DBPSK to DQPSK or CCK switchover, as required.

In the 1Mbps DBPSK mode, the I and Q Channels are connected together and driven with the output of the scrambler and differential encoder. The I and Q Channels are then both multiplied with the 11-bit Barker word at the chip rate. The I and Q signals go to the quadrature upconverter within the ZIF chip to be modulated onto a carrier. Thus, the spreading and data modulation are BPSK modulated onto the carrier.

In the 2Mbps mode, the serial data is formed into bit pairs in the differential encoder as detailed above. One of the bits from the differential encoder goes to the I channel and the other to the Q channel. The I and Q channels are then both multiplied with the 11-bit Barker word at the chip rate. This forms QPSK modulation at the symbol rate (1Mbps) with BPSK modulation at the chip rate of 11Mbps.

The clear channel assessment (CCA) circuit implements the carrier sense portion of a carrier sense multiple access (CSMA) networking scheme. The CCA monitors the environment to determine when it is clear to transmit. The CCA circuit in the ISL3886 can be programmed to be a function of received signal strength (RSSI) [i.e. energy detected on the channel], quality metrics such as CS1 and SQ1, or various combinations of these. The decision of the MAC to transmit is based both on the existance of traffic to send and on the CCA indication. The CCA indication can be ignored, allowing transmissions independent of any channel conditions. The CCA, in combination with the visibility of the various internal parameters (i.e., energy detection measurement results), can assist the MAC in executing algorithms that can adapt to the environment. These algorithms can increase network throughput by minimizing collisions and reducing transmissions liable to errors. More information on the possible implementations of the CCA function may be found in the ISL3886 datasheet [2].

OFDM Transmitter

In order to create the OFDM symbols, the input stream of bits is partitioned into groups of 48 complex numbers in accordance with the scheme specified in the IEEE 802.11g

standard. Depending on the data rate selected, these are then mapped onto the individual tones as BPSK, QPSK, 16QAM or 64QAM modulation by the constellation mapper. This mapper also maps the four pilot tones.

Once the OFDM tones are fully specified, the 52 complex numbers representing them are transformed from the frequency domain to the time domain by a 64 point Inverse Fast Fourier Transform (IFFT) operation. The missing tones are indicated by 0 amplitude complex numbers. The output of the IFFT is a set of 64 complex numbers that represent the time domain amplitude and phase of the signal representing the symbol.

The OFDM symbols are extended to 80 samples by duplicating the last 16 samples and appending them to the beginning of the symbol. This creates a guard interval and also allows the symbol to be demodulated with a slight timing offset. This signal is passed to a pair of balanced output Digital to Analog Converters (DAC's) for conversion to analog signals which are then output from the chip. One DAC generates the In Phase (I) signal whereas the other generates the Quadrature (Q) signal.

Transmit Digital To Analog Converters (DAC's)

After being converted from digital to an analog signals by the I and Q Transmit DAC's in the BBP/MAC, the outputs are routed to the ISL3686A/B ZIF chip. These balanced signals are denoted TXI+, TXI-, TXQ+ and TXQ-.

The I and Q signals are fed through separate Low Pass Filters (LPF's), which attenuate unwanted aliasing signals generated in the DAC's. Note that one of the filter poles is determined by external shunt resistors and capacitors on the PCB (R43-C108, R48-C118, R51-C122 and R53-C123), while two additional complex poles are located within the ZIF chip. Since the DAC outputs are current sources, the resistors also determine the output voltage from the DAC's and therefore the drive level to the up-converting mixer.

Up-Converting Mixer and Transmit Amplifier

The output of the LPF's are routed to the Quadrature Up Converter, which translates the baseband signal to the 2.45GHz ISM band by mixing it, in a pair of balanced modulators, with the I and Q Local Oscillator signals derived from the external RF VCO .

Recall that the RF VCO operates at twice the channel frequency. The VCO signal is divided by two in a Flip-Flop circuit thereby generating equal amplitude and precise 90^{o} phase shifted I and Q balanced LO signals. Further details of this process are discussed in the Synthesizer and Receiver sections.

The 2.45GHz transmit signal is then amplified in the Transmit Amplifier and appears on the TX_Out pin of the ZIF chip as a 50Ω unbalanced signal.

RF Power Amplifier and Transmit/Receive Switching

The Transmit output signal from the ZIF chip is then fed to the ISL3980 Power Amplifier (PA).

In CCK and legacy 1 and 2Mbps modulation modes, the transmit signal's peak to average power ratio (PAR) is only 2.5dB. The PA can therefore be operated only slightly below its 1dB compression point, thereby maximizing its efficiency. The PA delivers +17dBm typical power output at the RF test point while meeting the required IEEE 802.11 adjacent channel power ratio (ACPR) specifications of less than -30dBc 1^{st} sidelobe and less than -50dBc 2^{nd} side lobe levels. In the various OFDM modulation modes however, the PA output power must be backed off further to ensure sufficient linearity to meet the more stringent Error Vector Magnitude (EVM) requirements of this more complex modulation. The degree of necessary backoff increases with modulation complexity. 64QAM modulation has a PAR of 13dB and therefore requires the highest degree of backoff. Power output in this mode is typically +12.5dBm.

After the RF PA, the signal travels through a Low Pass Filter which attenuates unwanted signals such as harmonics. The signal is then routed through the RF Crosspoint Switch, U8, to the built in antennas.

RF Crosspoint Switch

The RF Crosspoint Switch, U8, provides the dual function of both Transmit/Receive and Antenna Diversity switching. Compared to earlier PRISM designs, this switch offers two advantages: lower price and lower RF Insertion Loss. The operation of the switch is determined by the state of two complementary signal lines, ANT_SW and ANT_SW* which are controlled by the BBP/MAC IC, U1. Under one set of bias conditions, the Receive signal is routed to ANT1 and the Transmit signal is routed to ANT2. Under the reverse set of conditions, the Receive signal is routed to ANT2 and the Transmit signal is routed to ANT1. Therefore, in order to transmit and receive from the same antenna, these control lines must change states synchronously with the PE2 signal, i.e. the transmit/receive control line of the NIC. Alternately, the phase of this signal may be inverted by the BBP/MAC in order to change to the other antenna. The switch is fabricated in PHEMPT MOS technology and therefore draws no current on its control lines.

Transmitter Automatic Gain Control (TX AGC) Circuitry

The TX AGC maintains essentially constant transmitter power output irrespective of the operating channel. It also compensates for differences in power gain due to either IC to IC gain variations or supply voltage changes.

The ISL3980 Power Amplifier contains a power detector circuit which produces a voltage proportional to the output power. An Analog to Digital Converter (ADC) in the BBP/MAC chip converts this analog signal to an unsigned 2 digit hex number (more about unsigned hex numbers below). During initial testing of a transmitter, the power output is monitored on an

external RF Wattmeter while observing the spectral regrowth levels on a Spectrum Analyzer. In each modulation mode, this regrowth is compared to a limit case mask which is IEEE 802.11g compliant. The power output on each channel is set at a maximum possible level commensurate with compliance with this mask. The optimum Power Detector (hex) values are noted for each channel and then flashed back into the Production Data Area (PDA) in the non-volatile memory of the device under test to serve as the reference level for the TX AGC loop. In practice, to minimize the test time, it is not really necessary to measure the power output on each channel. Rather, we recommend testing on only four channels: 1, 6, 11 and 14. The Intersil Automatic Manufacturing Test (IMT) software then computes a best fit curve of power vs. frequency and stores the Production Data Area (PDA) values for each channel and modulation mode.

A matrix of PDA values are created and stored for each combination of channel and modulation mode. Recall that the PA backoff levels need to be independently set for each of the various modes as noted above in the circuit description of the Power Amplifier. Therefore, separate PDA entries are created for Legacy/CCK, BPSK OFDM, QPSK OFDM, 16QAM OFDM and 64QAM OFDM for each channel. The IMT software efficiently generates and stores this matrix in the NIC's EEPROM while maintaining a total test time per NIC of approximately two minutes.

A feedback signal, which controls the gain of the Transmit Amplifier in the ZIF, is stored in the Integrator register in the BBP/MAC as a two digit unsigned hex number (more about unsigned hex numbers below). This is converted to an analog signal in a Digital to Analog Converter (DAC) circuit in the BBP/MAC and is then applied to the TX_AGC pin of the ZIF chip to control its gain. During the beginning of the preamble portion of the packet header, the circuitry in the BBP/MAC compares the level in the power detector register to the optimum level stored in non-volatile memory for that particular channel and either increments or decrements the integrator register until the optimum level is obtained. The transmitter power is therefore set at the same optimum power level as originally determined during initial transmitter testing.

Selection Of The Values For The Resistors In The Power Detector Voltage Divider Circuit

Normally, the values of R33, R27 and C67 specified in the ISL38601M Reference Design are optimum for correct radio operation. These values are somewhat critical for proper circuit operation, so if any circuit changes to the output circuit of the PA are contemplated (e.g. a change in the vendor of the Low Pass Filter), the optimization should be repeated.

The Power Detector circuit is used to perform two separate and distinct functions:

- Transmitter Automatic Gain Control
- Balancing of the I and Q channels of the ZIF to ensure optimum EVM

The values selected must therefore optimize the operation of both circuits.

During one part of the IMT test, the NIC is placed in a special calibration mode and I and Q channel signals are applied to the ZIF, both singly and in combination. The PA Detector output is monitored and the signal levels in the I and Q channels are individually adjusted to provide essentially perfect balance of these outputs at the final operating frequency. We have therefore achieved a square geometric I-Q pattern in vector space which ensures minimum EVM in the radio under complex modulation conditions. These one-time calibration values are then stored in the EEPROM and "remembered" by the NIC.

The following are the optimization criteria for the resistor values:

- The sum of the values of R33 and R27 should be greater than 50kΩ
- 1% tolerance resistors and a 5% tolerance capacitor should always be used in this circuit
- When operating in CCK 1Mbps mode into a 50Ω dummy load, the ratio of the resistors should be adjusted such that the peak voltage at the junction of the resistors as set by the IMT software is 1.2 ±0.15V. A fairly large sample of radios should be checked to ensure proper centering of this voltage.
- The TX AGC ADC in the BBP/MAC is a half-rail device, so the peak voltage at the junction of the resistors should not exceed 1.5V.
- The value of C67 should be adjusted such that the time constant of R27*(C67 + stray PC Board capacity) is 350ns. The stray capacity of the trace on the ISL38601M Reference Design has been measured and found to be 4pF.

Unsigned Hex Numbers

The analog-to-digital (A/D) and digital-to-analog (D/A) conversion processes used in the PRISM TX AGC loop store values as unsigned hex numbers in the BBP/MAC registers. In these registers, 80h is equivalent to an analog voltage of zero volts. For register values between 80h and FFh, the equivalent analog voltage increases monotonically. FFh represents approximately a mid scale analog voltage (say 1.5V). The next register increment, i.e. rollover to 00h, continues this smooth monotonic increase. 7Fh (i.e. one increment below 80h)

represents a full scale analog voltage (say 3.0V). A graphic representation of this is shown in Figure 4.

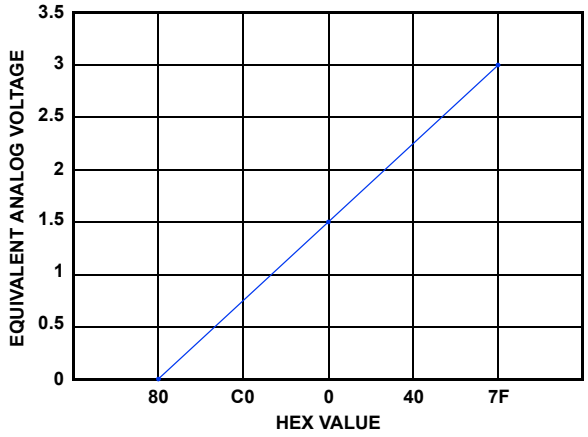

FIGURE 4. UNSIGNED HEX VALUE vs ANALOG VOLTAGE

Synthesizer Circuitry

There is only one local oscillator in the ISL38601M PRISM GT WLAN , the ISL3084 RF VCO. The VCO is phase locked to the 40MHz crystal controlled clock by the synthesizer and therefore constitutes an accurate channel frequency reference for the radio. Overall frequency accuracy is ±25ppm. The LO frequency range is 4824 to 4968MHz in two MHz steps. The LO frequency is always equal to twice the channel frequency so that the corresponding frequency range of the radio is 2412 to 2484MHz in one MHz steps. The RF LO output is internally buffered within the VCO to reduce frequency pulling effects due to transients involved in the T/R switching process.

Three data lines from the BBP/MAC program the synthesizer: Latch Enable (LE), Serial Clock (SCLK), and DATA. These can be monitored at test points C, D and E, respectively. The synthesizer program consists of four 20 bit data words each followed by a Latch Enable. Data is permanently latched in the synthesizer registers on the falling edge of the LE signal. See the ISL3686A/B datasheet [3,4] for further programming information.

The loop filter in the PLL, consisting of C104, C105, R41, R42 and C107, largely determines the transient response of the synthesizer. The 3dB bandwidth of the loop filter is approximately 40kHz.

Voltage Regulators

An integrated Triple Low Dropout Linear Voltage Regulator/Power-On Reset circuit, U3, an ISL6411, is used to provide filtering and isolation from the 3.3V input supply. Another advantage of using voltage regulators is a savings in overall supply current, as most of the chips consume less current at a 2.84V operating point than at 3.3V.

A total of three regulators are contained in this device. A Low Noise 2.84V output, designated VCCB, supplies voltage to the synthesizer, RF VCO and 40MHz Clock. A second 2.84V regulator, designated VCCA supplies voltage to the rest of the ZIF Chip as well as to the analog circuits in the BBP/MAC. A third output, the 1.8V Core regulator supplies the voltage to the digital portion of the BBP/MAC. The Input/Out and PHY pins however are operated from and referenced to the 3.3V computer bus.

Because of this dual set of voltages being applied to the BBP/MAC, it is important to time sequence the application and removal of the 1.8V core supply such that it always is applied before and removed after the 3.3V supply. This prevents a large burst of current from flowing into the I/O cells during the period when both voltages are not present which could effect the reliability of the device. When power is first applied, the FAULT pin of the ISL6411, U3-15 will be low since the 1.8V core voltage has not yet stabilized. Transistor, Q1 and MOSFET Q2 will both be off and no 3.3V will therefore be applied to the BBP/MAC. When the 1.8V core supply reaches 85% of its final value, i.e. 1.53V, the FAULT pin will switch high and both Q1 and Q2 will conduct thereby applying 3.3V to the BBP/MAC. On power down, the sequence will reverse.

The ISL6411 also contains a Power-Up-Reset circuit which supplies a nominal 25ms reset pulse to the BBP/MAC upon initial power-up. The length of the pulse is controlled by the value of C86. The 25ms length ensures that this reset pulse will be substantially longer than the time it takes for all voltage regulators to stabilize. Proper initialization of the BBP/MAC will therefore occur.

Explanation of Test Points

All measurements were taken using the “Continuous Transmit” or “Continuous Receive” features of the diagnostic software. Unless otherwise noted, spectrum measurements included in this section were obtained using a Hewlett-Packard 54006A 500Ω probe and 11742A coaxial blocking capacitor and do not indicate the actual amplitude of the signal due to losses associated with the probe. The 11Mb (CCK) mode was used.

Many of the signals are differential (i.e. balanced with respect to ground). These are denoted by + (plus) and (minus) symbols following the signal name (e.g. RX I+ and RX I-)

Test Points H and J

Transmit I (lower trace) and Q (upper trace):

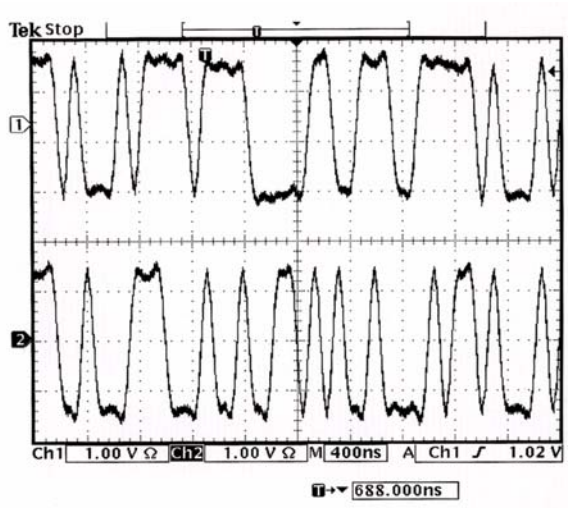

FIGURE 5. TX I AND Q DIFFERENTIAL SIGNALS

Figure 5 shows the differential Quadrature Transmit signal (total Q signal) and the differential In-Phase Transmit signal (total I signal) coming out of the BBP/MAC chip. These points were captured using the digital scope by monitoring test points H and J (reference Figure 2) through differential probes.

Test Point A

RF Transmit Signal (taken through the MAIN Antenna jack):

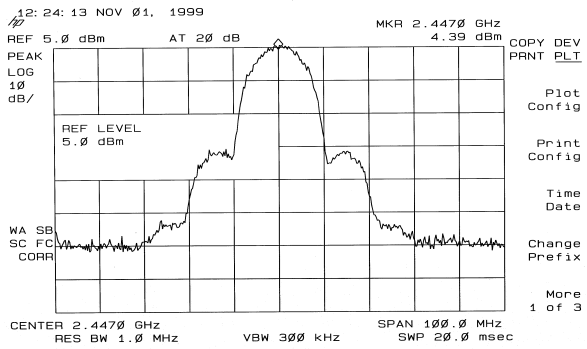

FIGURE 6. TRANSMITTED 2.4GHZ CCK SIGNAL SPECTRUM, CH8 (TEST POINT E)

The MAIN Antenna connector can be used to hook up a Spectrum Analyzer or an RF Wattmeter for RF evaluation.

Figure 6 shows the transmitter output of the card. The center frequency of this signal is 2412-2484MHz depending on the channel of operation (see Table 2). The output power of the signal on channel 8 is approximately +17.5dBm. The peaks of the sidelobes of the output spectrum (i.e. the spectral regrowth) are normally adjusted by the TX AGC to be a minimum of 30dB below the peak of the spectrum for the 1st sidelobes or 50dB for the 2nd sidelobes, whichever occurs first, per requirements of IEEE 802.11.

Test Point B

RF local oscillator (LO) (taken with 1kΩ RF probe):

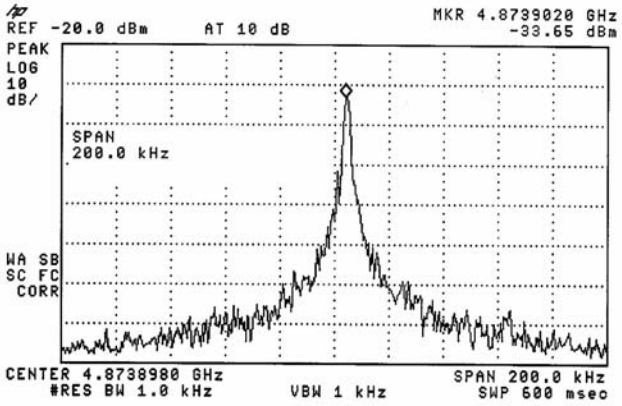

FIGURE 7. RF LOCAL OSCILLATOR OUTPUT AT CHANNEL 6 (TEST POINT B)

The VCO output is locked at twice the channel frequency (e.g. 4874MHz for CH6) as shown in Figure 7. The output power at test point B is approximately -4dBm. The attenuation in the 1K probe is approximately 26dB so the level indicated on the Spectrum Analyzer is -30dBm. Ideally, the tuning voltage of the VCO, when locked, falls between 0.5V and 2.2V.

Due to the ± 25ppm tolerance of the 40MHz reference clock, the RF Local Oscillator output may have a slight frequency error. Instead of locking at exactly 4874MHz on channel six, the RF LO output might instead be locked by as much as 61kHz off of this frequency.

Test Points F and G

Receive I (lower trace) and Q (upper trace):

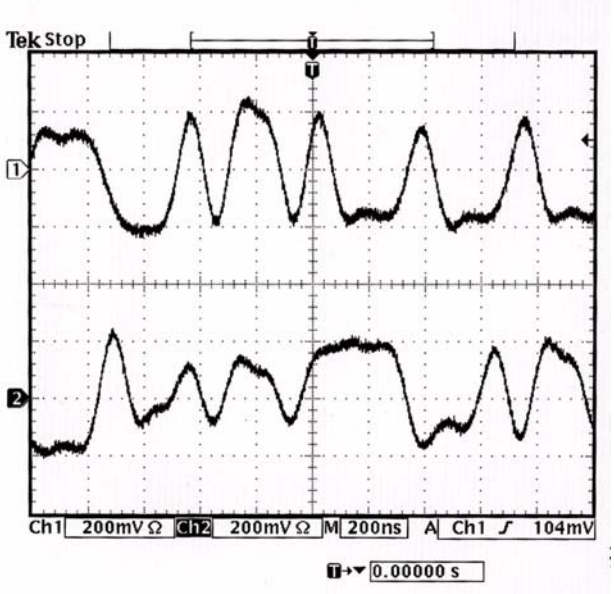

FIGURE 8. RECEIVE I AND Q DIFFERENTIAL SIGNALS

The receive In-phase and Quadrature (I and Q) signals, shown in Figure 8, are the demodulated lowpass-filtered data coming

out of the ZIF chip. The data was taken by using a pair of differential probes and monitoring the output from the test points listed below on a digital storage oscilloscope.

RXI+ and RXI- can be monitored at Test Point F RXQ+ and RXQ- can be monitored at Test Point G.

Synthesizer Data, Test Points C, D, and E

Shown in Figure 9 is the synthesizer data taken from a Logic Analyzer while transiting to Channel 6. The signals captured are the Latch Enable (LE), Serial Clock (SCK), and Data for the synthesizer. Each word of data is latched into the synthesizer register immediately following the LE high to low transition. Note that there is actually a fourth block of data transmitted followed by an LE signal, however this occurs off the screen and is therefore not visible in order to provide a clearer, more detailed display.

These 20 bit data words are binary ones and zeroes that control the operation of the A and B counters, Charge Pump, and Divide by 32/33 Prescaler. The programmed values for the A and B counters are unique to the channel selected.

Please see the ISL3686A, ISL3686B [3,4]datasheet for complete programming details. More information is also discussed in the Synthesizer section above.

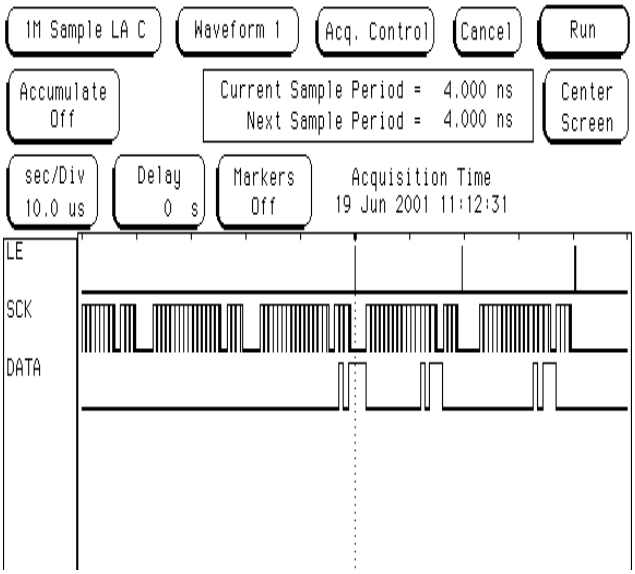

FIGURE 9. SYNTHESIZER DATA FOR CHANNEL 6

TX Automatic Gain Control

Test Point K

The Transmitter AGC level (TX AGC), sometimes referred to as Automatic Level Control (ALC), was taken at the 1Mbps data rate for various CR 9 low byte register settings in the Continuous Transmit mode and the following results were obtained.

TABLE 2. TX AGC VOLTAGE vs INPUT SIGNAL

TX AGC DECIMAL/HEX SETTING	TRANSMITTER AGC VOLTAGE (V)	OUTPUT POWER (dBm)
-6/FA	1.045	19.6
11/0B	1.186	19.0
27/1B	1.320	18.0
39/27	1.420	17.0
60/3C	1.595	15.0
88/58	1.024	12.0
105/69	1.963	10.0
113/71	2.029	9.0
121/79	2.095	8.0
127/7F	2.142	7.3

As the hex value of the Integrator register setting is increased the TX AGC voltage increases however the power decreases.

When viewing the output on the Spectrum Analyzer, the AGC's positive rail (decimal 127/hex 7F) produces maximum TX AGC voltage, a signal with no regrowth and very little power as this is the minimum gain point. Conversely, the AGC's negative rail (decimal -128/hex 80) produces essentially zero volts of TX AGC and a signal with severe regrowth (heavily clipped) and a high output power.

Receiver Automatic Gain Control (RX AGC)

Referencing Figure 10, the upper trace is the receive baseband signal monitored at the I output using a differential probe bridged between Test Points F (see Figure 2). The lower trace is the BBAGC+ level, which is taken out of the Baseband/MAC Combo Chip (Test Point "L" in Figure 3). This level increases as the input signal level is increased.

In the upper trace, observe the transistion from noise to the header of a packetized signal. Note that the response time of the AGC is very fast with only an extremely short overshoot and that it stabilizes in level right at the beginning of the packet.

This measurement can be made in a sensitivity setup by calibrating the transmitter system for -20dBm output and then

varying the step attenuators. The voltage can then be monitored on an oscilloscope as shown above.

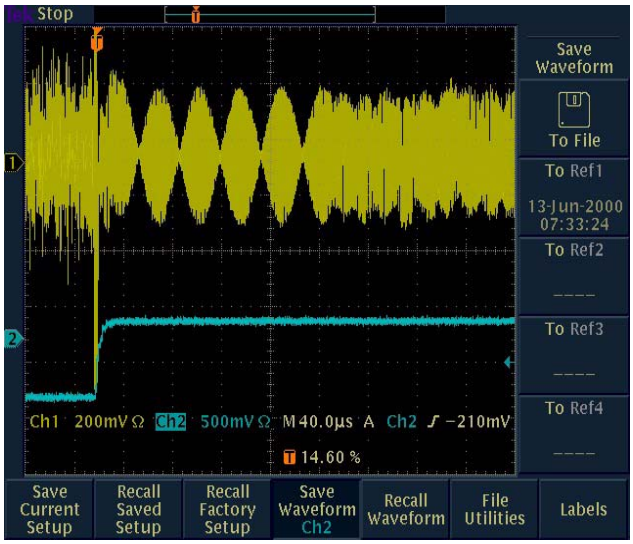

FIGURE 10. TEST POINT G: RX I DIFFERENTIAL SIGNAL vs RX AGC

I-Q Baseband Spectrum (0-20MHz)

Shown in Figure 11 is a typical baseband spectrum of the in-phase signal (I) taken on noise spanning from 0-20MHz. A plot of the Q spectrum would indicate similar results. The plot was obtained by monitoring test point F (ref Figure 2) through a differential probe.

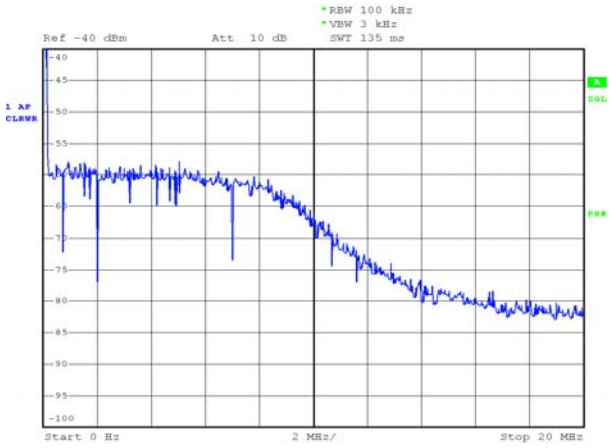

FIGURE 11. I SIGNAL BASEBAND PLOT FROM 0-20 MHz

A key feature in this spectrum plot is the noise rise due to the front end gain. The noise in the active bandwidth region spanning from zero to 8MHz is approximately 20dB above the residual background noise level at higher frequencies. This is indicative of a well designed radio gain distribution since the front end noise greatly exceeds the residual noise. The residual noise will therefore not degrade the radio's sensitivity. Note also that this spectrum is completely spurious free in the active region. This ensures optimum radio sensitivity.

I-Q Constellations

Recall that there are four different OFDM carrier modulation modes in the ISL38601C radio: BPSK, QPSK, 16QAM and 64QAM. Figure 12 shows a typical BPSK transmitter constellation pattern measured on an Agilent E4804A Vector Signal Analyzer (VSA). The constellation is colored red. Pilot tones are not visible since they lie on top of the constellation. Note that the Constellation is somewhat stretched in the "I" direction and flattened in the "Q" direction. This is due to the nature of the decoding algorithm in the VSA (and similar instruments) which uses the pilot tones to remove phase variations.

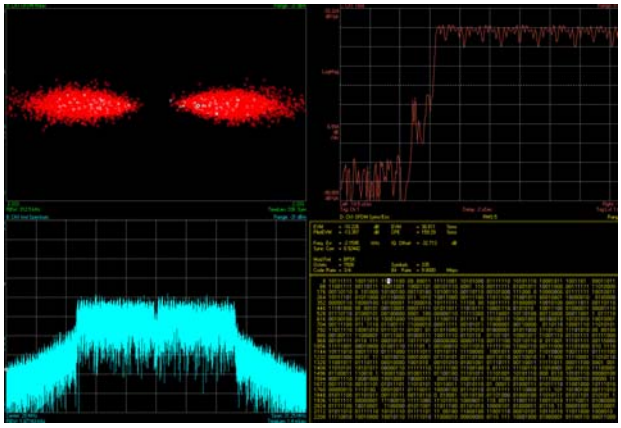

FIGURE 12. OFDM BPSK I-Q CONSTELLATION

Figures 13 through 15 show typical constellations for the other three OFDM modulation modes. The pilot tones are colored white. Two pairs of these tones overlap so only two white dots are visible. Note the low EVM and therefore high fidelity of the 64QAM constellation.

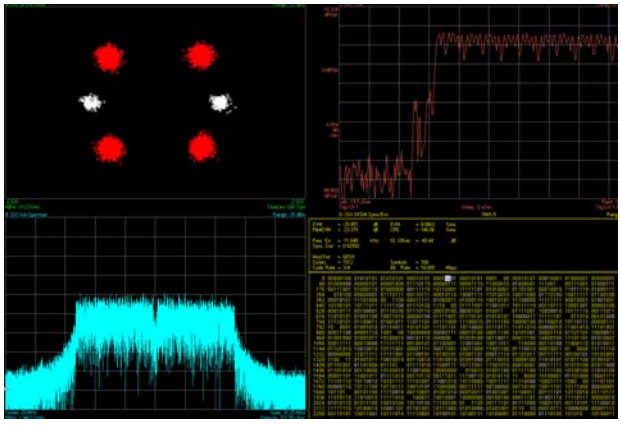

FIGURE 13. OFDM QPSK I-Q CONSTELLATION

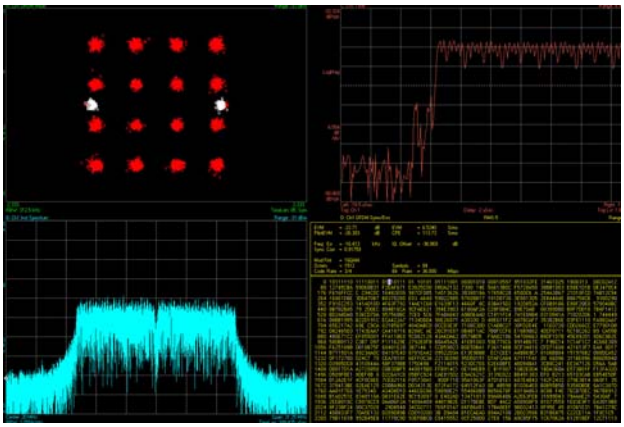

FIGURE 14. OFDM 16QAM I-Q CONSTELLATION

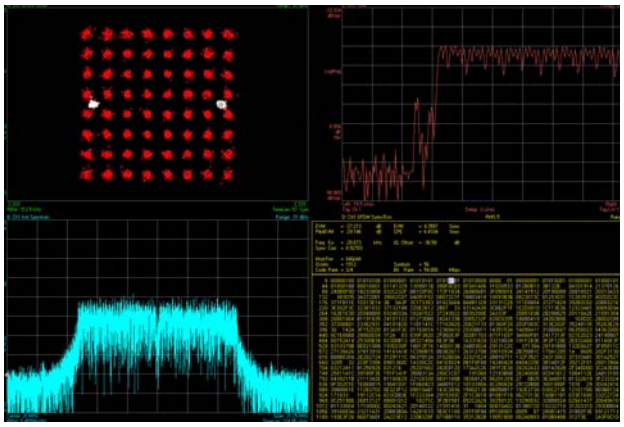

FIGURE 15. OFDM 64QAM I-Q CONSTELLATION

Figure 16 shows a spectral plot of the 11Mbps CCK waveform taken on CH8. Note that while the OFDM waveforms are a flat top or “Bartshead” spectrum, the CCK spectrum is significantly more rounded. This is characteristic of both the CCK and “legacy” 1 and 2Mbps spectra.

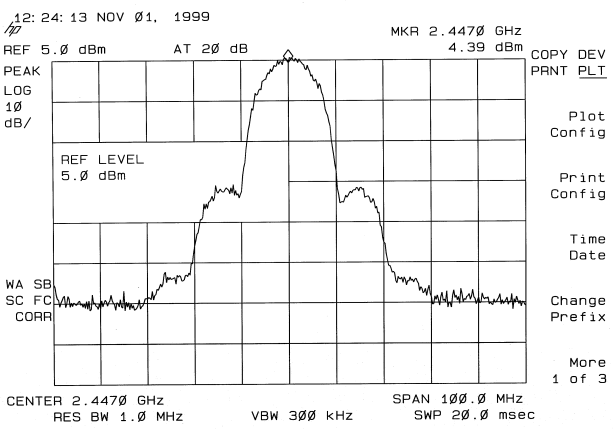

FIGURE 16. TRANSMITTED 2.4GHz CCK SIGNAL SPECTRUM, CH8 [SAME AS FIGURE 7] (TEST POINT E)

IEEE 802.11 International Agreement and Frequency Assignments

TABLE 3. - IEEE 802.11g CHANNELS

CHANNEL NUMBER	CHANNEL FREQUENCY	GEOGRAPHIC USAGE
1	2412MHz	US, CA, ETSI, TELEC
2	2417MHz	US, CA, ETSI, TELEC
3	2422MHz	US, CA, ETSI, TELEC
4	2427MHz	US, CA, ETS, TELECI
5	2432MHz	US, CA, ETSI, TELEC
6	2437MHz	US, CA, ETSI, TELEC
7	2442MHz	US, CA, ETSI, TELEC
8	2447MHz	US, CA, ETSI, TELEC
9	2452MHz	US, CA, ETSI, TELEC
10	2457MHz	US, CA, ETSI, FR, SP, TELEC
11	2462MHz	US, CA, ETSI, FR, SP, TELEC
12	2467MHz	ETSI, FR, TELEC
13	2472MHz	ETSI, FR, TELEC
14	2484MHz	TELEC

KEY: US = United States. CA = Canada, ETSI = ETSI countries (except France and Spain), FR = France, SP = Spain, TELEC=Japan

The preceding table delineates the IEEE 802.11 channels and their corresponding center frequencies. Information contained in Table 3 is deemed to be accurate, however local regulatory authorities should be consulted before using such equipment.

FCC Information to User

This product does not contain any user serviceable components and is to be used with approved antennas only. Any product changes or modifications will invalidate all applicable regulatory certifications and approvals.

FCC Electronic Emission Notices

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference
2. This device must accept any interference received, including interference that may cause undesired operation.

FCC Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

Operation of this equipment in a residential area may cause harmful interference in which case the user will be required to correct the interference at his own expense.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Export Restrictions

This product or software contains encryption code which may not be exported or transferred from the US or Canada without an approved US Department of Commerce export license.

FCC Guidelines for Human Exposure

In order to comply with RF exposure limits established in the ANSI C95.1 standard, the user is advised to maintain a distance of at least 1cm from the antenna of this device when in use. If the antenna is positioned less than 1.0cm from the user, it is recommended to limit the exposure time.

WARNING! Any changes or modifications of equipment not expressly approved by Intersil could void the user's authority to operate the equipment.

Handling and Processing Moisture Sensitive Surface Mount Devices

Certain plastic encapsulated surface mount devices (SMDs) if not handled properly can incur damage during the solder reflow attachment process to printed circuit boards (PCBs).The damage occurs as a result of internal package cracking (commonly referred to as popcorn cracking) and/or delamination between internal package interfaces.

The root cause of this type of failure mechanism is the rapid heating of the moisture absorbed within the plastic encapsulant. All plastic packages absorb moisture. During typical solder reflow operations when SMDs are mounted onto a PCB, the entire PCB and device population are exposed to a rapid change in ambient temperature. Any absorbed moisture is quickly turned into superheated steam. This sudden change in vapor pressure can cause the package to swell. If the pressure exerted exceeds the flexural strength of the plastic mold compound, then it is possible to crack the package. Even if the package does not crack, interfacial delamination can occur.

If a particular package style is determined to be moisture sensitive, then the product must be shipped in dry pack. The dry pack bag is a tough, moisture resistant bag. Placed inside a dry pack bag along with predetermined amount of desiccant and a humidity sensitive indicator card. Upon opening a dry pack bag with product, the user needs to check 2 items: the seal date on the label, and the moisture indicator from within the bag. If the humidity indicator card shows >20% RH, the product may need to be re-baked prior to reflow.

If a rework of a PCB with moisture sensitive SMDs is required, special precautions must be observed. Should the rework require complete exposure of the PCB to reflow conditions, then the manufacturer needs to take into account the shortest floor life of any moisture sensitive SMD on the board. If the floor life has been surpassed, then the entire board should be re-baked.

The following table gives the moisture level ratings of the various IC's used in the PRISM GTchipset. If the "Max Exposure Time Without Re-Baking" interval is exceeded, the devices must undergo a re-baking procedure before soldering them on a PC board [8]. Although this data is accurate as of the time of publication of this document, please consult the datasheets of the individual IC's for the latest up-to-date information.

TABLE 4. MOISTURE RATING OF IC'S

IC	MOISTURE LEVEL	MAX EXPOSURE TIME WITHOUT RE-BAKING
ISL3084	Level 1	No time limit
ISL3686A, ISL3686B	Level 3	168 Hours
ISL3886	Level 2	1 year
ISL3980	Level 2	1 year
ISL6411	Level 3	168 Hours

References

For Intersil documents available on the internet, see web site http://www.intersil.com/
Intersil AnswerFAX (321) 724-7800.

1. FN8081 datasheet, Intersil Corporation, "ISL38601M"
2. FN8070 datasheet, Intersil Corporation, "ISL3886"
3. FN8065 datasheet, Intersil Corporation, "ISL3686A"
4. FN8067 datasheet, Intersil Corporation, "ISL3686B"
5. FN8055 datasheet, Intersil Corporation, "ISL3980"
6. FN5042.1 datasheet, Intersil Corporation, "ISL3084"
7. FN9081.1 datasheet, Intersil Corporation, "ISL6411"
8. TB382 Technicl Brief, Intersil Corporation, "Measurement of WLAN Receiver Sensitivity"
9. TB363 Technical Brief, Intersil Corporation, "Guidelines for Handling and Processing Moisture Sensitive surface Mount Devices"
10. AN9623 Application Note, Intersil Corporation, "Packet Error Rate Measurements Using the PRISM Chip Set"
11. AN9850 Application Note, Intersil Corporation, "Complementary Code Keying Made Simple"
12. AN9829 Application Note, Intersil Corporation, "Brief Tutorial on IEEE 802.11 Wireless LAN's"

13. AN9633 Application Note , Intersil Corporation, “Processing Gain for Direct Sequence Spread Spectrum Communication Systems and PRISM“
14. AN9895 Application Note, Intersil Corporation “Multipath Measurements in Wireless LANs”
15. TB389 Technical Brief “Surface Mount Guidelines for MLFP Packages”
16. TB337 Technical “A Brief Tutorial on Spread Spectrum and Packet Radio”
17. AN9820 Application Note “A Condensed Review of Spread Spectrum Techniques”
18. “Effects of Physical Layer Impairments on OFDM Systems” by Bob Cutler, RF Design, May 2002
19. “The Principals of OFDM” by Louis Litwin and Michael Pugel, RF Design, January 2001

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

© 2018 Renesas Electronics Corporation. All rights reserved.

Colophon 7.0