PCB Design and Layout Considerations for Adesto Memory Devices

March 8, 2018

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Revision History

Revision Number	Date	Tasks
A1	March 8, 2018	PCB Design Guide Application Note initial release.

Table of Contents

1. INTRODUCTION

The Adesto family of memory devices supports a variety of package types such as standard SOIC, UDFN, WLCSP and BGA. Each of these package types has their own unique PCB design requirements. This document describes the PCB design guidelines for each package type, both for power/ground, signalling, and special cases as described below.

Concepts described in this document include:

- Placement of decoupling capacitors between power and ground.
  - The placement differs based on the package type. SOIC capacitor placement is different from UDFN or BGA placement.
  - Methodology also differs depending on the number of PCB layers.
- Steps required to ensure signal integrity. Specific rules should be followed to minimize any signal integrity issues.
- Special cases.
  - Information on how to handle scenarios such as having multiple devices in parallel (populated and unpopulated).
  - Reset signal issues.
  - Integration of debug support such as test points.

2. OVERVIEW OF CAPACITIVE DECOUPLING

This section provides the basics of capacitive decoupling and describes both an overview of why decoupling capacitors are necessary, and the placement of these capacitors relative to the VCC and GND pins of an Adesto memory device.

2.1 What is Capacitive Decoupling and Why Do We Need It?

The VCC and GND pins of Adesto memory devices are connected to a power supply with conductive traces and other structures on the PCB (pads, traces, vias, solid copper layers etc.) These traces have a finite impedance. The reactive components (trace inductance and capacitance) represent parasitic effects that affect the efficiency of power distribution from the power supply to the variety of devices on the PCB.

During normal operation of the device, the amount of current drawn varies significantly. Typically, on the rising and falling edges of the clock (external or internal), many transistors inside the device are switching simultaneously, drawing a significant amount of current in short period of time (significantly larger than in steady-state operation). These current surges result in a voltage drop across the parasitic impedances of the PCB structure that manifests itself as voltage fluctuations, voltage spikes and/or glitches on the VCC, or ground bounce on the GND pins.

Depending on the amplitude of these voltage fluctuations, the consequence could be signal integrity degradation. This can result in a wide-range of failures, including unreliable device operation due to: setup and hold time violations, logical 1's and 0's erroneously altering states, false triggering of the data signals if the glitches occur on the clock signals, incorrectly stored data in the memory cells, increased jitter, undesired resetting of the device, increased EMI etc.

To minimize the negative effects of these voltage fluctuations, Adesto recommends placing one or more decoupling capacitors between the VCC and GND pins of each memory device in the system, physically as close as possible to the pins of the device (minimizing trace lengths and therefore their parasitic effects).

The value of the decoupling capacitor is device dependent. The typical value will be 1 μF, but certain high-performance devices may require a larger decoupling capacitor, or pairs or capacitors, such as 4.7 μF and 100 nF capacitors in parallel.

The decoupling capacitor works as a local energy storage, supplying large transient currents as necessary. The presence of a decoupling capacitor in close proximity to the VCC and GND pins of the device compensates for the voltage drop caused by parasitic effects in the power supply and PCB structures (parasitic inductance, capacitance of the traces, vias).

According to capacitor equation, $i(t) = CdV(t)/dt$, the voltage drop between the VCC and GND pins results in current being drawn out from the capacitor and supplied to the device. When the amount of capacitance 'C' is large enough, sufficient current is supplied to minimize the range of the voltage drop.

Figure 1 shows the effect of the decoupling capacitor when placed very close to the Adesto memory device. The decoupling capacitor acts as a high-pass filter for noise and fast voltage variations and it bypasses the large inductance of the PCB traces from the power supply and its bulk capacitors. This reduces the voltage drop associated with fast switching of the internal transistors. The decoupling capacitor also significantly shortens the length of the current return path, minimizing current loops and as a result decreasing EMI and noise susceptibility, and electro-magnetic radiation.
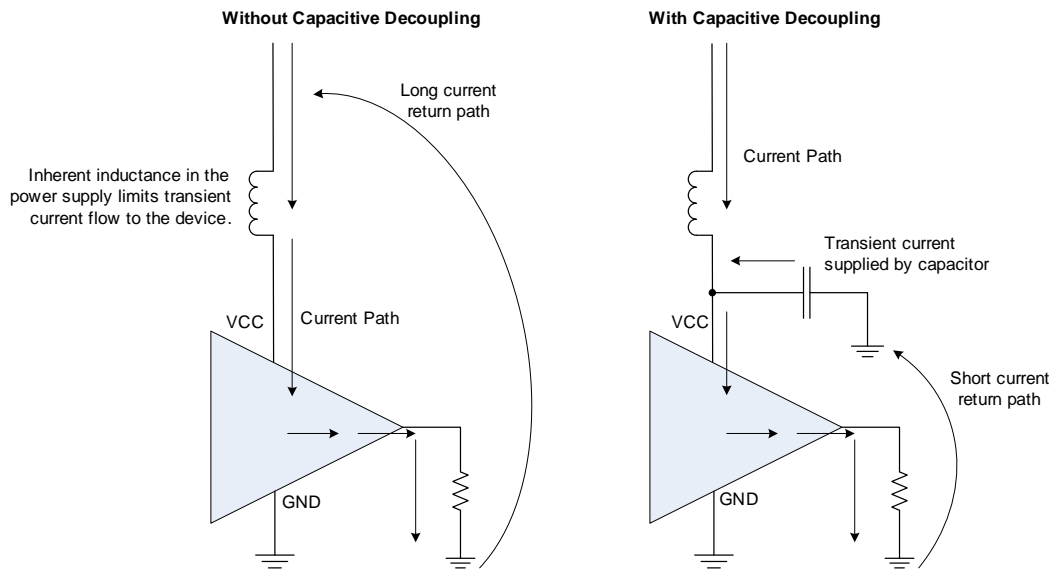
Without Capacitive Decoupling

Long current return path

Inherent inductance in the power supply limits transient current flow to the device.

VCC

Current Path

GND

With Capacitive Decoupling

Current Path

Transient current supplied by capacitor

VCC

Short current return path

GND

Figure 1. Capacitive Decoupling and Current Return Path Comparison

2.2 Decoupling Capacitor Layout

The VCC and GND pins of the Adesto memory device connect to each side of the decoupling capacitor. The proximity of these connections to the capacitor is very important and can have a dramatic effect on the efficiency of the capacitor and its ability to supply the transient current required to offset the voltage fluctuations described in the previous section.

As a general rule, traces should be as short as possible, and vias should be as close as possible to the decoupling capacitors.

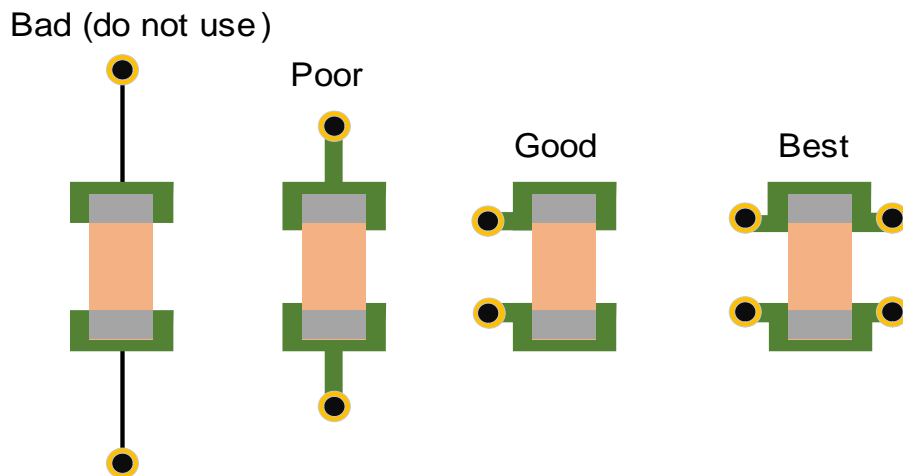Figure 2 shows some capacitor layouts from worst to best.

Bad (do not use)

Poor

Good

Best

Figure 2. Decoupling Capacitor Layouts

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PCB Design and Layout Considerations

2.3 Decoupling Capacitor Placement

To minimize ground noise in the system, Adesto recommends placing one or more decoupling capacitors as close as possible to the VCC and GND pins of the device. In some cases a single 1 μF capacitor can be used. For additional decoupling, a second smaller capacitor can be added in parallel. If there are multiple VCC and GND pins, a capacitor should be placed between each VCC/GND pair. Alternatively, a single capacitor or pair of capacitors can be used to connect to multiple VCC/GND pairs. Some examples are shown in Figure 3.
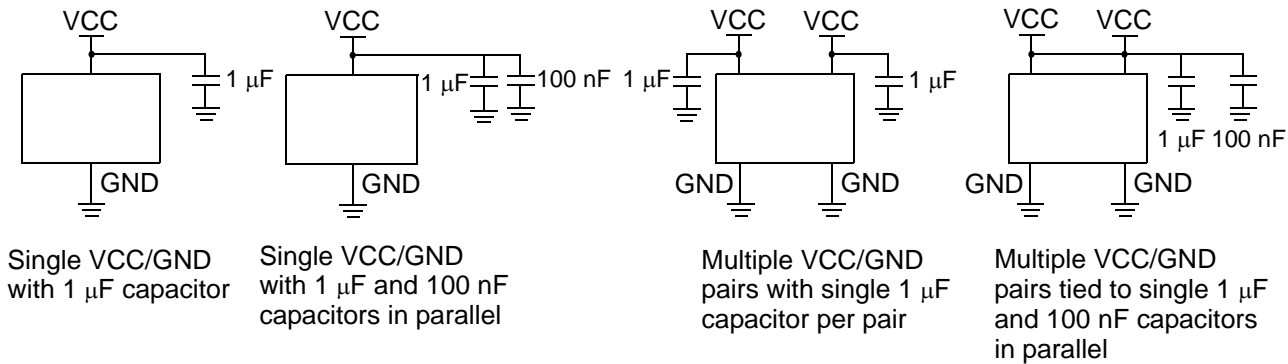
.

Single VCC/GND with 1 μF capacitor

Single VCC/GND with 1 μF and 100 nF capacitors in parallel

Multiple VCC/GND pairs with single 1 μF capacitor per pair

Multiple VCC/GND pairs tied to single 1 μF and 100 nF capacitors in parallel

Figure 3. Inserting a Decoupling Capacitor Between VCC and GND

The following sections describe the component placement and signal routing considerations for each of the package types described in Section 2, Overview of Capacitive Decoupling.

2.4 Decoupling Capacitor Selection

Adesto recommends using ceramic, low ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance) decoupling capacitors as shown in Figure 4.

Ideal Capacitor (No ESR or ESL)
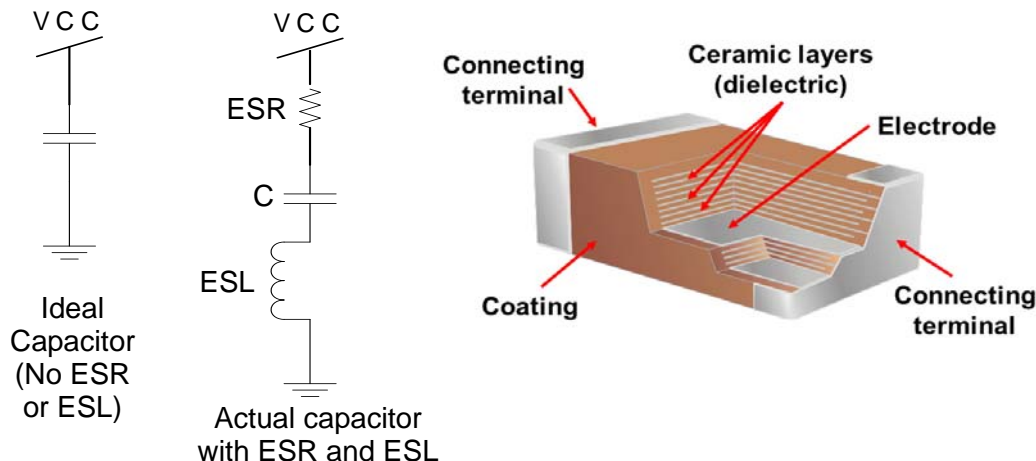
Actual capacitor with ESR and ESL

Figure 4. Cut-Out View of Ceramic Decoupling Capacitor

The designer must also consider the physical size, maximum voltage and temperature range of the capacitor, appropriate for the conditions the system is specified for.

2.5 Capacitor De-rating and Coding

When selecting a decoupling capacitor, note that the amount of capacitance gradually decreases at higher voltages and higher temperatures (capacitor de-rating). This is less of an issue with multi-layer ceramic capacitors, but something to keep in mind when designing for manufacturing.

Table 1 shows an example of how the temperature range (minimum and maximum) and capacitance tolerance are coded for a decoupling capacitor. The most commonly used types are X5R and X7R.

Table 1. Examples of Decoupling Capacitor Coding

Letter Code (Low Temperature)	Number Code (Upper Temperature)	Letter Code (Change of capacitance over the temperature range)
X = -55 ^{o}C (-67 ^{o}F)	4 = +65 ^{o}C (+149 ^{o}F)	P = ±10%
Y = -30 ^{o}C (-22 ^{o}F)	5 = +85 ^{o}C (+185 ^{o}F)	R = ±15%
Z = +10 ^{o}C (+50 ^{o}F)	6 = +105 ^{o}C (+221 ^{o}F)	S = ±22%
	7 = +125 ^{o}C (+257 ^{o}F)	T = ±22/-33%
	8 = +150 ^{o}C (+302 ^{o}F)	U = ±22/-56%
	9 = +200 ^{o}C (+392 ^{o}F)	V = ±22/-82%

2.6 Document Conventions

Throughout this document the following conventions are used:

- Single digit reference designator (C1, C2, C3, etc.) is used for larger value capacitors, e.g. 1 µF, 4.7 µF, or other (depending on the device requirements).

- When capacitors are connected in parallel, the 2-digit reference designator (C11, C12, C13, etc.) represents the smaller value capacitor e.g. 100 nF or other (depending on the device requirements).

3. SIGNAL ROUTING DESIGN CONSIDERATIONS

This section provides signal routing guidelines to use when designing with Adesto memory devices.

Adesto memory device signals can be divided into three categories:

- High-speed data signals: SI, SO, I/O[7:0], SCK, DQS

- Low-speed control signals: $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$/$\overline{RESET}$

- Power supply pins (VCC, GND)

Sections 3.1 through 3.3 address the design considerations for the high and low speed data and control signals. Section 4 addresses the VCC and GND routing for various Adesto package types.

3.1 Data Pin Usage

Adesto memory devices support up to eight data pins depending on the mode of operation. These pins include SI, SO, $\overline{WP}$, and $\overline{HOLD}$/$\overline{RESET}$. Which pins are used to transfer data depends on the operating mode as follows:

Table 2. Operating Mode and Pin Configurations During a Data Transfer

Pin	Operating Mode			
	Single	Dual	Quad	Octal
SI (I/O$_0$)	input	input/output	input/output	input/output
SO (I/O$_1$)	output	input/output	input/output	input/output
$\overline{WP}$ (I/O$_2$)	n/a[1]	n/a[1]	input/output	input/output
$\overline{HOLD}$ (I/O$_3$)	n/a[1]	n/a[1]	input/output	input/output
I/O$_4$				input/output
I/O$_5$				input/output
I/O$_6$				input/output
I/O$_7$				input/output

1. Used as a control pin only. Not used to transfer data.

3.2 High Speed Data Signal Routing Guidelines

Routing of these signals should adhere to the following layout guidelines.

- Device placement. Make sure the device is placed as close as possible to the MCU. This ensures that trace lengths are as short as possible. This by itself will take care of many potential pitfalls in device routing.

- If it is not possible to place the device close to the MCU, make sure the high-speed signals traces are as short as possible.

- Ideally all high-speed (possibly all signals) should be referenced to an adjacent solid ground plane, with no gaps in the ground plane. This ensures good current return paths, minimizing the possibility of signal cross-talk, noise sensitivity due to increased ground loops and the possibility of electromagnetic interference (EMI) and electromagnetic radiation.

- Above 100 MHz and when using DDR/DTR (Double Data Rate / Double Transfer Rate), the length of all high-speed signals should be length-matched.

  Note that signal propagation in a microstrip is slower than in a stripline. Therefore, if two high-speed signals of about equal overall length, one routed mostly in a microstrip, and the other mostly in a stripline; will result in different propagation delays, resulting in different "electrical lengths" of the signals. This may affect signal timing, which may lead to timing violations resulting in incorrect device operation.

- All high-speed signals should be routed on the same layer whenever possible.
  - If layer switching is necessary, try to maintain identical trace lengths on each layer. This ensures that the electrical lengths of the high-speed signals about the same.
  - The number of vias on the high-speed signals should be kept to a minimum and avoided whenever possible, to minimize the effects of the parasitic inductance of the vias.

- Do NOT route signals under crystals, oscillators, clock synthesizers, magnetics, and other high-speed or high-power devices.

- In a multi-ground layer PCB, if a particular signal (referenced to one of the ground planes) must transition to another layer (referenced to another ground plane in the PCB), then the two ground planes must be "stitched" together using a stitching via. The via must be less than 2 inches away from the via where the signal transitions layers.

- In system configurations where one or more devices are connected in parallel and only one of the devices is populated (to provide option of selecting one of multiple devices), minimize stub lengths on the high-speed signals wherever possible.

3.3 Low Speed Control Signal Routing Guidelines

This section describes the routing guidelines for the low-speed $\overline{CS}$, $\overline{WP}$, and $\overline{HOLD}/\overline{RESET}$ control signals.

3.3.1 Aggressor and Victim Signals

Due to cross-coupling, "aggressor" signals such as the high-speed data signals can induce voltages into the "victim" low-speed control signals. This may introduce noise and glitches causing unreliable device operation.

Considering that the slow control signals are often routed on the outer layers of the PCB, they can act as an antenna to any high-frequency signals. The noise injected into the victim signals is radiated out, resulting in radiated emissions that may cause the system to fail EMI compliance.

To mitigate the occurrence of such effects, Adesto recommends to avoid routing victim signals closer than 3 - 4 trace widths to other high-speed and/or high-power signals ("aggressors") such as: clocks, data-lines switching a high data rates (tens of MHz or higher), switched mode power supply signals carrying large currents and switching at tens of kHz or higher.

In addition, if it is necessary to route these signals in close proximity to the above signals, please minimize the length of paralleling this signals as much as possible or just cross them at 90 degree angle.

3.3.2 Routing of Pullup Resistors

Certain control signals on the Adesto devices may require a usage of pull-up resistors for correct operation. This section describes the routing of these pull-up resistors. Typically, pull-up resistors are used for low-speed control signals. However, when the pin has dual functionality, for instance when acting as a slow-speed

PCB Design and Layout Considerations

control signal in one mode of operation, with the option to be configured as a high-speed data signal in another mode, it is important to treat those signals as high-speed signals.

Some examples of dual-use pins include:

- $\overline{WP}$ (I/O$_2$): The $\overline{WP}$ low-speed signal also functions as the I/O$_2$ high speed data signal in Quad / QPI mode

- $\overline{HOLD}$ (I/O$_3$): The $\overline{HOLD}$ low-speed signal also functions as the I/O$_3$ high speed data signal in Quad / QPI mode

Typically these signals have internal pull-ups, but for certain devices the datasheet may recommend also using external pull-ups on these signals.

When an external pull-up resistor is recommended, one pad of the pull-up resistor should be placed close to the signal trace. The other pad of the pull-up resistor is connected to VCC with shortest possible trace as shown in Figure 5.
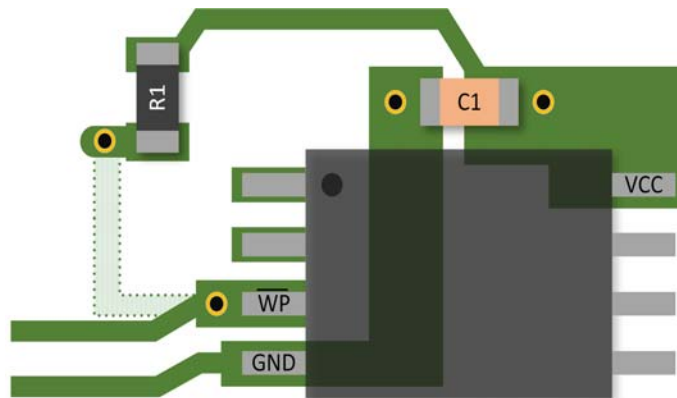

Figure 5. Example of Pull-up Resistor Routing

4. DECOUPLING CAPACITOR ROUTING PER PACKAGE TYPE

The following subsections describe the decoupling capacitor routing options based on package type.

4.1 Standard SOIC Package — Pinout A

This section describes the decoupling capacitor(s) used for routing VCC/GND signals and data signal considerations when designing with the Adesto Standard SOIC package type where the VCC and GND pins are on opposite sides of the device. The Small Outline Integrated Circuit (SOIC) package contains eight pins organized as shown in Figure 6. Pins 1 - 4 reside on the left side of the package, and pins 5 - 8 reside on the right side of the package. On this package, pin 4 is GND and pin 8 is VCC.

4.1.1 Decoupling Capacitor Placement — 2-Layer or Multi-Layer Board with Top Layer Mount

In a 2-layer board layout, where the VCC and GND planes are exposed on the top and bottom layers, effort should be made to place the decoupling capacitor as close to VCC and GND as possible. This may require the use of vias as shown in Figure 6. This option can be used for not only a 2-layer board, but also for a multi-layer board where the capacitor is placed on the top layer. Both single and parallel capacitor options are shown. In this figure, C1 = 1 μF and C10 = 100 nF.
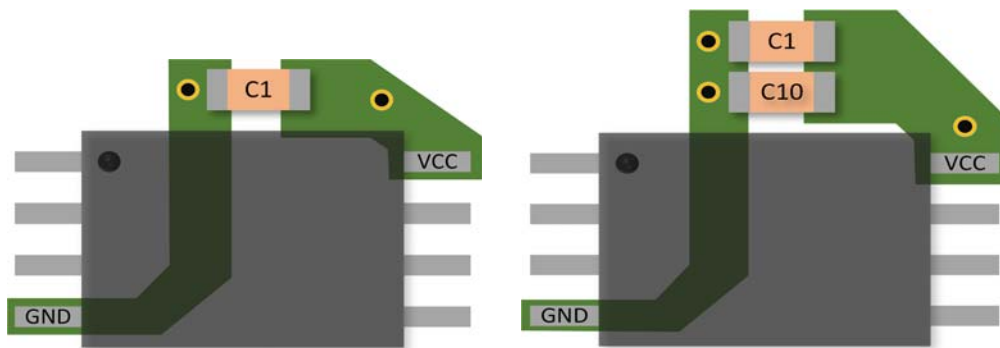

Figure 6. Routing Decoupling Capacitors Between VCC and GND — T op Layer

4.1.2 Placement of Decoupling Capacitor — Multi-Layer Board Bottom Mount

In a board with 4 or more layers, the VCC and GND planes are embedded on the inner layers of the board. In this case the decoupling capacitors can be placed either very close to the package on the top side of the PCB or directly under the package on the bottom side of the PCB. This requires the use of vias as shown in Figure 7.

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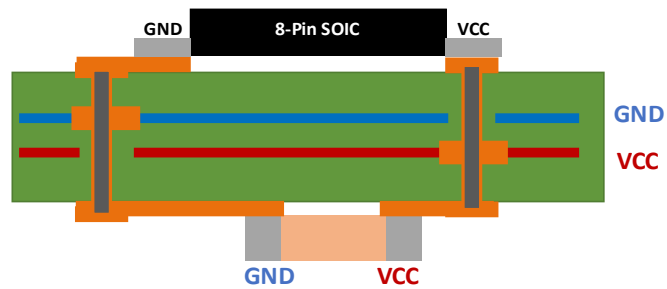# PCB Design and Layout Considerations

Figure 7. Routing Decoupling Capacitors Between VCC and GND Planes on a Multi-Layer Board

4.1.3 Standard Flash SOIC Package Signal Routing Considerations

The Adesto Flash memory signal routing rules are the same for all packages as described in *Section 3, Signal Routing Design Considerations.*

4.2 Standard SOIC Package — Pinout B

This section describes the decoupling capacitor(s) used for routing VCC/GND signals and data signal considerations when designing with the Adesto Standard SOIC package type where the VCC and GND pins are located adjacent to one another on the device. The Small Outline Integrated Circuit (SOIC) package contains eight pins organized as shown in Figure 8. Pins 1 - 4 reside on the left side of the package, and pins 5 - 8 reside on the right side of the package.

4.2.1 Placement of Decoupling Capacitors — 2-Layer Board

Unlike the Standard SOIC package described in the previous section, on this package, pin 6 is GND and pin 7 is VCC. This makes routing of the decoupling capacitor simple and easy. No vias are required, and the capacitors are placed on the top layer of the board right next to the VCC and GND pins, regardless of the number of board layers. The capacitor values are the same as shown in Figure 8. In this figure, C1 = 1 μF.

Figure 8. Placement of Decoupling Capacitor on an Adesto SOIC Device with Adjacent VCC/GND Pins

4.2.2 Placement of Decoupling Capacitors — Multi-Layer Board

As shown in Figure 8, the VCC and GND pins are specifically positioned next to one another on the device. As such, the decoupling capacitor should be placed as close as possible to the VCC and GND pins on the top layer of the board. For this package, mounting the capacitor on the bottom of the board using vias to connect to the VCC and GND planes is not recommended. Adesto recommends connecting directly to the pins on the top signal layer.

4.2.3 SOIC Package Signal Routing Considerations

The Adesto Flash memory signal routing rules are the same for all packages as described in *Section 3, Signal Routing Design Considerations.*

4.3 Standard Flash UDFN Package

This section describes the decoupling capacitor placement on the VCC and GND pins when designing with the Adesto Standard Flash UDFN package type. This package pinout is identical to the Standard Flash SOIC package described above. The difference is that with the UDFN parts, the pins are under the device. Routing of decoupling capacitors is similar to the Standard Flash SOIC package.

4.3.1 Placement of Decoupling Capacitors — 2-Layer Board

In a 2-layer board layout, where the VCC and GND planes are exposed on the top and bottom layers, effort should be made to place the decoupling capacitor as close to the VCC and GND pins as possible. This may require the use of vias as shown in Figure 9. This layout can also be used for a multi-layer board when the capacitor is located on the top layer. In this figure, C1 = 1 μF.
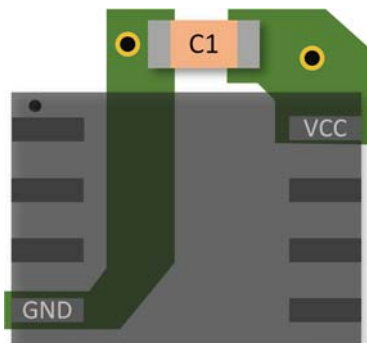
Figure 9.   Placement of Decoupling Capacitor on a UDFN Package — 2-Layer Board

4.3.2 Placement of Decoupling Capacitors — Multi-Layer Board

In a board with 4 or more layers, the VCC and GND planes are embedded on the inner layers of the board. In this case the decoupling capacitors can be placed either very close to the package on the top side of the PCB or directly under the package on the bottom side of the PCB. This requires the use of vias as shown in Figure 10.
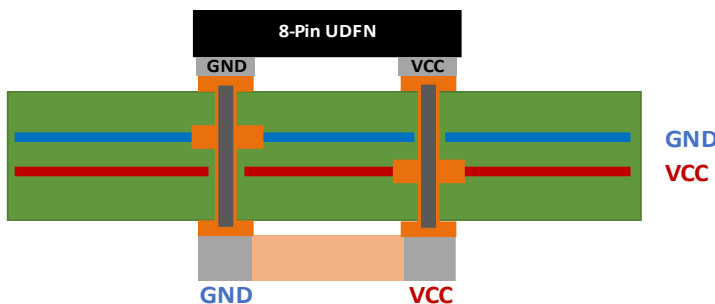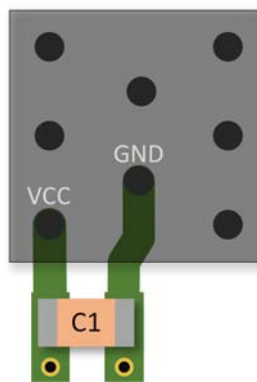

Figure 10. Placement of Decoupling Capacitors on a UDFN Package — Multi-Layer Board Bottom Mount

4.3.3 Standard Flash UDFN Package Signal Routing Considerations

The Standard Flash UDFN package signal routing rules are the same as those for the Standard Flash SOIC device as described above. Refer to the section entitled *Section 3, Signal Routing Design Considerations.*

4.4 WLCSP Package

This section describes the decoupling capacitors used for routing power/ground signals and data signal considerations when designing with the WLCSP package type. This package pinout is comprised of eight balls organized in a vertical 3-2-3 grid as shown in Figure 11.

4.4.1 Placement of Decoupling Capacitor — 2-Layer Board

In a 2-layer board layout, where the VCC and GND planes are exposed on the top and bottom layers, effort should be made to place the two decoupling capacitors as close together as possible to the package on the top layer of the PCB, or directly under the package on the opposite side of the board. This requires the use of vias as shown in Figure 11. This layout can also be used in multi-layer boards where the capacitor is located on the top layer. In this figure, C1 = 1 μF.

Figure 11. Placement of Decoupling Capacitor on a WLCSP Package — 2-Layer Board

4.4.2 Placement of Decoupling Capacitor — Multi-Layer Board

In a board with 4 or more layers, the VCC and GND planes are embedded on the inner layers of the board. In this case it may not be feasible to place the decoupling capacitor between the actual GND and VCC pins of the Adesto device as the power and ground planes are on the inner layers.

However, effort should be made to place the decoupling capacitor as close together as possible to the VCC and GND pins on the top layer of the PCB (as depicted in Figure 11), or directly under the package on the opposite side of the board. This requires the use of vias as shown in Figure 12.
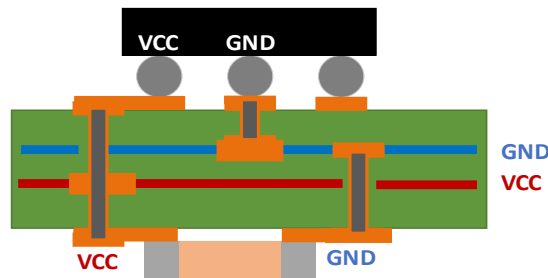

Figure 12. Bottom Mount of Decoupling Capacitors on a WLCSP Package — Multi-Layer Board

4.4.3 WLSCP Package Signal Routing Considerations

The Adesto WLSCP package signal routing rules are the same as those for the Standard SOIC Flash device as described above. Refer to the section entitled *Section 3, Signal Routing Design Considerations.*

PCB Design and Layout Considerations

4.5 BGA Package

This section describes the decoupling capacitor placement used for routing power/ground signals and data signal considerations when designing with the BGA package type.

This package pinout is comprised of 24 balls organized in a 5x4+4 grid as shown in Figure 13.

4.5.1 Bottom Mount of Decoupling Capacitors — 2-Layer Board

The 24-pin BGA package contains 3 sets of VCC/GND pins. In PCB designs where the components are placed on top layer only, there are several options to dealing with the placement and routing of the decoupling capacitors:

- When mounting the capacitors on the top signal layer, place a 1 µF capacitor, or a parallel combination of a 1 µF and 100 nF capacitors on each VCC pin, as depicted in Figure 13. In this figure, C1, C2, and C3 = 1 µF. C11, C12, and C13 = 100 nF.

- When mounting the capacitors on the bottom signal layer, tie all VCC signals together and connect them to a single 4.7 µF capacitor, or a parallel combination of a 4.7 µF and a 100 nF capacitors. This option is shown Figure 15.

In all cases make sure that the decoupling capacitor(s) are placed as close as possible to the VCC and GND pins of the device.
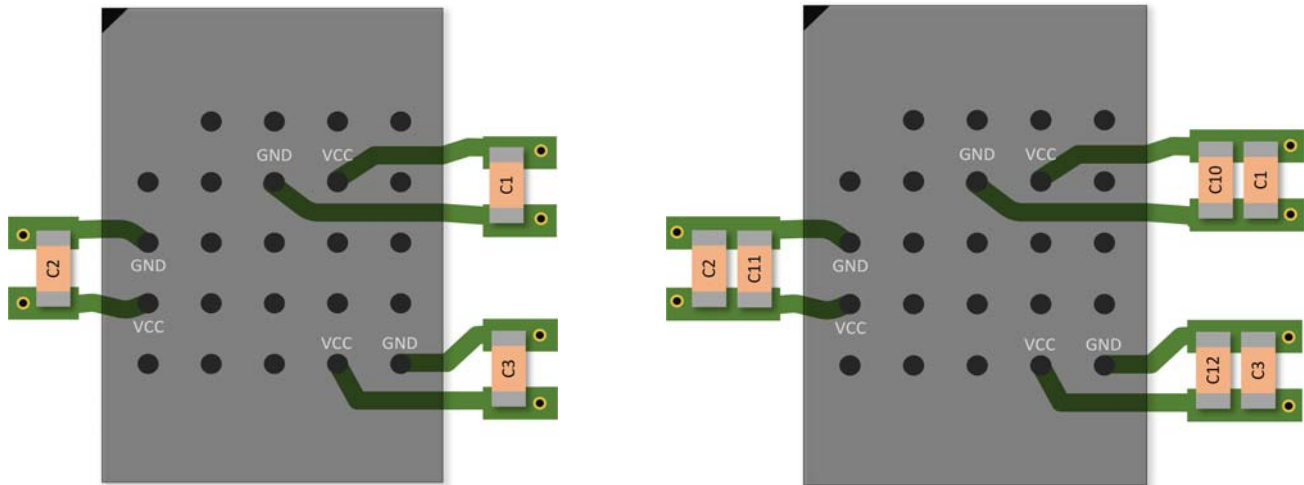

Figure 13. Placement of Decoupling Capacitors on a BGA Package — 2-Layer Board

4.5.2 Placement of Decoupling Capacitor — Top and Bottom Layer Mount

In PCB designs where the components are placed on TOP and BOTTOM layers and where the VCC and GND planes are embedded on the inner layers of the board, the best options are:

- Tie with a via all VCC pins to the power trace or layer underneath the chip
- Tie with a via all GND pins to the solid ground layer underneath the chip
- Connect the terminals of the decoupling capacitor(s) (placed directly underneath the chip, on the bottom layer of the PCB), to the VCC and GND layers of the PCB using short traces, as depicted in Figure 14.

In a board with 4 or more layers, the VCC and GND planes are embedded on the inner layers of the board. In this case, place the decoupling capacitors directly under the package on the bottom side of the PCB. This requires the use of vias as shown in Figure 14. This drawing shows the placement of one of the three VCC/GND pairs on the BGA package.
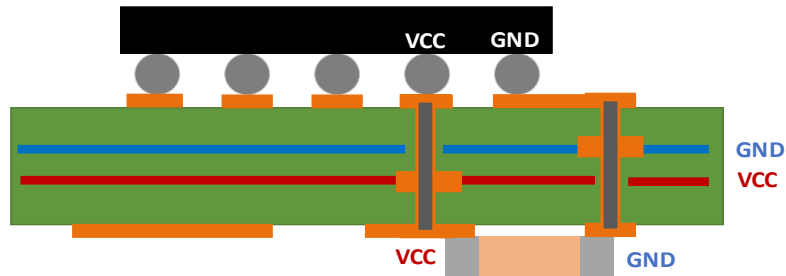

Figure 14. Placement of Decoupling Capacitors on a BGA Package — Multi-Layer Board

4.5.3 BGA Package Signal Routing Considerations

The Adesto WLSCP package signal routing rules are the same as those for the Standard SOIC Flash device as described above. Refer to the section entitled *Section 3, Signal Routing Design Considerations*

4.5.4 Alternative BGA Package Bottom Mount Capacitor Placement

An alternative to placing a capacitor for each VCC and GND pair is to share two decoupling capacitors connected in parallel between all VCC and GND pins. The capacitors are placed on the bottom layer of the PCB and connect to the pins using vias. This is the solution Adesto recommends for use with the EcoXiP devices.In this figure, C1 = 4.7 μF and C10 = 100 nF.
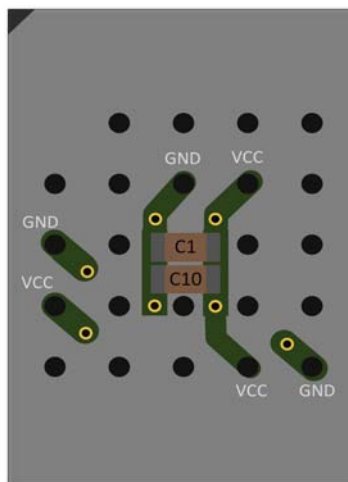

Figure 15. Bottom Mount Capacitor Placement for 24-Pin BGA Package

5. SPECIAL CASES

This section discusses some special layout considerations, such as:

• Two memory devices in parallel

• Reset signal layout considerations

• Test point layout

5.1 Two Flash Devices in Parallel

In a system where two memory devices are placed in parallel and one of the devices is not populated, a stub is created that can cause signal reflections and reduce signal integrity. To mitigate the stub effect, a 0Ω resistor can be placed at close as possible to the intersection where the signals for the unpopulated device branch off of the main signal path. The would be one resistor per memory device signal. This concept is shown in Figure 16.
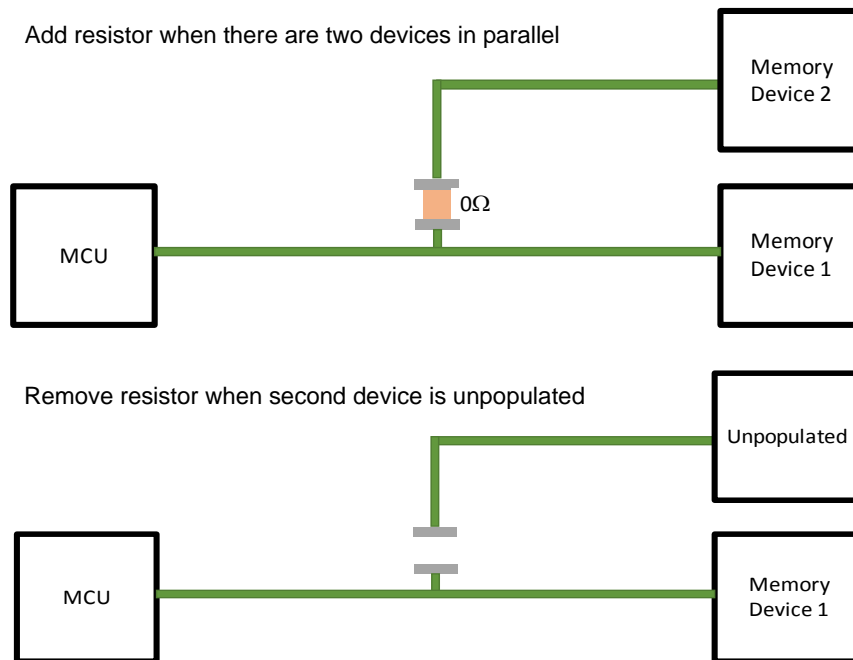
Figure 16. Using Resistors to Maintain Signal Integrity

5.2 Reset Signal Considerations

It may be necessary to be able to reset the memory device during debug. In this case, a 0Ω resistor can be placed in-line with the RESET/HOLD signal. Once the debug function is completed, the resistor can be removed if the pin will not be used during normal operation. This concept is shown in Figure 17.
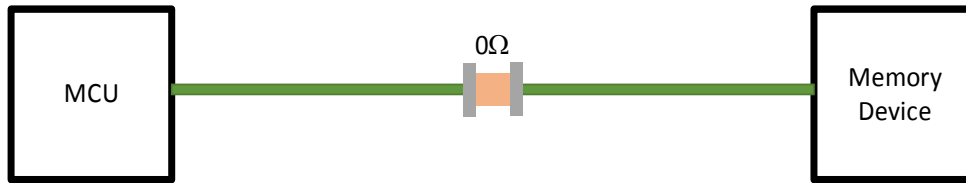
Figure 17. In-line 0 Ohm Resistor Used During Manufacturing Test and Debug

5.3 Test Points

For manufacturing test or debug purposes, it may be useful to place test points on selected memory device signals. In this case, place the test point as close as possible to the signal under observation. This concept is shown in Figure 18. Placing the test point farther away from the signal line can create a 'stub' effect and cause signal reflections.
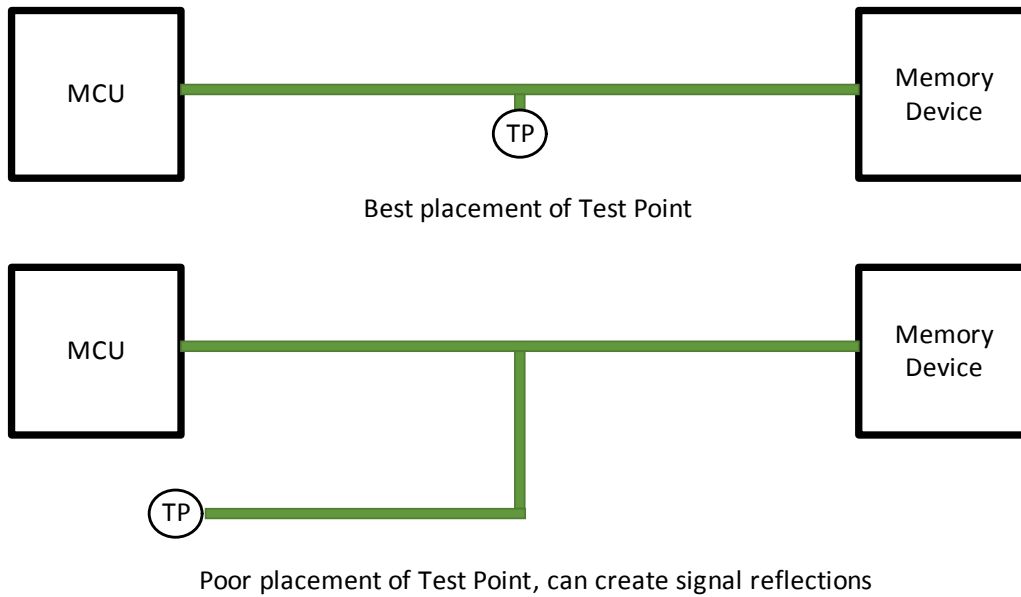

Best placement of Test Point

Poor placement of Test Point, can create signal reflections

Figure 18. Placement of Test Point Along a Signal Path

PCB Design and Layout Considerations

APPENDIX A. ADESTO PACKAGE TYPES

Adesto memory products come in the following basic package types. Note that not all package of each type are shown. But the information in this document pertains to any Adesto package.
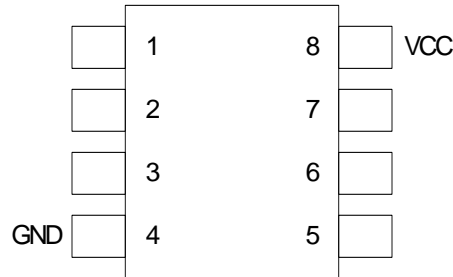
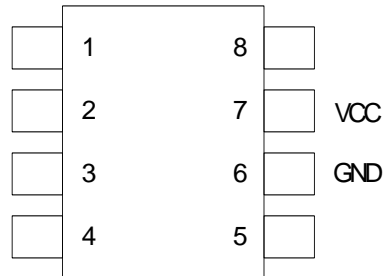**Figure 19. Standard Flash — SOIC Package, Pinout A**

Figure 20. Standard Flash — SOIC Package, Pinout B
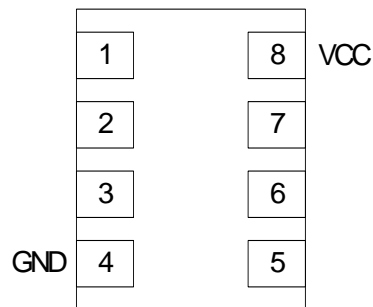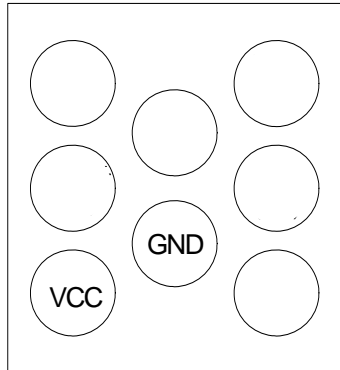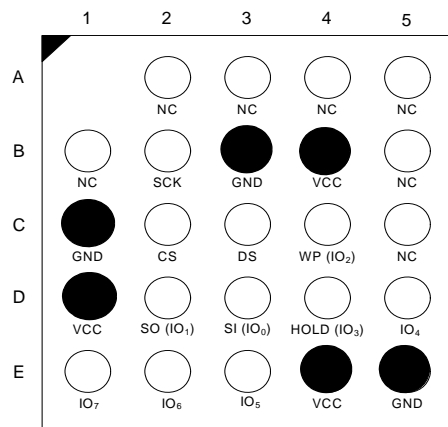
Figure 21. Standard Flash — UDFN Package

Figure 22. Standard Flash — 8-Pin WLCSP Package

Figure 23. Standard Flash — 24-Pin BGA Package

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