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Renesas Electronics Corporation

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H8/300L Super Low Power Series

Addition of Signed 32-Bit Binary Numbers (SADD)

Introduction

The software SADD adds a signed 32-bit binary number to another signed 32-bit binary number and places the result in general-purpose registers.

Target Device

H8/38024

Contents

1. Arguments

Description		Memory area	Data length (bytes)
Input	Augend	R0, R1	4
	Addend	R2, R3	4
Output	Result of addition	R0, R1	4
	Carry	V flag (CCR)	—

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6	R7
○	○	—	—	—	—	×	—

I	U	H	U	N	Z	V	C
—	×	×	×	×	×	○	×

Legend
—: No change
×: Undefined
○: Result

3. Specifications

Program memory (bytes)
20
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
44
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Description

4.1 Details of functions

1. The following arguments are used with the software SADD:
   a. Input arguments
      R0, R1: Sets a signed 32-bit binary augend.
      R2, R3: Sets a signed 32-bit binary addend.
   b. Output arguments
      R0, R1: The result of addition (a signed 32-bit binary number) is placed here.
      V flag (CCR): Indicates whether there is or isn't a carry as a result of addition.
         V flag = 1: A carry has been produced.
         V flag = 0: No carry has been produced.
2. The following figure illustrates the execution of the software SADD. When the input arguments are set as shown in (1), the result of addition is placed in R0 and R1 as shown in (2).

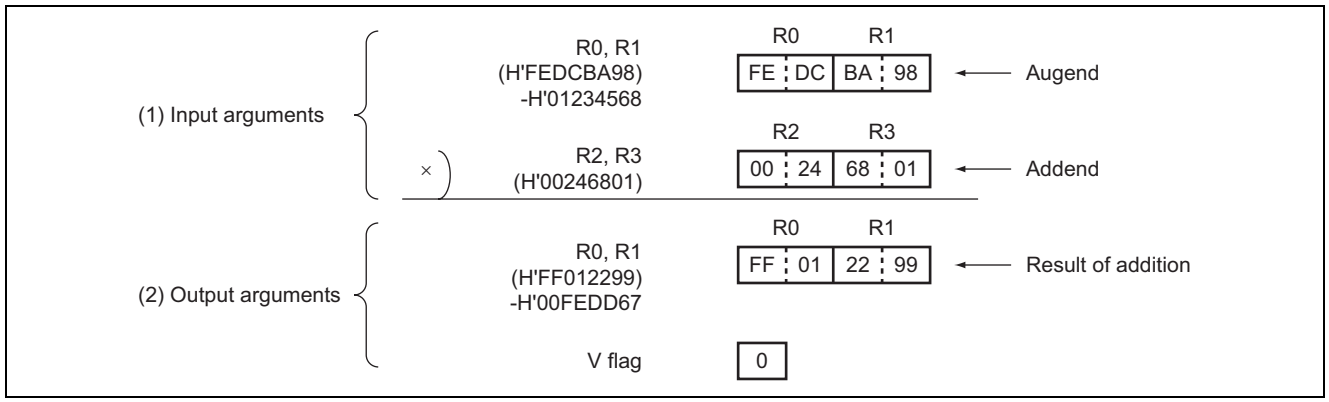


Figure 1 Example of Software SADD Execution

4.2 Notes on usage

After execution of the software SADD, the augend will be lost because the result is placed in R0 and R1. When the augend is still needed after software SADD execution, save it in memory beforehand.

4.3 Data memory

The software SADD uses no data memory.

4.4 Example of usage

Set an augend and an addend in the input arguments and call the software SADD as a subroutine.

```
WORK1     . RES. W      2

WORK2     . RES. W      2        ---------  Reserve a data memory area in which the user program places
                                              a 32-bit binary augend, addend and the result of addition.

WORK3     . RES. W      2

          MOV. W        @WORK1, R0   }-------  Place the 32-bit binary augend set by the user program
          MOV. W        @WORK1+2, R1 }         in the input arguments (R0 and R1).

          MOV. W        @WORK2, R2   }-------  Place the 32-bit binary addend set by the user program
          MOV. W        @WORK2+2, R3 }         in the input arguments (R2 and R3).

          JSR           @SADD        -------  Call the software SADD as a subroutine.

          VBS           OVER

          MOV. W        R0, @WORK3   }-------  Place the result set in the output arguments (R3 and R4)
          MOV. W        R1  @WORK3+2 }         in the data memory area of the user program.
              .
              .
              .
OVER      Carry processing routine

              .
              .
              .
```

4.5 Operation

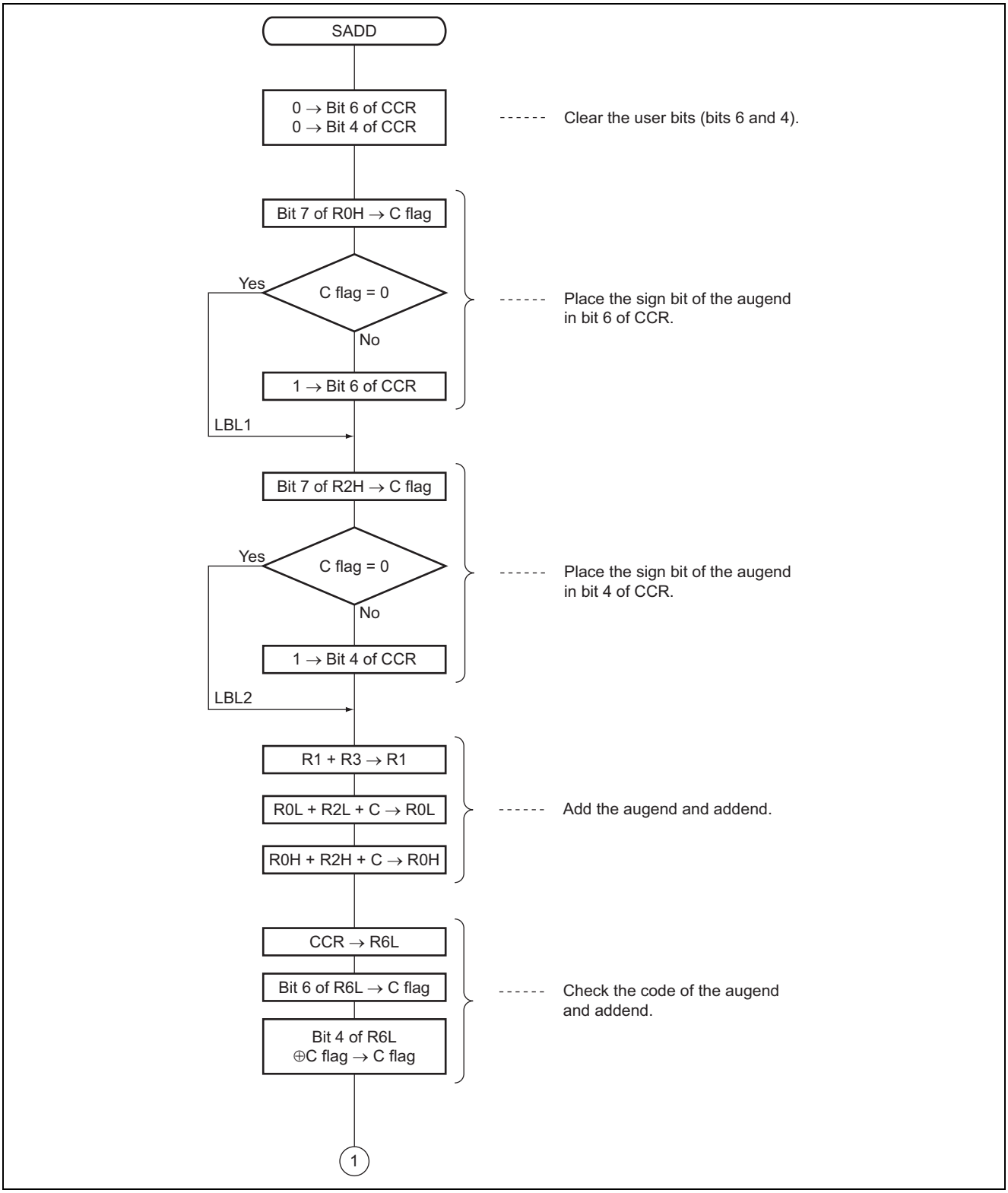
1. Addition of signed 32-bit binary numbers is done by using add instructions (ADD.W and ADDX.B).
2. The addition is performed in the following steps:
   a. An augend is placed in R0 and R1 and an addend in R2 and R3.
   b. The user bits (bits 6 and 4) and the overflow flag (bit 2) of the CCR are cleared.
   c. When the augend is negative, the user bit (bit 6) of the CCR is set to 1 as a sign bit. When the addend is negative, the user bit (bit 4) of the CCR is set to 1 as a sign bit.
   d. The augend is added to the addend as follows:

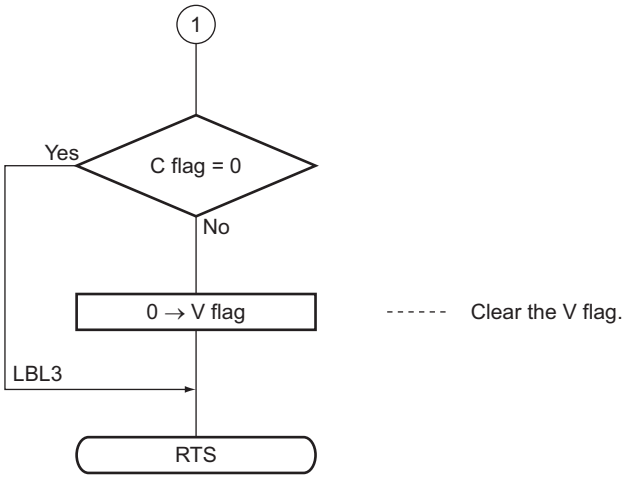
R1 + R3 → R1
R0L + R2L + C → R0L
R0H + R2H + C → R0H
------- equation 1

   e. Finally, the sign bits (CCR user bits) are tested and the V flag is operated as follows:

<Sign bit> Bit 6 of CCR (Augend)	Bit 4 of CCR (Addend)	
0	0	→ Continue processing.
0	1	→ Clear the V flag.
1	0	
1	1	→ Continue processing.

5. Flowchart


SADD
0 → Bit 6 of CCR
0 → Bit 4 of CCR
Clear the user bits (bits 6 and 4).
Bit 7 of R0H → C flag
Yes
C flag = 0
No
1 → Bit 6 of CCR
Place the sign bit of the augend in bit 6 of CCR.
LBL1
Bit 7 of R2H → C flag
Yes
C flag = 0
No
1 → Bit 4 of CCR
Place the sign bit of the augend in bit 4 of CCR.
LBL2
R1 + R3 → R1
R0L + R2L + C → R0L
R0H + R2H + C → R0H
Add the augend and addend.
CCR → R6L
Bit 6 of R6L → C flag
Bit 4 of R6L
⊕C flag → C flag
Check the code of the augend and addend.
1


1
Yes
C flag = 0
No
0 → V flag
------ Clear the V flag.
LBL3
RTS

6. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:15:08
PROGRAM NAME =
 1                              ;*************************************************************
 2                              ;*
 3                              ;*      00 - NAME     :SIGNED 32 BIT BINARY ADDITION (SADD)
 4                              ;*
 5                              ;*************************************************************
 6                              ;*
 7                              ;*      ENTRY         :R0 (UPPER WORD OF SUMMAND)
 8                              ;*                     R1 (LOWER WORD OF SUMMAND)
 9                              ;*                     R2 (UPPER WORD OF ADDEND)
10                              ;*                     R3 (LOWER WORD OF ADDEND)
11                              ;*
12                              ;*      RETURNS       :R0 (UPPER WORD OF RESULT)
13                              ;*                     R1 (LOWER WORD OF RESULT)
14                              ;*                     V FLAG OF CCR
15                              ;*                     (V=0;TRUE,V=1:OVERFLOW OR UNDERFLOW)
16                              ;*
17                              ;*************************************************************
18                              ;
19  SADD_cod C    0000                      .SECTION              SADD_code,CODE,ALIGN=2
20                                          .EXPORT               SADD
21                              ;
22  SADD_cod C          00000000  SADD      .EQU $                ;Entry point
23  SADD_cod C    0000  06AD                ANDC      #H'AD,CCR   ;Clear user bits and V flag of CCR
24  SADD_cod C    0002  7770                BLD       #7,R0H      ;Load sign bit of summand
25  SADD_cod C    0004  4402                BCC       LBL1        ;Branch if C = 0
26  SADD_cod C    0006  0440                ORC.B     #H'40,CCR   ;Bit set user bit (bit 6 of CCR)
27  SADD_cod C    0008            LBL1
28  SADD_cod C    0008  7772                BLD       #7,R2H      ;Load sign bit of addend
29  SADD_cod C    000A  4402                BCC       LBL2        ;Branch if C = 0
30  SADD_cod C    000C  0410                ORC.B     #H'10,CCR   ;Bit set user bit (bit 4 of CCR)
31  SADD_cod C    000E            LBL2
32  SADD_cod C    000E  0931                ADD.W     R3,R1       ;R3 + R1 -> R1
33  SADD_cod C    0010  0EA8                ADDX.B    R2L,R0L     ;R2L + R0L + C -> R0L
34  SADD_cod C    0012  0E20                ADDX.B    R2H,R0H     ;R2H + R0H + C -> R0H
35  SADD_cod C    0014  020E                STC       CCR,R6L     ;CCR -> R6L
36  SADD_cod C    0016  776E                BLD       #6,R6L      ;Bit load bit 4 of R6L
37  SADD_cod C    0018  754E                BXOR      #4,R6L      ;Bit exclusive OR sign bits
38  SADD_cod C    001A  4402                BCC       LBL3        ;Barnch if C = 0
39  SADD_cod C    001C  06FD                ANDC.B    #H'FD,CCR   ;Clear V flag
40  SADD_cod C    001E            LBL3
41  SADD_cod C    001E  5470                RTS
42                              ;
43                                          .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

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Revision Record

		Description	
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