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SH7080 Group

A/D Conversion in Single-cycle Scan Mode

Introduction

This application note describes the single-cycle scan mode of A/D conversion. It is intended as reference material to help in the design of user software.

Target Device

SH7086

Contents

1. Specification

In this sample application, the A/D converter for the SH7086 performs A/D conversion in single-cycle scan mode.

Three rounds of A/D conversion proceed on analog input channels 0 to 3 (AN0 to AN3). Converted data are stored in the on-chip RAM. An overview of the operation is shown in figure 1.

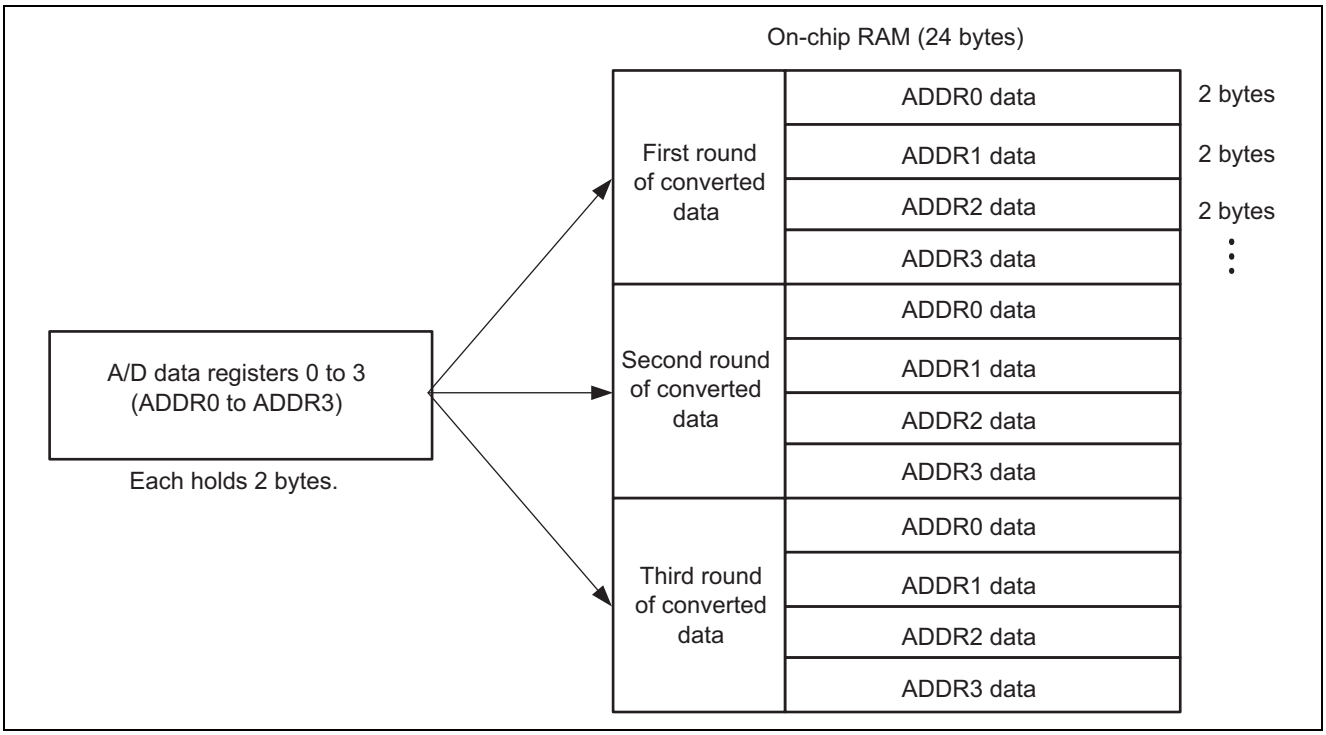


Figure 1 Overview of A/D Conversion

2. Applicable Conditions

The applicable conditions for this sample application are shown in table 1.

Table 1 Applicable Conditions

Item	Setting
Device	SH7086 (R5F70865)
Operating frequency	Internal clock: Iϕ = 80 MHz Bus clock: Bϕ = 40 MHz Peripheral clock: Pϕ = 40 MHz MTU2 clock: MPϕ = 40 MHz MTU2S clock: MIϕ = 80 MHz
Operating mode	Single-chip mode
Development environment	Renesas Technology products: High-performance Embedded Workshop Version 4.03.00.001 (integrated development environment) SuperH RISC engine Standard Toolchain (V.9.1.1.0) SuperH RISC engine C/C++ Compiler (V.9.01.01)
C compiler options	High-performance Embedded Workshop default settings: [-cpu=sh2 -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo]

3. Description of Modules Used

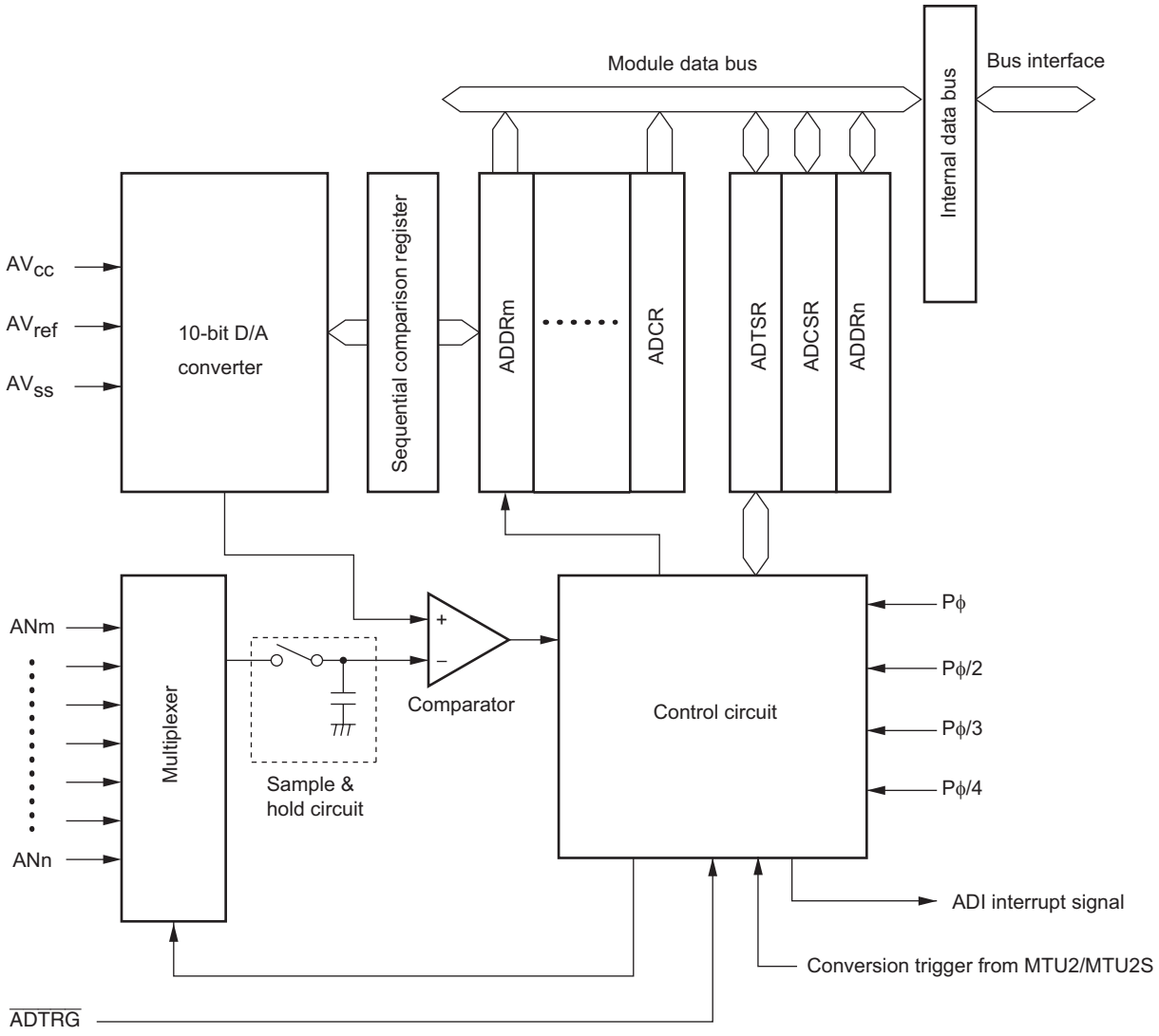
In this sample application, A/D converter channels 0 to 3 are used for A/D conversion.

The functions of the SH7080 group A/D converter are outlined in table 2.

Table 2 A/D Converter Function Overview

Item	Overview
Resolution	10 bits
Input channels	• 8 channels (2 independent A/D conversion modules on chip) for the SH7083/84/85 • 16 channels (3 independent A/D conversion modules on chip) for the SH7086
Conversion time	• 2.0 µs per channel (when Pϕ = 25 MHz)
Operation mode	• Single mode: A/D conversion on one channel • Continuous scan mode: A/D conversion repeated on up to 4 channels for the SH7083/84/85 or up to 8 channels for the SH7086 • 1-cycle scan mode: A/D conversion repeated on up to 4 channels for the SH7083/84/85 or up to 8 channels for the SH7086
Data register	Results of A/D conversion are stored in 16-bit data registers corresponding to the respective input channels.
A/D conversion start method	• Operation of the A/D control register (ADCR) by software • A/D converter start trigger from the multi-function timer pulse unit 2 (MTU2) or 2S (MTU2S) can be selected. • External trigger signal
Interrupt source	• A/D conversion end interrupt request (ADI)
Others	• Sample & hold functions are provided. • Module standby mode can be set. • DMAC/DTC can be started by an interrupt.

A block diagram of the A/D converter is shown in figure 2.



[Legend]

AV_{CC}	: Power supply pin or reference voltage in the analog portion
AV_{ref}	: Reference voltage for A/D conversion
AV_{SS}	: Ground or reference voltage in the analog portion
ANm to ANn	: Analog input pins
ADCR	: A/D control register
ADCSR	: A/D control/status register
ADTSR	: A/D trigger select register
ADDRm/n	: A/D data register m/n

Note: The register number corresponds to the channel number of modules.
(m/n = 0 to 7 for the SH7083/84/85 and 0 to 15 for the SH7086)

Figure 2 A/D Converter Block Diagram (One Module)

- The A/D data registers (ADDRm and ADDRn) are 16-bit read-only registers which hold the results of conversion on the corresponding analog input channels. Converted data are stored in bits 15 to 6 of ADDR. The 6 lower bits are always 0.
- The A/D control register (ADCR) controls the start of A/D conversion.
- The A/D control/status register (ADCSR) controls A/D conversion and sets the A/D conversion time.
- The A/D trigger select register (ADTSR) enables an external trigger to start A/D conversion.

Note: For details on the operational specifications, refer to the section on A/D converter (ADC) in the SH7080 Group Hardware Manual.

4. Principles of Operation

In this sample application, A/D conversion is performed three times in single-cycle scan mode on each of analog input channels 0 to 3 (AN0 to AN3). Converted data are stored in the on-chip RAM on completion of each round of conversion on all channels. Figure 3 is a timing diagram of operations in this sample application.

In single-cycle mode, A/D conversion starts when the ADST bit is set to 1. On completion of conversion for the specified number of channels, the ADST bit is automatically cleared and the ADF bit is automatically set to 1. In this sample application, three rounds of A/D conversion are performed. The ADF bit is cleared on completion of A/D conversion. Then ADST bit is set to1 and the remaining two rounds of A/D conversion are performed.

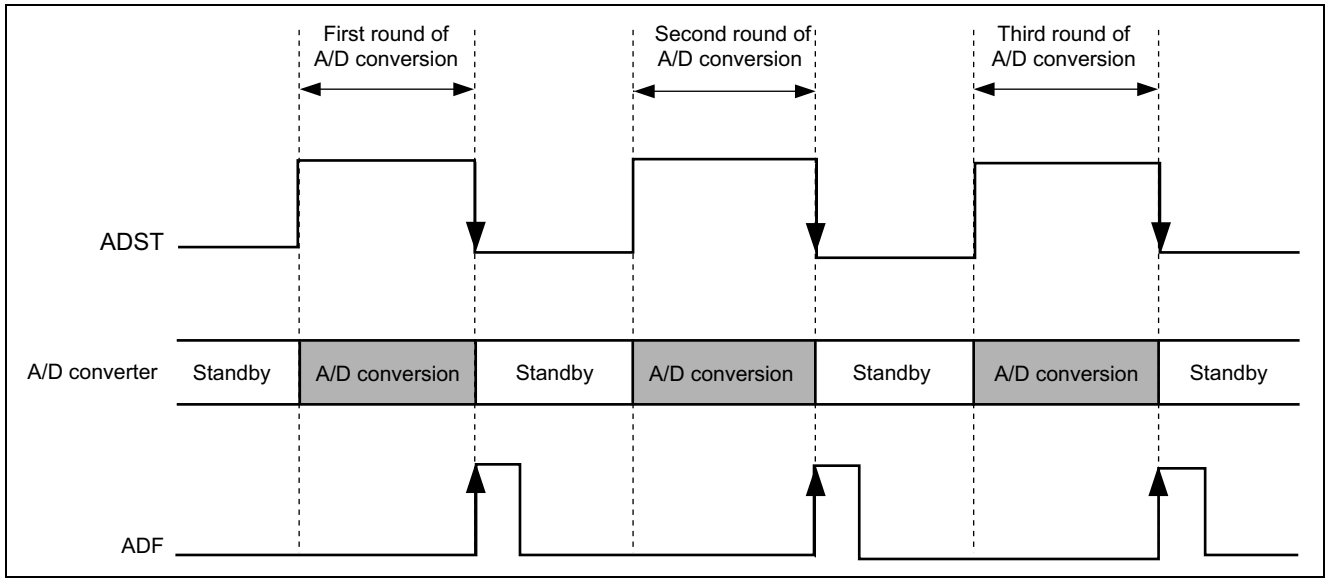


Figure 3 Operational Timing for A/D Conversion

A more detailed view of the timing is given in figure 4. Processing at the numbered points is described in table 3.

Firstly, the mode, channel, clock, etc., are selected with ADCSR_0 and ADCR_0 ((1) in figure 4).

Then, the ADST bit in ADCR_0 is set to 1 to start A/D conversion (figure 4, (2) and (3)). At the end of each round of A/D conversion on all the channels (0 to 3), the converted data are stored in bits 15 to 6 of the corresponding register from ADDR0 to ADDR3 (figure 4, (4)). The ADF bit is set to 1 after conversion on all channels has been completed (figure 4, (5)). Also, the ADST bit is cleared to 0 (figure 4, (6)). In single-cycle scan mode, A/D conversion is performed only once on each specified channel (in this sample application, A/D conversion is performed once on each of the channels AN0 to AN3). After that, the ADF flag of ADCSR_0 is cleared to 0 (figure 4, (7)) and data from all the four registers are stored in the on-chip RAM (figure 4, (8)).

Steps (2) to (8) shown in figure 3 are repeated twice (figure 4, (9) and (10)).

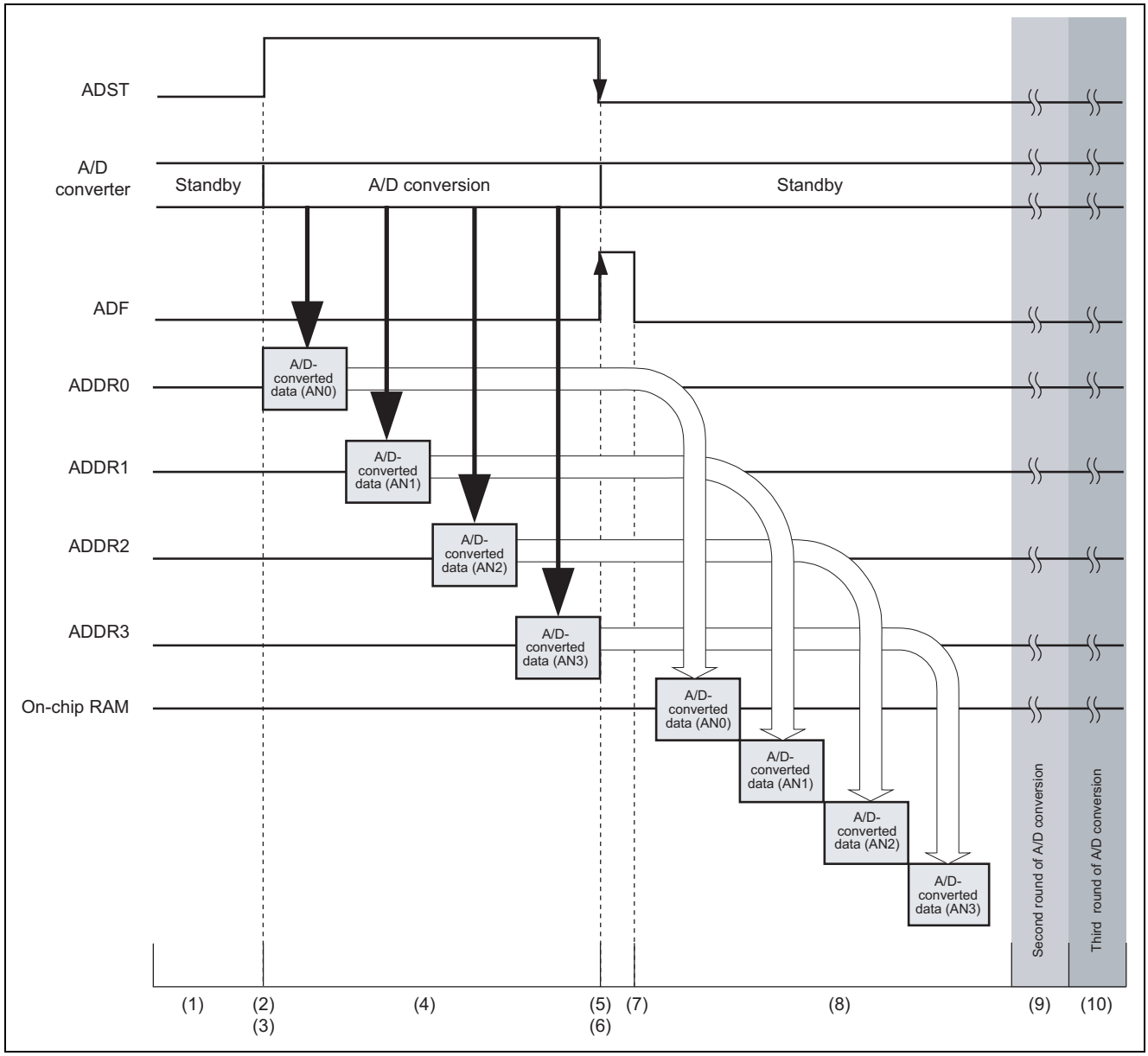


Figure 4 Details on the Timing of A/D Conversion

Table 3 Processing

	Software processing	Hardware processing
(1)	ADCSR_0 and ADCR_0 are used to select the mode, channel, clock, etc.	—
(2)	Setting the ADST bit of ADCR_0 to 1.	Starting A/D conversion on input channel AN0.
(3)	—	Sampling the analog inputs and performing conversion.
(4)	—	After conversion storing converted data in registers from ADDR0 to ADDR3.
(5)	—	Setting the ADF bit of ADCSR_0 to 1.
(6)	—	Clearing the ADST bit to 0.
(7)	Clearing the ADF bit of ADCSR_0 to 0.	—
(8)	Storing data from the registers ADDR0 to ADDR3 in the RAM.	—
(9)	Repeating steps (2) to (8) (to perform A/D conversion a second time).	Repeating steps (2) to (8) (to perform A/D conversion a second time).
(10)	Repeating steps (2) to (8) (to perform A/D conversion a third time).	Repeats steps (2) to (8) (to perform A/D conversion a third time).

5. Description of Software

5.1 List of Functions

The functions of this sample application are listed below.

Table 4 List of Functions

Function Name	Description
main()	Initializes A/D converter module 0 and calls the A/D conversion routine.
ad_conv()	Starts A/D conversion and stores the results of conversion in the on-chip RAM.

5.2 Variables Used

The variables used in this sample application are listed below.

Table 5 List of Variables

Variable/Label Name	Description	Referring function
Unsigned short Ad_data[AD][CH]	Array (2 bytes) for storing A/D-converted data. AD indicates the number of rounds of A/D conversion, i.e. 3 in this sample application. CH indicates the number of channels, i.e. 4 in this sample application.	ad_conv()
Unsigned char ad_count	A/D conversion counter	ad_conv()
Unsigned char ch_count	A/D conversion channel number counter	ad_conv()

5.3 Section Assignment

Section assignment for this sample application is as follows.

Table 6 Section Assignment

Address	Section Name	Description
H'00000000	DVECTTBL, DINTTBL, PIntPRG	DVECTTBL: Exception vector table DINTTBL: Interrupt vector table PIntPRG: Interrupt program
H'00000800	PResetPRG	Reset program
H'00001000	P, C$BSEC, C$DEC, D	P: Program area C$BSEC: Stores an address for B section initialization. C$DEC: Stores an address for D section initialization. D: Stores data.
H'FFFF4000	B, R	B: uninitialized data area R: initialized data
H'FFFFBC00	S	Stack area

5.4 Register Settings

The registers used in this sample application are described below. The settings below are the values used in this sample application and differ from the initial values.

5.4.1 Clock Oscillator (CPG) Settings

(1) **Frequency Control Register (FPQCR)**

Function: Specifies the division ratios for the frequency output by the PLL circuit.

Set value: H'0241

Bit	Bit Name	Set Value	Description
15	—	0	Reserved
14 to 12	IFC[2:0]	000	Frequency division ratio of the internal clock (Iϕ) frequency 000: × 1 (Iϕ = 80 MHz for an input clock frequency of 10 MHz)
11 to 9	BFC[2:0]	001	Frequency division ratio of the bus clock (Bϕ) frequency 001: × 1/2 (Bϕ = 40 MHz for an input clock frequency of 10 MHz)
8 to 6	PFC[2:0]	001	Frequency division ratio of the peripheral clock (Pϕ) frequency 001: × 1/2 (Pϕ = 40 MHz for an input clock frequency of 10 MHz)
5 to 3	MIFC[2:0]	000	Frequency division ratio of the MTU2S clock (MIϕ) frequency 000: × 1 (MIϕ = 80 MHz for an input clock frequency of 10 MHz)
2 to 0	MPFC[2:0]	001	Frequency division ratio of the MTU2 clock (MPϕ) frequency 001: × 1/2 (MPϕ = 40 MHz for an input clock frequency of 10 MHz)

5.4.2 Low Power Mode Settings

(1) **Standby Control Register 4 (STBCR4)**

Function: Controls the operation of individual modules in low-power-consumption mode.

Set value: H'FE

Bit	Bit Name	Set Value	Description
7	MSTP23	1	Module stop bit 23. When set to 1, stops the clock supply to the MTU2S. When set to 0, makes the MTU2S operate.
6	MSTP22	1	Module stop bit 22. When set to 1, stops the clock supply to the MTU2. When set to 0, makes the MTU2 operate.
5	MSTP21	1	Module stop bit 21. When set to 1, stops the clock supply to the CMT. When set to 0, makes the CMT operate.
4, 3	—	All 1	Reserved
2	MSTP18	1	Module stop bit 18. When set to 1, stops the clock supply to the AD_2. When set to 0, makes the AD_2 operate.
1	MSTP17	1	Module stop bit 17. When set to 1, stops the clock supply to the AD_1. When set to 0, makes the AD_1 operate.
0	MSTP16	0	Module stop bit 16. When set to 1, stops the clock supply to the AD_0. When set to 0, makes the AD_0 operate.

5.4.3 A/D Conversion Settings

(1) **A/D Control/Status Register _0 (ADCSR_0)**

Function: Controls A/D conversion and sets A/D conversion time.

Set value: H'0013

Bit	Bit Name	Set Value	Description
15	ADF	0	A/D end flag A status flag which indicates the end of A/D conversion. [Setting conditions] • When A/D conversion on all channels is completed in scan mode. [Clearing conditions] • When 0 is written after reading it as 1. • When DMAC/DTC is activated by an ADI interrupt and ADDR is read.
14	ADIE	0	A/D interrupt (ADI) enable When set to 1, generation of an ADI interrupt by ADF is enabled.
13, 12	—	All 0	Reserved
11	TRGE	0	Trigger enable When TRGE = 0, the A/D conversion trigger is disabled.
10	—	0	Reserved
9	CONADF	0	ADF control Controls ADF operation in 2-channel scan mode.
8	STC	0	State control Sets A/D conversion time (50 states for this sample application).
7, 6	CKSL[1:0]	00	Clock select bits 1 and 0 Set A/D conversion time (Pϕ/4 for this sample application).
5, 4	ADM[1:0]	01	A/D mode bits 1 and 0 Select A/D conversion mode (4-channel scan mode for this sample application).
3	ADCS	0	A/D continuous scan (single-cycle scan mode for this sample application)
2 to 0	CH[2:0]	011	Channel select bits 2 to 0 Select analog input channels for A/D conversion (channels AN0 to AN3 for this sample application).

(2) **A/D Control Register _0 (ADCR_0)**

Function: Controls the start of A/D conversion.

Set value: H'0000

Bit	Bit Name	Set Value	Description
15, 14	—	All 0	Reserved
13	ADST	0	A/D start. When cleared to 0, the A/D conversion is stopped and the A/D converter enter the idle state. When set to 1, A/D conversion is started. Cleared automatically in single mode upon completion of A/D conversion on the selected channel.
12 to 0	—	All 0	Reserved

(3) **A/D Trigger Select Register _0 (ADTSR_0)**

Function: Enables an external trigger for the start of A/D conversion.

Set value: H'0000 (initial value)

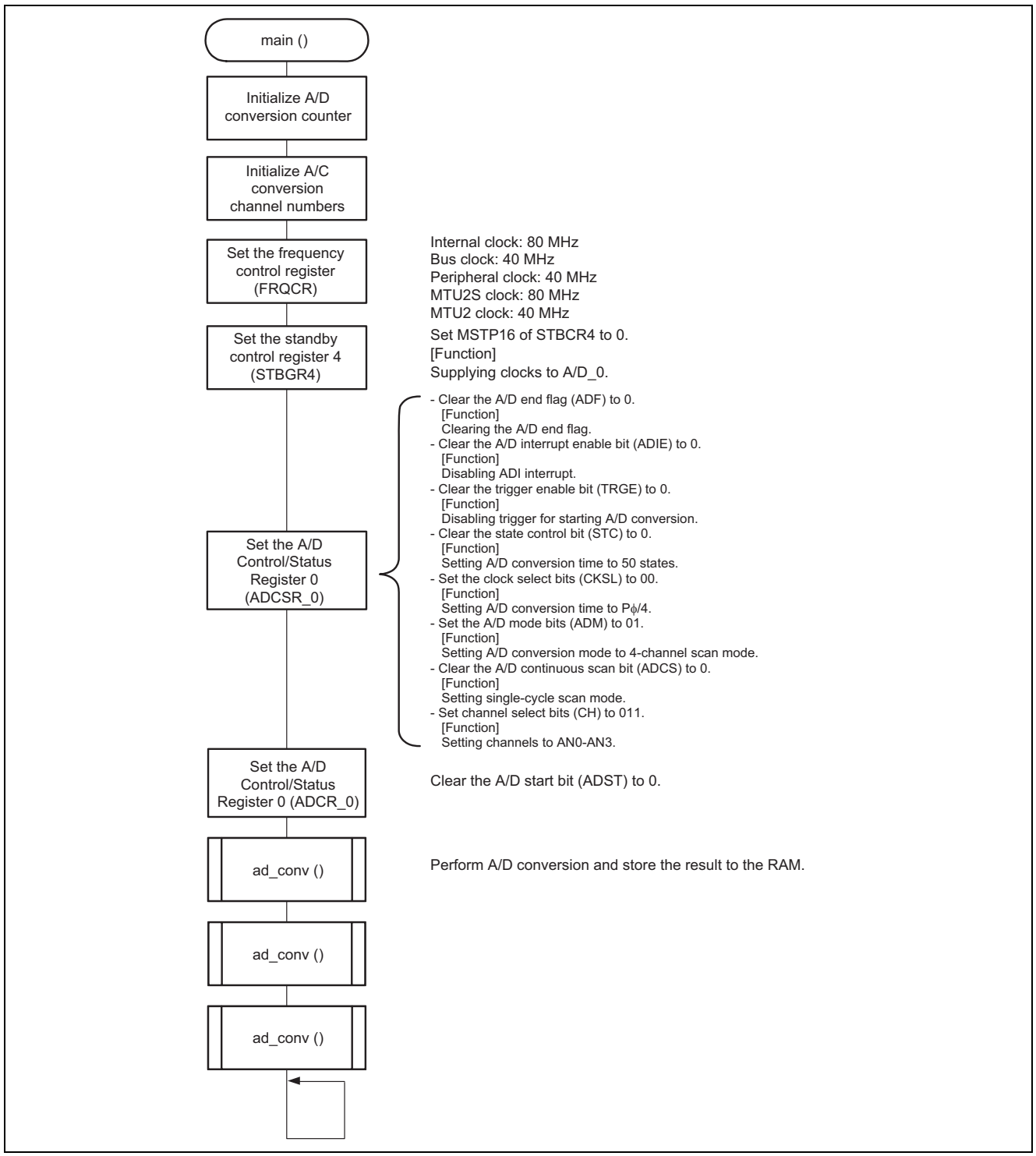
This sample application does not use an external trigger. Thus, this register is not set and its initial values are used as-is.

Bit	Bit Name	Initial Value	Description
15 to 12	TRG11S[3:0]	0000	A/D Trigger 1 Group 1 Select 3 to 0. Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for group 1 when A/D module 1 is in 2-channel scan mode.
11 to 8	TRG01S[3:0]	0000	A/D Trigger 0 Group 1 Select 3 to 0. Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for group 1 when A/D module 0 is in 2-channel scan mode.
7 to 4	TRG1S[3:0]	0000	A/D Trigger 1 Select 3 to 0. Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for A/D module 1.
3 to 0	TRG0S[3:0]	0000	A/D Trigger 0 Select 3 to 0. Select an external trigger, MTU2 trigger or MTU2S trigger to start A/D conversion for A/D module 1.

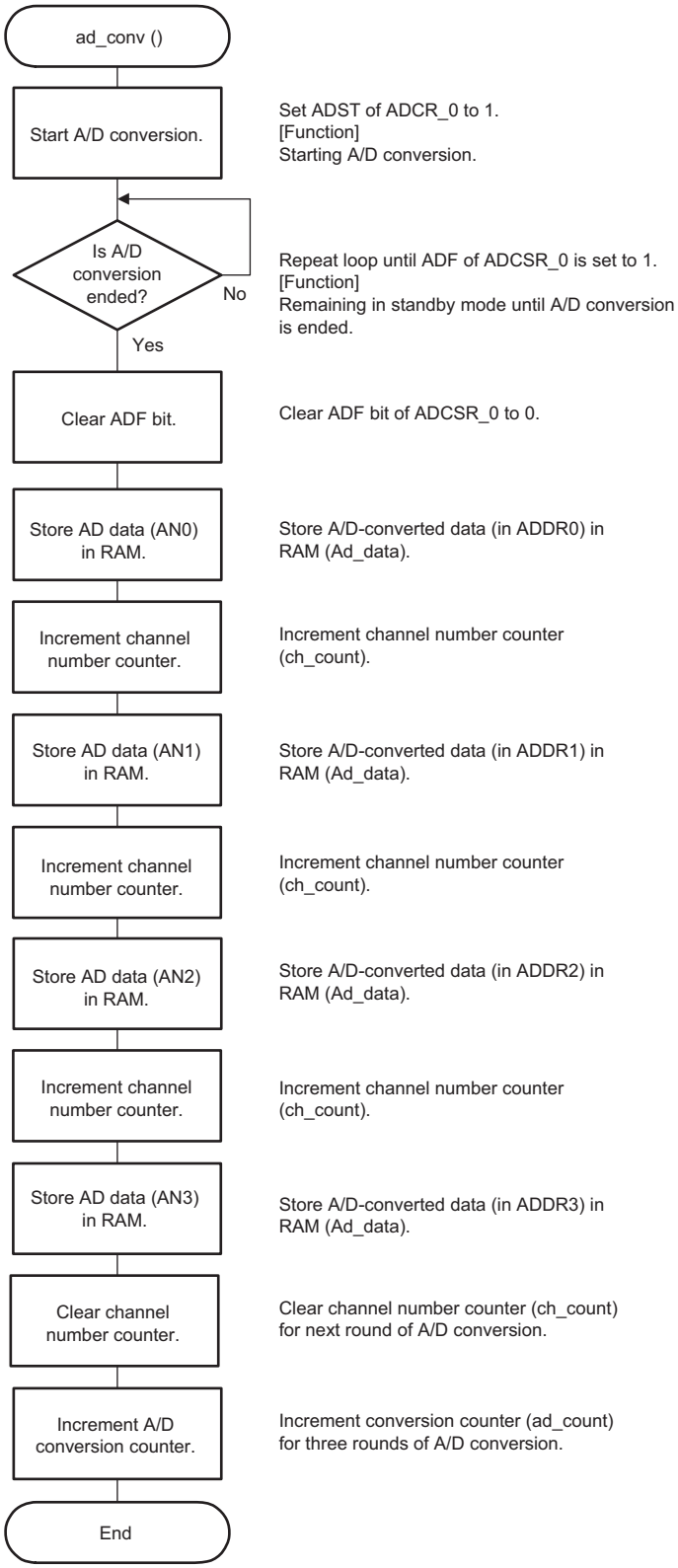
6. Flowchart

A flowchart for this sample application is shown below.

6.1 Main Routine



6.2 A/D Conversion Routine



7. Documents for Reference (Note)

- Software Manual
  SH-1/SH-2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7080 Group Hardware Manual
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