

## 1 Description

The 82P337xx are Synchronous Equipment Timing Source (SETS) for Synchronous Ethernet (SyncE) per ITU-T G.8264. These SETS generates ITU-T G.8262 compliant SyncE clocks, Telcordia GR-1244-CORE/GR-253-CORE, and ITU-T G.813 compliant SONET/SDH clocks.

## 2 Programming Information

### 2.1 Timing Commander

The user is urged to obtain from their local IDT FAE the Timing Commander/Evaluation Board Users Guide, a copy of the IDT Timing Commander software and the appropriate Personality file (.tcp extension) to model the specific SMU. An initial Settings file (.tcs extension), which contains all register values, can be generated by the IDT SMU Applications group and the IDT FAE with user input to define the application.

The Timing Commander Personality (.tcp extension) allows the majority of the register settings of the device to be established without the requirement of consulting the register map directly. It also demonstrates that the devices that contain an APLL3, the 82P33731, respond to two different I2C addresses. The DPLL, APLL1 and APLL2 all respond to I2C eight bit write addresses. The fourth write address is taken by APLL3. The 8-bit I2C address is xxxx[a2][a1][a0]0, where xxxx defaults to 1010 (h'A); [a0] must be '0' to access APLL3 and '1' to access the rest of the chip. A2, A6, AA, AE are the four address for DPLLs, APLL1 & APLL2. For all other devices, there can be 8 I2C addresses.

After the initial tcs file is generated, refinements to the register settings can be made on the evaluation board as the user becomes more familiar with the feature set of the part defined in the memory map. The evaluation board is also a useful debug tool to determine the expected behavior when register settings are changed.

### 2.2 Programming over the Slave Microprocessor Interface

The device supports I2C, SPI and UART modes. An I2C device driver is available and recommended to assist setting up the device.

These devices define the most significant four bits of the I2C base address, I2C\_AD[6:3], as 0b1010. Of the remaining three bits, I2C\_AD[2:0], I2C\_AD[2:1] are defined by strapping pins on the part and are 0b00 by default. For 'x31 devices, I2C\_AD0 = 1 and is defined internal to the part; there is no I2C\_A0 strapping pin provided.

All register accesses are done as 8-bit bus cycles. The memory is structured as eight pages of 128 bytes each (with the exception of APLL3). The ten bit extended address, which locates any register in the memory map, requires that the three most significant bits to define the page be concatenated with the seven least significant bits of the offset address within the page. The 8 bit Slave address will then be the seven bit register offset address within the active page padded with a leading zero.

The three page bits are located in the single Page Register at the offset location set by the lower seven bits of 0x7F or equivalently at the extended address defined by the lower ten bits of 0x07F. This single page register can be accessed directly for reading or writing from any other page at offset address x7F, or equivalently, at the extended addresses x07F, x0FF, x17F, x1FF, x27F, x2FF, x37F and x3FF.

Said another way, the Page Register located in Page 0 is mapped into the offset address space of every other page at the offset address 0x7F. This means that regardless of the page currently selected, any bus transaction to offset address 0x7F always accesses the Page Register.

If access to a different page is required, a separate write to the Page Register is required. This makes the new page active and all subsequent reads and writes can be made anywhere within that page. It is recommended that the page pointer is set back to 0 once any contiguous set of transactions are completed.

After reset with no EEPROM load, all the registers are set to their default values. All DPLL and APLL3 registers are available to either read or write via the microprocessor slave interface. If the device is loaded from an EEPROM on the I2C Master bus, two things must be kept in mind. First, changes in the Page Register cannot be made by the EEPROM. The page register within each page then must mimic the required Page Register changes to step across the pages sequentially. That is, x07F = x01, x0FF = x02, x17F = x03, ..., x37F = x07. Second, APLL3 must still be programmed from the Slave bus because the SMU Master can only issue a single address on the master bus.

The access of the Multi-word Registers is different from that of the Single-worded Registers. Consider the register `interrupt_mask_cnfg[31:0]` on page 0 and spanning offset addresses x0B, x0C, x0D and x0E. The write operation for Multi-word Registers follows a fixed sequence. The register x0B is configured first and the register x0E is configured last. The four registers are configured continuously and should not be interrupted by any operation. The mask configuration will take effect after all four registers are configured. During read operation, the x0B is read first and the register x0E is read last.

Certain bit locations within the device register map are designated as Reserved. To ensure proper and predictable operation, bits designated as Reserved must be left with their default values. If using EEPROM, the bits designated as Reserved must be set with their default values.

### 3 DPLL Register Map

Table 1: Register Map

| Address                  | Register (Abbrev)                         | Register Name  |
|--------------------------|---|--|
| Global Control Registers |   |  |
| 0x00                     | id  | Identification Register  |
| 0x01                     | mpu_sel_cfg                               | MPU Selection Configuration Register                                 |
| 0x02                     | xo_freq_cfg                               | XO Frequency Configuration Register                                  |
| 0x03                     | nominal_freq_cfg[7:0]                     | Nominal Frequency Configuration Register [23:0]                      |
| 0x04                     | nominal_freq_cfg[15:8]                    |  |
| 0x05                     | nominal_freq_cfg[23:16]                   |  |
| 0x06                     | interrupt_cfg                             | Interrupt Configuration Register                                     |
| 0x07                     | interrupt_sts[7:0]                        | Interrupt Status Register [7:0]                                      |
| 0x08                     | interrupt_sts[15:8]                       | Interrupt Status Register [15:8]                                     |
| 0x09                     | interrupt_sts[23:16]                      | Interrupt Status Register [23:16]                                    |
| 0x0A                     | interrupt_sts[31:24]                      | Interrupt Status Register [31:24]                                    |
| 0x0B                     | interrupt_mask_cfg[7:0]                   | Interrupt Mask Configuration Register [7:0]                          |
| 0x0C                     | interrupt_mask_cfg[15:8]                  | Interrupt Mask Configuration Register [15:8]                         |
| 0x0D                     | interrupt_mask_cfg[23:16]                 | Interrupt Mask Configuration Register [23:16]                        |
| 0x0E                     | interrupt_mask_cfg[31:24]                 | Interrupt Mask Configuration Register [31:24]                        |
| 0x0F                     | i2c_slave_addr_cfg                        | I2C Slave Address Configuration Register                             |
| Pre-Divider Registers    |   |  |
| 0x11–0x12                | in{1:2}_cfg                               | Input {1:2} Configuration Register                                   |
| 0x13–0x1E                | in{3:14}_cfg                              | Input {3:14} Configuration Register                                  |
| 0x1F                     | hf_div_cfg[7:0]                           | High Frequency Divider Configuration Register [7:0] for input {3:6}  |
| 0x20                     | hf_div_cfg[11:8]                          | High Frequency Divider Configuration Register [11:8] for input {7:8} |
| 0x21                     | in_pdn_cfg                                | Input Power-Down Configuration Register for input {1:8}              |
| 0x2C                     | in3_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]                 |
| 0x2D                     | in3_fec_divp_cfg[15:8] – Starting address |  |
| 0x2E                     | in3_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0]               |
| 0x2F                     | in3_fec_divq_cfg[15:8] – Starting address |  |
| 0x30                     | in3_pre_divn_cfg[7:0] – Starting address  | Input {3:14} Pre-divider Denominator N Register [14:0]               |
| 0x31                     | in3_pre_divn_cfg[14:8] – Starting address |  |
| 0x32                     | in4_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]                 |
| 0x33                     | in4_fec_divp_cfg[15:8] – Starting address |  |
| 0x34                     | in4_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0]               |
| 0x35                     | in4_fec_divq_cfg[15:8] – Starting address |  |

Table 1: Register Map (Continued)

| Address | Register (Abbrev)                          | Register Name  |
|---------|--|--|
| 0x36    | in4_pre_divn_cfg[7:0] – Starting address   | Input {3:14} Pre-divider Denominator N Register [14:0] |
| 0x37    | in4_pre_divn_cfg[14:8] – Starting address  |  |
| 0x38    | in5_fec_divp_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Numerator P Register [15:0]   |
| 0x39    | in5_fec_divp_cfg[15:8] – Starting address  |  |
| 0x3A    | in5_fec_divq_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Denominator Q Register [15:0] |
| 0x3B    | in5_fec_divq_cfg[15:8] – Starting address  |  |
| 0x3C    | in5_pre_divn_cfg[7:0] – Starting address   | Input {3:14} Pre-divider Denominator N Register [14:0] |
| 0x3D    | in5_pre_divn_cfg[14:8] – Starting address  |  |
| 0x3E    | in6_fec_divp_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Numerator P Register [15:0]   |
| 0x3F    | in6_fec_divp_cfg[15:8] – Starting address  |  |
| 0x40    | in6_fec_divq_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Denominator Q Register [15:0] |
| 0x41    | in6_fec_divq_cfg[15:8] – Starting address  |  |
| 0x42    | in6_pre_divn_cfg[7:0] – Starting address   | Input {3:14} Pre-divider Denominator N Register [14:0] |
| 0x43    | in6_pre_divn_cfg[14:8] – Starting address  |  |
| 0x44    | in7_fec_divp_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Numerator P Register [15:0]   |
| 0x45    | in7_fec_divp_cfg[15:8] – Starting address  |  |
| 0x46    | in7_fec_divq_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Denominator Q Register [15:0] |
| 0x47    | in7_fec_divq_cfg[15:8] – Starting address  |  |
| 0x48    | in7_pre_divn_cfg[7:0] – Starting address   | Input {3:14} Pre-divider Denominator N Register [14:0] |
| 0x49    | in7_pre_divn_cfg[14:8] – Starting address  |  |
| 0x4A    | in8_fec_divp_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Numerator P Register [15:0]   |
| 0x4B    | in8_fec_divp_cfg[15:8] – Starting address  |  |
| 0x4C    | in8_fec_divq_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Denominator Q Register [15:0] |
| 0x4D    | in8_fec_divq_cfg[15:8] – Starting address  |  |
| 0x4E    | in8_pre_divn_cfg[7:0] – Starting address   | Input {3:14} Pre-divider Denominator N Register [14:0] |
| 0x4F    | in8_pre_divn_cfg[14:8] – Starting address  |  |
| 0x50    | in9_fec_divp_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Numerator P Register [15:0]   |
| 0x51    | in9_fec_divp_cfg[15:8] – Starting address  |  |
| 0x52    | in9_fec_divq_cfg[7:0] – Starting address   | Input {3:14} FEC Divider Denominator Q Register [15:0] |
| 0x53    | in9_fec_divq_cfg[15:8] – Starting address  |  |
| 0x54    | in9_pre_divn_cfg[7:0] – Starting address   | Input {3:14} Pre-divider Denominator N Register [14:0] |
| 0x55    | in9_pre_divn_cfg[14:8] – Starting address  |  |
| 0x56    | in10_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]   |
| 0x57    | in10_fec_divp_cfg[15:8] – Starting address |  |
| 0x58    | in10_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0] |
| 0x59    | in10_fec_divq_cfg[15:8] – Starting address |  |

Table 1: Register Map (Continued)

| Address                     | Register (Abbrev)                          | Register Name   |
|-----------------------------|--|---|
| 0x5A                        | in10_pre_divn_cfg[7:0] – Starting address  | Input {3:14} Pre-divider Denominator N Register [14:0]  |
| 0x5B                        | in10_pre_divn_cfg[14:8] – Starting address |   |
| 0x5C                        | in11_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]    |
| 0x5D                        | in11_fec_divp_cfg[15:8] – Starting address |   |
| 0x5E                        | in11_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0]  |
| 0x5F                        | in11_fec_divq_cfg[15:8] – Starting address |   |
| 0x60                        | in11_pre_divn_cfg[7:0] – Starting address  | Input {3:14} Pre-divider Denominator N Register [14:0]  |
| 0x61                        | in11_pre_divn_cfg[14:8] – Starting address |   |
| 0x62                        | in12_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]    |
| 0x63                        | in12_fec_divp_cfg[15:8] – Starting address |   |
| 0x64                        | in12_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0]  |
| 0x65                        | in12_fec_divq_cfg[15:8] – Starting address |   |
| 0x66                        | in12_pre_divn_cfg[7:0] – Starting address  | Input {3:14} Pre-divider Denominator N Register [14:0]  |
| 0x67                        | in12_pre_divn_cfg[14:8] – Starting address |   |
| 0x68                        | in13_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]    |
| 0x69                        | in13_fec_divp_cfg[15:8] – Starting address |   |
| 0x6A                        | in13_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0]  |
| 0x6B                        | in13_fec_divq_cfg[15:8] – Starting address |   |
| 0x6C                        | in13_pre_divn_cfg[7:0] – Starting address  | Input {3:14} Pre-divider Denominator N Register [14:0]  |
| 0x6D                        | in13_pre_divn_cfg[14:8] – Starting address |   |
| 0x6E                        | in14_fec_divp_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Numerator P Register [15:0]    |
| 0x6F                        | in14_fec_divp_cfg[15:8] – Starting address |   |
| 0x70                        | in14_fec_divq_cfg[7:0] – Starting address  | Input {3:14} FEC Divider Denominator Q Register [15:0]  |
| 0x71                        | in14_fec_divq_cfg[15:8] – Starting address |   |
| 0x72                        | in14_pre_divn_cfg[7:0] – Starting address  | Input {3:14} Pre-divider Denominator N Register [14:0]  |
| 0x73                        | in14_pre_divn_cfg[14:8] – Starting address |   |
| 0x7F                        | page_reg                                   | Page Register   |
| Reference Monitor Registers |  |   |
| 0x80                        | freq_mon_factor_cfg                        | Frequency Monitor Factor Configuration Register         |
| 0x81                        | hard_freq_mon_threshold_cfg                | Hard Frequency Monitor Threshold Configuration Register |
| 0x82                        | soft_freq_mon_threshold_cfg                | Soft Frequency Monitor Threshold Configuration Register |
| 0x83                        | upper_threshold_0_cfg                      | Upper Threshold {0:3} Configuration Register            |
| 0x84                        | lower_threshold_0_cfg                      | Lower Threshold {0:3} Configuration Register            |
| 0x85                        | bucket_size_0_cfg                          | Bucket Size {0:3} Configuration Register                |
| 0x86                        | decay_rate_0_cfg                           | Decay Rate {0:3} Configuration Register                 |

Table 1: Register Map (Continued)

| Address         | Register (Abbrev)                   | Register Name  |
|-----------------|-------------------------------------|--|
| 0x87            | *_1_cnfg – Starting address         | Upper Threshold {0:3} Configuration Register           |
| 0x8B            | *_2_cnfg – Starting address         | Upper Threshold {0:3} Configuration Register           |
| 0x8F            | *_3_cnfg – Starting address         | Upper Threshold {0:3} Configuration Register           |
| 0x93–0xA0       | in{1:14}_freq_read_sts              | Input {1:14} Frequency Read Status Register            |
| 0xA1            | remote_input_valid_cnfg[8:1]        | Remote Input Valid Configuration Register [8:1]        |
| 0xA2            | remote_input_valid_cnfg[14:9]       | Remote Input Valid Configuration Register [14:9]       |
| 0xA3            | phase_alarm_time_cnfg               | Phase Alarm Time Configuration Register                |
| 0xA4            | los_sts                             | Loss of Signal Status Register                         |
| 0xA5–0xB2       | in{1:14}_sts                        | Input {1:14} Status Register                           |
| 0xB3–0xB4       | in{1:2}_los_sync_cnfg               | Input {1:2} LOS Sync Configuration Register            |
| 0xB5–0xC0       | in{3:14}_los_sync_cnfg              | Input {3:14} LOS Sync Configuration Register           |
| 0xC1            | in{4-1}_sync_phase_cnfg             | Input 4–1 Sync Phase Configuration Register            |
| 0xC2            | in{8-5}_sync_phase_cnfg             | Input 8–5 Sync Phase Configuration Register            |
| 0xC3            | in{12-9}_sync_phase_cnfg            | Input 12–9 Sync Phase Configuration Register           |
| 0xC4            | in{14-13}_sync_phase_cnfg           | Input 14–13 Sync Phase Configuration Register          |
| 0xC5–0xD0       | in{3:14}_phase_offset_cnfg          | Input {3:14} Phase Offset Configuration Register       |
| 0x0FF           | page_reg                            | Page Register  |
| DPLL1 Registers |                                     |  |
| 0x100           | dpll1_priority_table_sts[7:0]       | dpll1 Priority Table Status Register [7:0]             |
| 0x101           | dpll1_priority_table_sts[15:8]      | dpll1 Priority Table Status Register [15:8]            |
| 0x102           | dpll1_operating_sts                 | dpll1 Operating Status Register                        |
| 0x103           | dpll1_current_dpll_freq_sts[7:0]    | dpll1 Current DPLL Frequency Status Register [39:0]    |
| 0x104           | dpll1_current_dpll_freq_sts[15:8]   |  |
| 0x105           | dpll1_current_dpll_freq_sts[23:16]  |  |
| 0x106           | dpll1_current_dpll_freq_sts[31:24]  |  |
| 0x107           | dpll1_current_dpll_freq_sts[39:32]  |  |
| 0x108           | dpll1_current_dpll_phase_sts[7:0]   | dpll1 Current DPLL Phase Status Register [19:0]        |
| 0x109           | dpll1_current_dpll_phase_sts[15:8]  |  |
| 0x10A           | dpll1_current_dpll_phase_sts[19:16] |  |
| 0x116           | dpll1_input_mode_cnfg               | dpll1 Input Mode Configuration Register                |
| 0x117           | dpll1_mon_sw_pbo_cnfg               | dpll1 Monitor Software Register                        |
| 0x118           | dpll1_in1_in2_sel_priority_cnfg     | dpll1 Input 1/2 Select Priority Configuration Register |
| 0x119           | dpll1_in3_in4_sel_priority_cnfg     | dpll1 Input 3/4 Select Priority Configuration Register |
| 0x11A           | dpll1_in5_in6_sel_priority_cnfg     | dpll1 Input 5/6 Select Priority Configuration Register |
| 0x11B           | dpll1_in7_in8_sel_priority_cnfg     | dpll1 Input 7/8 Select Priority Configuration Register |

Table 1: Register Map (Continued)

| Address     | Register (Abbrev)                     | Register Name   |
|-------------|---------------------------------------|---|
| 0x11C       | dpll1_in9_in10_sel_priority_cfg       | dpll1 Input 9/10 Select Priority Configuration Register       |
| 0x11D       | dpll1_in11_in12_sel_priority_cfg      | dpll1 Input 11/12 Select Priority Configuration Register      |
| 0x11E       | dpll1_in13_in14_sel_priority_cfg      | dpll1 Input 13/14 Select Priority Configuration Register      |
| 0x11F       | dpll1_input_sel_cfg                   | dpll1 Input Select Configuration Register                     |
| 0x120       | dpll1_operating_mode_cfg              | dpll1 Operating Mode Configuration Register                   |
| 0x121       | dpll1_fb_sel_cfg                      | dpll1 Feedback Select Configuration Register                  |
| 0x122       | dpll1_update_event_cfg                | dpll1 Update Event Configuration Register                     |
| 0x123       | dpll1_dppll_path_cfg                  | dpll1 DPLL Path Configuration Register                        |
| 0x124       | dpll1_dppll_start_bw_damping_cfg      | dpll1 DPLL Start Bandwidth Damping Configuration Register     |
| 0x125       | dpll1_dppll_acq_bw_damping_cfg        | dpll1 DPLL Acquired Bandwidth Damping Configuration Register  |
| 0x126       | dpll1_dppll_locked_bw_damping_cfg     | dpll1 DPLL Locked Bandwidth Configuration Register            |
| 0x127       | dpll1_bw_overshoot_cfg                | dpll1 Bandwidth Overshoot Configuration Register              |
| 0x128       | dpll1_phase_loss_coarse_limit_cfg     | dpll1 Phase Loss Coarse Limit Configuration Register          |
| 0x129       | dpll1_phase_loss_fine_limit_cfg       | dpll1 Phase Loss Fine Limit Configuration Register            |
| 0x12A       | dpll1_holdover_mode_cfg[7:0]          | dpll1 Holdover Mode Configuration Register [7:0]              |
| 0x12B       | dpll1_holdover_mode_cfg[15:8]         | dpll1 Holdover Mode Configuration Register [15:8]             |
| 0x12C       | dpll1_holdover_freq_cfg[7:0]          | dpll1 Holdover Frequency Configuration Register               |
| 0x12D       | dpll1_holdover_freq_cfg[15:8]         |   |
| 0x12E       | dpll1_holdover_freq_cfg[23:16]        |   |
| 0x12F       | dpll1_holdover_freq_cfg[31:24]        |   |
| 0x130       | dpll1_holdover_freq_cfg[39:32]        |   |
| 0x131       | dpll1_dppll_freq_soft_limit_cfg       |   |
| 0x132       | dpll1_dppll_freq_hard_limit_cfg[7:0]  | dpll1 DPLL Frequency Hard Limit Configuration Register [7:0]  |
| 0x133       | dpll1_dppll_freq_hard_limit_cfg[15:8] | dpll1 DPLL Frequency Hard Limit Configuration Register [15:8] |
| 0x13E       | dpll1_fr_mfr_sync_cfg                 | dpll1 Frame/Multi-Frame Sync Configuration Register           |
| 0x13F       | dpll1_sync_monitor_cfg                | dpll1 Sync Monitor Configuration Register                     |
| 0x140       | dpll1_sync_edge_cfg                   | dpll1 Sync Edge Configuration Register                        |
| 0x141–0x142 | reserved                              | reserved  |
| 0x143       | dpll1_phase_offset_cfg[7:0]           | dpll1 Phase Offset Configuration Register [28:0]              |
| 0x144       | dpll1_phase_offset_cfg[15:8]          |   |
| 0x145       | dpll1_phase_offset_cfg[23:15]         |   |
| 0x146       | dpll1_phase_offset_cfg[28:24]         |   |
| 0x147       | dpll1_timer_interval[7:0]             | dpll1 Timer Interval Register [7:0]                           |
| 0x148       | dpll1_timer_interval[13:8]            | dpll1 Timer Interval Register [13:8]                          |

Table 1: Register Map (Continued)

| Address         | Register (Abbrev)                 | Register Name  |
|-----------------|-----------------------------------|--|
| 0x149           | dpll1_sys_time_sts[7:0]           | dpll1 System Time Status Register                          |
| 0x14A           | dpll1_sys_time_sts[15:8]          |  |
| 0x14B           | dpll1_sys_time_sts[23:15]         |  |
| 0x14C           | dpll1_sys_time_sts[31:24]         |  |
| 0x14D           | dpll1_bw_sw_time1_cfg             | dpll1 Bandwidth Software Time 1 Configuration Register     |
| 0x14E           | dpll1_bw_sw_time2_cfg             | dpll1 Bandwidth Software Time 2 Configuration Register     |
| 0x14F           | dpll1_bw_sw_time2_cfg             | dpll1 Bandwidth Software Time 3 Configuration Register     |
| 0x150           | dpll1_slave_force_ref_sel_cfg     | dpll1 Slave Force Reference Select Configuration Register  |
| 0x151           | dpll1_prog_ph_limit_cfg[7:0]      | dpll1 Program Limit Configuration Register [23:0]          |
| 0x152           | dpll1_prog_ph_limit_cfg[15:8]     |  |
| 0x153           | dpll1_prog_ph_limit_cfg[23:16]    |  |
| 0x17F           | page_reg                          | Page Register  |
| DPLL2 Registers |                                   |  |
| 0x200           | dpll2_priority_table_sts[7:0]     | DPLL2 Priority Table Status Register [7:0]                 |
| 0x201           | dpll2_priority_table_sts[15:8]    | DPLL2 Priority Table Status Register [15:8]                |
| 0x202           | dpll2_operating_sts               | DPLL2 Operating Status Register                            |
| 0x203–0x215     | reserved                          | reserved   |
| 0x216           | dpll2_input_mode_cfg              | DPLL2 Input Mode Configuration Register                    |
| 0x217           | dpll2_mon_cfg                     | DPLL2 Monitor Configuration Register                       |
| 0x218           | dpll2_in1_in2_sel_priority_cfg    | DPLL2 Input 1/2 Select Priority Configuration Register     |
| 0x219           | dpll2_in3_in4_sel_priority_cfg    | DPLL2 Input 3/4 Select Priority Configuration Register     |
| 0x21A           | dpll2_in5_in6_sel_priority_cfg    | DPLL2 Input 5/6 Select Priority Configuration Register     |
| 0x21B           | dpll2_in7_in8_sel_priority_cfg    | DPLL2 Input 7/8 Select Priority Configuration Register     |
| 0x21C           | dpll2_in9_in10_sel_priority_cfg   | DPLL2 Input 9/10 Select Priority Configuration Register    |
| 0x21D           | dpll2_in11_in12_sel_priority_cfg  | DPLL2 Input 11/12 Select Priority Configuration Register   |
| 0x21E           | dpll2_in13_in14_sel_priority_cfg  | DPLL2 Input 13/14 Select Priority Configuration Register   |
| 0x21F           | dpll2_input_sel_cfg               | DPLL2 Input Select Configuration Register                  |
| 0x220           | dpll2_operating_mode_cfg          | DPLL2 Operating Mode Configuration Register                |
| 0x221–0x225     | reserved                          | reserved   |
| 0x226           | dpll2_dpll_locked_bw_damping_cfg  | DPLL2 DPLL Locked Bandwidth Damping Configuration Register |
| 0x227           | reserved                          | Reserved   |
| 0x228           | dpll2_phase_loss_coarse_limit_cfg | DPLL2 Phase Loss Coarse Limit Register                     |
| 0x229           | dpll2_phase_loss_fine_limit_cfg   | DPLL2 Phase Loss Fine Limit Configuration Register         |
| 0x22A           | reserved                          | reserved   |
| 0x22B           | dpll2_holdover_mode_cfg           | DPLL2 Holdover Mode Configuration Register                 |



Table 1: Register Map (Continued)

| Address         | Register (Abbrev)                    | Register Name   |
|-----------------|--------------------------------------|---|
| 0x22C–0x230     | reserved                             | reserved  |
| 0x231           | dpll2_dpll_freq_soft_limit_cfg       | DPLL2 DPLL Frequency Soft Limit Configuration Register        |
| 0x232           | dpll2_dpll_freq_hard_limit_cfg[7:0]  | DPLL2 DPLL Frequency Hard Limit Configuration Register [7:0]  |
| 0x233           | dpll2_dpll_freq_hard_limit_cfg[15:8] | DPLL2 DPLL Frequency Hard Limit Configuration Register [15:8] |
| 0x250           | dpll2_fbdiv_cfg[7:0]                 | DPLL2 Feedback Divisor Configuration Register [7:0]           |
| 0x251           | dpll2_fbdiv_cfg[13:8]                | DPLL2 Feedback Divisor Configuration Register [13:8]          |
| 0x252           | dpll2_divn_frac_l_cfg                | DPLL2 Divisor N Fractional L Configuration Register           |
| 0x253           | dpll2_divn_frac_m_cfg                | DPLL2 Divisor N Fractional M Configuration Register           |
| 0x254           | dpll2_divn_frac_h_cfg                | DPLL2 Divisor N Fractional H Configuration Register           |
| 0x255           | dpll2_divn_den_l_cfg                 | DPLL2 Divisor N Denominator L Configuration Register          |
| 0x256           | dpll2_divn_den_h_cfg                 | DPLL2 Divisor N Denominator H Configuration Register          |
| 0x257           | dpll2_divn_num_l_cfg                 | DPLL2 Divisor N Numerator L Configuration Register            |
| 0x258           | dpll2_divn_num_h_cfg                 | DPLL2 Divisor N Numerator H Configuration Register            |
| 0x259           | dpll2_divn_int_cfg                   | DPLL2 Divisor N Interrupt Configuration Register              |
| 0x25A–0x25B     | reserved                             | reserved  |
| 0x25C           | dpll2_dpll_dsm_cfg                   | DPLL2 DPLL DSM Configuration Register                         |
| 0x25D–0x27E     | reserved                             | reserved  |
| 0x27F           | page_reg                             | Page Register   |
| APLL1 Registers |                                      |   |
| 0x280           | apl1_icp_ctrl_cfg                    | APLL1 Charge Pump Current Control Configuration Register      |
| 0x281           | apl1_divisor_frac_l_cfg              | APLL1 Divisor Fractional L Configuration Register             |
| 0x282           | apl1_divisor_frac_m_cfg              | APLL1 Divisor Fractional M Configuration Register             |
| 0x283           | apl1_divisor_frac_h_cfg              | APLL1 Divisor Fractional H Configuration Register             |
| 0x284           | apl1_divisor_den_l_cfg               | APLL1 Divisor Denominator L Configuration Register            |
| 0x285           | apl1_divisor_den_h_cfg               | APLL1 Divisor Denominator H Configuration Register            |
| 0x286           | apl1_divisor_num_l_cfg               | APLL1 Divisor Numerator L Configuration Register              |
| 0x287           | apl1_divisor_num_h_cfg               | APLL1 Divisor Numerator H Configuration Register              |
| 0x288           | apl1_dsm_cfg                         | APLL1 DSM Configuration Register                              |
| 0x289           | apl1_divisor_int_cfg                 | APLL1 Divisor Integer Configuration Register                  |
| 0x28A           | apl1_fr_ratio_cfg[7:0]               | APLL1 Frame/Multi-Frame Ratio Configuration Register [7:0]    |
| 0x28B           | apl1_fr_ratio_cfg[15:8]              | APLL1 Frame/Multi-Frame Ratio Configuration Register [15:8]   |
| 0x28C           | apl1_fr_ratio_cfg[23:16]             | APLL1 Frame/Multi-Frame Ratio Configuration Register [23:16]  |
| 0x28D           | apl1_fr_ratio_cfg[28:24]             | APLL1 Frame/Multi-Frame Ratio Configuration Register [28:24]  |
| 0x28E           | apl2_icp_ctrl_cfg                    | APLL2 Change Pump Current Control Configuration Register      |
| 0x28F           | apl2_divisor_frac_l_cfg              | APLL2 Divisor Fractional L Configuration Register             |

Table 1: Register Map (Continued)

| Address                  | Register (Abbrev)        | Register Name  |
|--------------------------|--------------------------|--|
| 0x290                    | apl2_divisor_frac_m_cfg  | APLL2 Divisor Fractional M Configuration Register            |
| 0x291                    | apl2_divisor_frac_h_cfg  | APLL2 Divisor Fractional H Configuration Register            |
| 0x292                    | apl2_divisor_den_l_cfg   | APLL2 Divisor Denominator L Configuration Register           |
| 0x293                    | apl2_divisor_den_h_cfg   | APLL2 Divisor Denominator H Configuration Register           |
| 0x294                    | apl2_divisor_num_l_cfg   | APLL2 Divisor Numerator L Configuration Register             |
| 0x295                    | apl2_divisor_num_h_cfg   | APLL2 Divisor Numerator H Configuration Register             |
| 0x296                    | apl2_dsm_cfg             | APLL2 DSM Configuration Register                             |
| 0x297                    | apl2_divisor_int_cfg     | APLL2 Divisor Integer Configuration Register                 |
| 0x298                    | apl2_fr_ratio_cfg[7:0]   | APLL2 Frame/Multi-Frame Ratio Configuration Register [7:0]   |
| 0x299                    | apl2_fr_ratio_cfg[15:8]  | APLL2 Frame/Multi-Frame Ratio Configuration Register [15:8]  |
| 0x29A                    | apl2_fr_ratio_cfg[23:16] | APLL2 Frame/Multi-Frame Ratio Configuration Register [23:16] |
| 0x29B                    | apl2_fr_ratio_cfg[28:24] | APLL2 Frame/Multi-Frame Ratio Configuration Register [28:24] |
| System Registers         |                          |  |
| 0x29C                    | rsvd                     | Reserved Register  |
| 0x29D                    | rsvd                     | Reserved Register  |
| 0x29E                    | rsvd                     | Reserved Register  |
| 0x29F                    | rsvd                     | Reserved Register  |
| 0x2A0                    | rsvd                     | Reserved Register  |
| 0x2A1                    | rsvd                     | Reserved Register  |
| 0x2A2                    | rsvd                     | Reserved Register  |
| 0x2A3                    | rsvd                     | Reserved Register  |
| 0x2A4                    | rsvd                     | Reserved Register  |
| 0x2A5                    | rsvd                     | Reserved Register  |
| 0x2A6                    | rsvd                     | Reserved Register  |
| 0x2A7-0x2FE              | rsvd                     | Reserved Register  |
| 0x2FF                    | page_reg                 | Page Register  |
| Output Divider Registers |                          |  |
| 0x300                    | out1_mux_cfg             | Output 1 Mux Configuration Register                          |
| 0x301                    | out1_div1_cfg            | Output 1 Divisor 1 Configuration Register [4:0]              |
| 0x302                    | out1_div2_cfg[7:0]       | Output 1 Divisor 2 Configuration Register [26:0]             |
| 0x303                    | out1_div2_cfg[15:8]      |  |
| 0x304                    | out1_div2_cfg[23:16]     |  |
| 0x305                    | out1_div2_cfg[26:24]     |  |
| 0x306                    | out1_ph1_cfg             | Output 1 Phase 1 Configuration Register [4:0]                |

Table 1: Register Map (Continued)

| Address | Register (Abbrev)     | Register Name                                     |
|---------|-----------------------|---|
| 0x307   | out1_ph2_cnfg[7:0]    | Output 1 Phase 2 Configuration Register [26:0]    |
| 0x308   | out1_ph2_cnfg[15:8]   |   |
| 0x309   | out1_ph2_cnfg[23:16]  |   |
| 0x30A   | out1_ph2_cnfg[26:24]  |   |
| 0x30B   | out1_fine_ph_cnfg     | Output 1 Fine Phase Configuration Register        |
| 0x30C   | out2_mux_cnfg         | Output 2 Mux Configuration Register               |
| 0x30D   | out2_div1_cnfg        | Output 2 Divisor 1 Configuration Register [4:0]   |
| 0x30E   | out2_div2_cnfg[7:0]   | Output 2 Divisor 2 Configuration Register [26:0]  |
| 0x30F   | out2_div2_cnfg[15:8]  |   |
| 0x310   | out2_div2_cnfg[23:16] |   |
| 0x311   | out2_div2_cnfg[26:24] |   |
| 0x312   | out2_ph1_cnfg[4:0]    | Output 2 Phase 1 Configuration Register [4:0]     |
| 0x313   | out2_ph2_cnfg[7:0]    | Output 2 Phase 2 Configuration Register [7:0]     |
| 0x314   | out2_ph2_cnfg[15:8]   | Output 2 Phase 2 Configuration Register [15:8]    |
| 0x315   | out2_ph2_cnfg[23:16]  | Output 2 Phase 2 Configuration Register [23:16]   |
| 0x316   | out2_ph2_cnfg[26:24]  | Output 2 Phase 2 Configuration Register [26:24]   |
| 0x317   | out2_fine_ph_cnfg     | Output 2 Fine Phase Configuration Register        |
| 0x318   | out3_mux_cnfg         | Output 3 Mux Configuration Register               |
| 0x319   | out3_div1_cnfg[4:0]   | Output 3 Divisor 1 Configuration Register [4:0]   |
| 0x31A   | out3_div2_cnfg[7:0]   | Output 3 Divisor 2 Configuration Register [7:0]   |
| 0x31B   | out3_div2_cnfg[15:8]  | Output 3 Divisor 2 Configuration Register [15:8]  |
| 0x31C   | out3_div2_cnfg[23:16] | Output 3 Divisor 2 Configuration Register [23:16] |
| 0x31D   | out3_div2_cnfg[26:24] | Output 3 Divisor 2 Configuration Register [26:24] |
| 0x31E   | out3_ph1_cnfg[4:0]    | Output 3 Phase 1 Configuration Register [4:0]     |
| 0x31F   | out3_ph2_cnfg[7:0]    | Output 3 Phase 2 Configuration Register [7:0]     |
| 0x320   | out3_ph2_cnfg[15:8]   | Output 3 Phase 2 Configuration Register [15:8]    |
| 0x321   | out3_ph2_cnfg[23:16]  | Output 3 Phase 2 Configuration Register [23:16]   |
| 0x322   | out3_ph2_cnfg[26:24]  | Output 3 Phase 2 Configuration Register [26:24]   |
| 0x323   | out3_ph2_cnfg[26:24]  | Output 3 Fine Phase Configuration Register        |
| 0x324   | out4_mux_cnfg         | Output 4 Mux Configuration Register               |
| 0x325   | out4_div1_cnfg[4:0]   | Output 4 Divisor 1 Configuration Register [4:0]   |
| 0x326   | out4_div2_cnfg[7:0]   | Output 4 Divisor 2 Configuration Register [7:0]   |
| 0x327   | out4_div2_cnfg[15:8]  | Output 4 Divisor 2 Configuration Register [15:8]  |
| 0x328   | out4_div2_cnfg[23:16] | Output 4 Divisor 2 Configuration Register [23:16] |
| 0x329   | out4_div2_cnfg[26:24] | Output 4 Divisor 2 Configuration Register [26:24] |
| 0x32A   | out4_ph1_cnfg[4:0]    | Output 4 Phase 1 Configuration Register [4:0]     |

Table 1: Register Map (Continued)

| Address | Register (Abbrev)    | Register Name                                     |
|---------|----------------------|---|
| 0x32B   | out4_ph2_cfg[7:0]    | Output 4 Phase 2 Configuration Register [7:0]     |
| 0x32C   | out4_ph2_cfg[15:8]   | Output 4 Phase 2 Configuration Register [15:8]    |
| 0x32D   | out4_ph2_cfg[23:16]  | Output 4 Phase 2 Configuration Register [23:16]   |
| 0x32E   | out4_ph2_cfg[26:24]  | Output 4 Phase 2 Configuration Register [26:24]   |
| 0x32F   | out4_fine_ph_cfg     | Output 4 Fine Phase Configuration Register        |
| 0x330   | out5_mux_cfg         | Output 5 Mux Configuration Register               |
| 0x331   | out5_div1_cfg[4:0]   | Output 5 Divisor 1 Configuration Register [4:0]   |
| 0x332   | out5_div2_cfg[7:0]   | Output 5 Divisor 2 Configuration Register [7:0]   |
| 0x333   | out5_div2_cfg[15:8]  | Output 5 Divisor 2 Configuration Register [15:8]  |
| 0x334   | out5_div2_cfg[23:16] | Output 5 Divisor 2 Configuration Register [23:16] |
| 0x335   | out5_div2_cfg[26:24] | Output 5 Divisor 2 Configuration Register [26:24] |
| 0x336   | out5_ph1_cfg[4:0]    | Output 5 Phase 1 Configuration Register [4:0]     |
| 0x337   | out5_ph2_cfg[7:0]    | Output 5 Phase 2 Configuration Register [7:0]     |
| 0x338   | out5_ph2_cfg[15:8]   | Output 5 Phase 2 Configuration Register [15:8]    |
| 0x339   | out5_ph2_cfg[23:16]  | Output 5 Phase 2 Configuration Register [23:16]   |
| 0x33A   | out5_ph2_cfg[26:24]  | Output 5 Phase 2 Configuration Register [26:24]   |
| 0x33B   | out5_fine_ph_cfg     | Output 5 Fine Phase Configuration Register        |
| 0x33C   | out6_mux_cfg         | Output 6 Mux Configuration Register               |
| 0x33D   | out6_div1_cfg[7:0]   | Output 6 Divisor 1 Configuration Register [7:0]   |
| 0x33E   | out6_div2_cfg[7:0]   | Output 6 Divisor 2 Configuration Register [7:0]   |
| 0x33F   | out6_div2_cfg[15:8]  | Output 6 Divisor 2 Configuration Register [15:8]  |
| 0x340   | out6_div2_cfg[23:16] | Output 6 Divisor 2 Configuration Register [23:16] |
| 0x341   | out6_div2_cfg[26:24] | Output 6 Divisor 2 Configuration Register [26:24] |
| 0x342   | out6_ph1_cfg         | Output 6 Phase 1 Configuration Register [4:0]     |
| 0x343   | out6_ph2_cfg[7:0]    | Output 6 Phase 2 Configuration Register [7:0]     |
| 0x344   | out6_ph2_cfg[15:8]   | Output 6 Phase 2 Configuration Register [15:8]    |
| 0x345   | out6_ph2_cfg[23:16]  | Output 6 Phase 2 Configuration Register [23:16]   |
| 0x346   | out6_ph2_cfg[26:24]  | Output 6 Phase 2 Configuration Register [26:24]   |
| 0x347   | out6_fine_ph_cfg     | Output 6 Fine Phase Configuration Register        |
| 0x348   | out7_mux_cfg         | Output 7 Mux Configuration Register               |
| 0x349   | out7_div1_cfg[7:0]   | Output 7 Divisor 1 Configuration Register [7:0]   |
| 0x34A   | out7_div2_cfg[7:0]   | Output 7 Divisor 2 Configuration Register [7:0]   |
| 0x34B   | out7_div2_cfg[15:8]  | Output 7 Divisor 2 Configuration Register [15:8]  |
| 0x34C   | out7_div2_cfg[23:16] | Output 7 Divisor 2 Configuration Register [23:16] |
| 0x34D   | out7_div2_cfg[26:24] | Output 7 Divisor 2 Configuration Register [26:24] |
| 0x34E   | out7_ph1_cfg[4:0]    | Output 7 Phase 1 Configuration Register [4:0]     |

Table 1: Register Map (Continued)

| Address                 | Register (Abbrev)     | Register Name  |
|-------------------------|-----------------------|--|
| 0x34F                   | out7_ph2_cnfg[7:0]    | Output 7 Phase 2 Configuration Register [7:0]        |
| 0x350                   | out7_ph2_cnfg[15:8]   | Output 7 Phase 2 Configuration Register [15:8]       |
| 0x351                   | out7_ph2_cnfg[23:16]  | Output 7 Phase 2 Configuration Register [23:16]      |
| 0x352                   | out7_ph2_cnfg[26:24]  | Output 7 Phase 2 Configuration Register [26:24]      |
| 0x353                   | out7_fine_ph_cnfg     | Output 7 Fine Phase Configuration Register           |
| 0x354                   | out8_mux_cnfg         | Output 8 Mux Configuration Register                  |
| 0x355                   | out8_div1_cnfg[7:0]   | Output 8 Divisor 1 Configuration Register [7:0]      |
| 0x356                   | out8_div2_cnfg[7:0]   | Output 8 Divisor 2 Configuration Register [7:0]      |
| 0x357                   | out8_div2_cnfg[15:8]  | Output 8 Divisor Configuration Register [15:8]       |
| 0x358                   | out8_div2_cnfg[23:8]  | Output 8 Divisor Configuration Register [23:16]      |
| 0x359                   | out8_div2_cnfg[26:24] | Output 8 Divisor 2 Configuration Register [26:24]    |
| 0x35A                   | out8_ph1_cnfg[4:0]    | Output 8 Phase 1 Configuration Register [4:0]        |
| 0x35B                   | out8_ph2_cnfg[7:0]    | Output 8 Phase 2 Configuration Register [7:0]        |
| 0x35C                   | out8_ph2_cnfg[15:8]   | Output 8 Phase 2 Configuration Register [15:8]       |
| 0x35D                   | out8_ph2_cnfg[23:16]  | Output 8 Phase 2 Configuration Register [23:16]      |
| 0x35E                   | out8_ph2_cnfg[26:24]  | Output 8 Phase 2 Configuration Register [26:24]      |
| 0x35F                   | out8_fine_ph_cnfg     | Output 8 Fine Phase Configuration Register           |
| 0x360                   | out9_freq_cnfg        | Output 9 Frequency Configuration Register            |
| 0x361–0x36B             | rsvd                  | Reserved Register                                    |
| 0x36C                   | out10_cnfg            | Output 10 Configuration Register                     |
| 0x36D                   | out10_freq_cnfg[7:0]  | Output 10 Frequency Configuration Register [7:0]     |
| 0x36E                   | out10_freq_cnfg[14:8] | Output 10 Frequency Configuration Register [14:8]    |
| 0x36F–0x377             | rsvd                  | Reserved Register                                    |
| 0x378                   | out11_cnfg            | Output 11 Configuration Register                     |
| 0x379                   | out11_freq_cnfg[7:0]  | Output 11 Frequency Configuration Register [7:0]     |
| 0x37A                   | out11_freq_cnfg[14:8] | Output 11 Frequency Configuration Register [14:8]    |
| 0x37E                   | fr_mfr_path_cnfg      | Output Frame/Multi-Frame Sync Configuration Register |
| 0x37F                   | page_reg              | Page Register  |
| Manufacturing Registers |                       |  |
| 0x380                   | rsvd                  | Reserved Register                                    |
| 0x381                   | soft_rst              | Soft Reset Register                                  |
| 0x382                   | rsvd                  | Reserved Register                                    |
| 0x383                   | rsvd                  | Reserved Register                                    |
| 0x384                   | rsvd                  | Reserved Register                                    |

Table 1: Register Map (Continued)

| Address | Register (Abbrev) | Register Name       |
|---------|-------------------|---------------------|
| 0x385   | rsvd              | Reserved Register   |
| 0x386   |                   |                     |
| 0x387   |                   |                     |
| 0x388   | rsvd              | Reserved Register   |
| 0x389   |                   |                     |
| 0x38A   |                   |                     |
| 0x38B   | rsvd              | Reserved Register   |
| 0x38C   |                   |                     |
| 0x38D   |                   |                     |
| 0x38E   | rsvd              | Reserved Register   |
| 0x38F   | rsvd              | Reserved Register   |
| 0x390   | rsvd              | Reserved Register   |
| 0x391   | rsvd              | Reserved Register   |
| 0x392   | rsvd              | Reserved Register   |
| 0x393   |                   |                     |
| 0x394   | rsvd              | Reserved Register   |
| 0x395   | rsvd              | Reserved Register   |
| 0x396   | rsvd              | Reserved Register   |
| 0x397   | rsvd              | Reserved Register   |
| 0x398   | rsvd              | Reserved Register   |
| 0x399   | rsvd              | Reserved Register   |
| 0x39A   | rsvd              | Reserved Register   |
| 0x39B   | rsvd              | Reserved Register   |
| 0x39C   | rsvd              | Reserved Register   |
| 0x39D   | rsvd              | Reserved Register   |
| 0x39E   | eeeprom_crc       | EEPROM CRC Register |
| 0x3FF   | page_reg          | Page Register       |

Note: OUT8 is not available for 82P33731. It is routed internally (TO\_APLL3).

## 4 DPLL Register Descriptions

### 4.1 Global Control Registers

#### Identification Register

| Register (Abbrev): id<br>Address: 0x00<br>Type: RO<br>Default Value: xxxx_0010 |             |                        |   |   |   |   |            |
|--|-------------|------------------------|---|---|---|---|------------|
| 7  | 6           | 5                      | 4 | 3 | 2 | 1 | 0          |
| dev_id[7:0]  |             |                        |   |   |   |   |            |
| Bit  | Name        | Description            |   |   |   |   | Def. Value |
| 7:0  | dev_id[7:0] | Device identification. |   |   |   |   | xxxx_0010  |

#### MPU Selection Configuration Register

| Register (Abbrev): mpu_sel_cnfg<br>Address: 0x01<br>Type: RW<br>Default Value: 0000_0xxx |   |   |   |   |                |                   |   |
|--|---|---|---|---|----------------|-------------------|---|
| 7  | 6   | 5   | 4 | 3 | 2              | 1                 | 0   |
| reserved   | reserved                                    |   |   |   | sonet_sdh_cnfg | mpu_sel_cnfg[1:0] |   |
| Bit  | Name  | Description   |   |   |                |                   | Def. Value  |
| 7  | reserved (device)<br>eeprom_rd_spd (EEPROM) | This bit selects the I2C EEPROM read speed.<br>0: 100 kbps<br>1: 400 kbps   |   |   |                |                   | 0   |
| 6:3  | reserved                                    | reserved  |   |   |                |                   | 000_0   |
| 2  | sonet_sdh_cnfg                              | This bit selects the SDH or SONET network type.<br>0: SDH. The DPLL required clock is 2.048 MHz when the in{1:14}_freq bits are '0001'; the output from the 16E1/16T1 path is 16E1.<br>1: SONET. The DPLL required clock is 1.544 MHz when the in{1:14}_freq bits are '0001'; the output from the 16E1/16T1 path is 16T1. |   |   |                |                   | Determined by SONET/SDH pin during reset or EEPROM      |
| 1:0  | mpu_sel_cnfg[1:0]                           | 00: I2C<br>01: SPI<br>10: UART<br>11: EEPROM boot mode (I2C EEPROM (16-bit))  |   |   |                |                   | Determined by MPU_MODE[1:0] pins during reset or EEPROM |

### XO Frequency Configuration Register

| Register (Abbrev): xo_freq_cfg<br>Address: 0x02<br>Type: RO<br>Default Value: 0000_0xxx |                  |  |   |           |                  |   |  |
|---|------------------|--|---|-----------|------------------|---|--|
| 7   | 6                | 5  | 4 | 3         | 2                | 1 | 0  |
| reserved  |                  |  |   | osci_edge | xo_freq_cfg[2:0] |   |  |
| Bit   | Name             | Description  |   |           |                  |   | Def. Value   |
| 7:4   | reserved         | reserved   |   |           |                  |   | 0000   |
| 3   | osci_edge        | This bit selects a better active edge of the master clock.<br>0: The rising edge<br>1: The falling edge                          |   |           |                  |   | 0  |
| 2:0   | xo_freq_cfg[2:0] | 000: 10 MHz<br>001: 12.8 MHz<br>010: 13 MHz<br>011: 19.44 MHz<br>100: 20 MHz<br>101: 24.576 MHz<br>110: 25 MHz<br>111: 30.72 MHz |   |           |                  |   | Determined by XO_FREQ[2:0] pins during reset or EEPROM |

### Nominal Frequency Configuration Register [23:0]

| Register (Abbrev): nominal_freq_cfg[23:0]<br>Address: 0x03, 0x04, 0x05<br>Type: RW<br>Default Value: 0000_0000 |                         |  |   |   |   |   |            |
|--|-------------------------|--|---|---|---|---|------------|
| 7  | 6                       | 5  | 4 | 3 | 2 | 1 | 0          |
| nominal_freq_cfg[7:0]  |                         |  |   |   |   |   |            |
| nominal_freq_cfg[15:8]   |                         |  |   |   |   |   |            |
| nominal_freq_cfg[23:16]  |                         |  |   |   |   |   |            |
| Bit  | Name                    | Description  |   |   |   |   | Def. Value |
| 7:0  | nominal_freq_cfg[7:0]   | nominal_freq_cfg[23:0] represent a 2's complement signed integer.<br>The calibration value for the master clock in ppm is obtained by multiplying this register value by 0.0000884. The calibration range is within $\pm 741$ ppm. |   |   |   |   | 0000_0000  |
|  | nominal_freq_cfg[15:8]  |  |   |   |   |   |            |
|  | nominal_freq_cfg[23:16] |  |   |   |   |   |            |



### Interrupt Configuration Register

| Register (Abbrev): interrupt_cfg<br>Address: 0x06<br>Type: RW<br>Default Value: 0000_0010 |              |  |   |   |   |             |              |
|---|--------------|--|---|---|---|-------------|--------------|
| 7   | 6            | 5  | 4 | 3 | 2 | 1           | 0            |
| reserved  |              |  |   |   |   | tristate_en | int_polarity |
| Bit   | Name         | Description  |   |   |   |             | Def. Value   |
| 7:2   | reserved     | reserved   |   |   |   |             | 0000_00      |
| 1   | tristate_en  | 0: Interrupt pin always driven when inactive<br>1: Interrupt pin only driven when active; high impedance when inactive   |   |   |   |             | 1            |
| 0   | int_polarity | 0: Active-low pin driven low to indicate active interrupt<br>1: Active-high pin driven high to indicate active interrupt |   |   |   |             | 0            |

### Interrupt Status Register [7:0]

| Register (Abbrev): interrupt_sts [7:0] <sup>1</sup><br>Address: 0x07<br>Type: RO<br>Default Value: 0000_0000 |                 |  |   |   |   |   |            |
|--|-----------------|--|---|---|---|---|------------|
| 7  | 6               | 5  | 4 | 3 | 2 | 1 | 0          |
| in[7:0]_sts_int  |                 |  |   |   |   |   |            |
| Bit  | Name            | Description  |   |   |   |   | Def. Value |
| 7:0  | in[7:0]_sts_int | 0: Corresponding input has not changed status (valid/invalid)<br>1: Corresponding input has changed status (valid/invalid)<br>Write 1 to clear |   |   |   |   | 0          |

1. Registers 0x07, 0x08, 0x09, and 0xA0 provide interrupt status information.

### Interrupt Status Register [15:8]

| Register (Abbrev): interrupt_sts [15:8]<br>Address: 0x08<br>Type: RO<br>Default Value: 0000_0000 |                  |  |   |   |   |   |            |
|--|------------------|--|---|---|---|---|------------|
| 7  | 6                | 5  | 4 | 3 | 2 | 1 | 0          |
| reserved   |                  | in[15:8]_sts_int   |   |   |   |   |            |
| Bit  | Name             | Description  |   |   |   |   | Def. Value |
| 7:6  | reserved         | reserved   |   |   |   |   | 00         |
| 5:0  | in[15:8]_sts_int | 0: Corresponding input has not changed status (valid/invalid)<br>1: Corresponding input has changed status (valid/invalid)<br>Write 1 to clear |   |   |   |   | 0          |

### Interrupt Status Register [23:16]

| Register (Abbrev): interrupt_sts[23:16]<br>Address: 0x09<br>Type: RO<br>Default Value: 0000_0000 |                 |  |          |           |          |           |            |
|--|-----------------|--|----------|-----------|----------|-----------|------------|
| 7  | 6               | 5  | 4        | 3         | 2        | 1         | 0          |
| rd_eeeprom_done  | rd_eeeprom_err  | reserved   | reserved | ami2_viol | ami2_los | ami1_viol | ami1_los   |
| Bit  | Name            | Description  |          |           |          |           | Def. Value |
| 7  | rd_eeeprom_done | 1: Start-up read of external I2C EEPROM finished<br>0: Start-up not finished or not initiated<br>Write 0xFF to register to clear this bit. |          |           |          |           | 0          |
| 6  | rd_eeeprom_err  | 1: Error during read of external I2C EEPROM<br>0: No error<br>Write 0xFF to register to clear this bit.                                    |          |           |          |           | 0          |
| 5  | reserved        | reserved   |          |           |          |           | 0000_00    |
| 4  | reserved        | reserved   |          |           |          |           | 0000_00    |
| 3  | ami2_viol       | 0: Input2 has no violation error<br>1: Input2 has violation error<br>Write 1 to clear.   |          |           |          |           | 0          |
| 2  | ami2_los        | 0: Input2 has no los error<br>1: Input2 has los error<br>Write 1 to clear.   |          |           |          |           | 0          |
| 1  | ami1_viol       | 0: Input1 has no violation error<br>1: Input1 has violation error<br>Write 1 clear.  |          |           |          |           | 0          |
| 0  | ami1_los        | 0: Input1 has no los error<br>1: Input1 has los error<br>Write 1 to clear.   |          |           |          |           | 0          |

### Interrupt Status Register [31:24]

| Register (Abbrev): interrupt_sts[31:24]<br>Address: 0x0A<br>Type: RO<br>Default Value: 0000_0000 |                           |   |          |          |          |                           |                        |
|--|---------------------------|---|----------|----------|----------|---------------------------|------------------------|
| 7  | 6                         | 5   | 4        | 3        | 2        | 1                         | 0                      |
| dppll1_operating_mode_sts  | dppll1_main_ref_failed    | dppll1_ex_sync_alarm  | reserved | reserved | reserved | dppll2_operating_mode_sts | dppll2_main_ref_failed |
| Bit  | Name                      | Description   |          |          |          |                           | Def. Value             |
| 7  | dppll1_operating_mode_sts | 0: Operating mode has not changed status<br>1: Operating mode has changed status<br>Write 1 to clear. |          |          |          |                           | 0                      |

### Interrupt Status Register [31:24]

|  |                          |   |   |   |   |   |   |
|--|--------------------------|---|---|---|---|---|---|
| Register (Abbrev): interrupt_sts[31:24]<br>Address: 0x0A<br>Type: RO<br>Default Value: 0000_0000 |                          |   |   |   |   |   |   |
| 7  | 6                        | 5 | 4   | 3 | 2 | 1 | 0 |
| 6  | dpll1_main_ref_failed    |   | 0: Input to the DPLL is qualified<br>1: Input to the DPLL has disqualified<br>Write 1 to clear.                   |   |   |   | 0 |
| 5  | dpll1_ex_sync_alarm      |   | 0: External Input framer sync has not occurred<br>1: External Input framer sync has occurred<br>Write 1 to clear. |   |   |   | 0 |
| 4  | reserved                 |   | reserved  |   |   |   | 0 |
| 3  | reserved                 |   | reserved  |   |   |   | 0 |
| 2  | reserved                 |   | reserved  |   |   |   | 0 |
| 1  | dpll2_operating_mode_sts |   | 0: Operating mode has not changed status<br>1: Operating mode has changed status<br>Write 1 to clear.             |   |   |   | 0 |
| 0  | dpll2_main_ref_failed    |   | 0: Input to the DPLL is qualified<br>1: Input to the DPLL has disqualified<br>Write 1 to clear.                   |   |   |   | 0 |

### Interrupt Mask Configuration Register [7:0]

| Register (Abbrev): interrupt_mask_cnfg[7:0] <sup>1</sup><br>Address: 0x0B<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |   |   |            |
|---|----------------------|---|---|---|---|---|------------|
| 7   | 6                    | 5   | 4 | 3 | 2 | 1 | 0          |
| in[7:0]_sts_int_mask  |                      |   |   |   |   |   |            |
| Bit   | Name                 | Description   |   |   |   |   | Def. Value |
| 7:0   | in[7:0]_sts_int_mask | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |   |   |   |   | 0          |

1. Registers 0x0B, 0x0C, 0x0D, and 0x0E provide interrupt mask configuration information.

### Interrupt Mask Configuration Register [15:8]

| Register (Abbrev): interrupt_mask_cfg[15:8]<br>Address: 0x0C<br>Type: RW<br>Default Value: 0000_0000 |                       |   |   |   |   |   |            |
|--|-----------------------|---|---|---|---|---|------------|
| 7  | 6                     | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved   |                       | in[15:8]_sts_int_mask   |   |   |   |   |            |
| Bit  | Name                  | Description   |   |   |   |   | Def. Value |
| 7:6  | reserved              | reserved  |   |   |   |   | 0          |
| 5:0  | in[15:8]_sts_int_mask | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |   |   |   |   | 0          |

### Interrupt Mask Configuration Register [23:16]

| Register (Abbrev): interrupt_mask_cfg[23:16]<br>Address: 0x0D<br>Type: RW<br>Default Value: 0000_0000 |                      |   |          |                |               |                |               |
|---|----------------------|---|----------|----------------|---------------|----------------|---------------|
| 7   | 6                    | 5   | 4        | 3              | 2             | 1              | 0             |
| rd_eeeprom_done_mask  | rd_eeeprom_err_mask  | reserved  | reserved | ami2_viol_mask | ami2_los_mask | ami1_viol_mask | ami1_los_mask |
| Bit   | Name                 | Description   |          |                |               |                | Def. Value    |
| 7   | rd_eeeprom_done_mask | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |                |               |                | 0             |
| 6   | rd_eeeprom_err_mask  | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |                |               |                | 0             |
| 5   | reserved             | reserved  |          |                |               |                | 0000_00       |
| 4   | reserved             | reserved  |          |                |               |                | 0000_00       |
| 3   | ami2_viol_mask       | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |                |               |                | 0             |
| 2   | ami2_los_mask        | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |                |               |                | 0             |
| 1   | ami1_viol_mask       | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |                |               |                | 0             |
| 0   | ami1_los_mask        | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |                |               |                | 0             |

### Interrupt Mask Configuration Register [31:24]

| Register (Abbrev): interrupt_mask_cfg[31:24]<br>Address: 0x0E<br>Type: RW<br>Default Value: 0000_0000 |                            |   |          |          |          |                           |                            |
|---|----------------------------|---|----------|----------|----------|---------------------------|----------------------------|
| 7   | 6                          | 5   | 4        | 3        | 2        | 1                         | 0                          |
| dpll1_operating_mode_mask   | dpll1_main_ref_failed_mask | dpll1_ex_sync_alarm_mask  | reserved | reserved | reserved | dpll2_operating_mode_mask | dpll2_main_ref_failed_mask |
| Bit   | Name                       | Description   |          |          |          |                           | Def. Value                 |
| 7   | dpll1_operating_mode_mask  | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |          |          |                           | 0                          |
| 6   | dpll1_main_ref_failed_mask | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |          |          |                           | 0                          |
| 5   | dpll1_ex_sync_alarm_mask   | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |          |          |                           | 0                          |
| 4   | reserved                   | reserved  |          |          |          |                           | 0                          |
| 3   | reserved                   | reserved  |          |          |          |                           | 0                          |
| 2   | reserved                   | reserved  |          |          |          |                           | 0                          |
| 1   | dpll2_operating_mode_mask  | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |          |          |                           | 0                          |
| 0   | dpll2_main_ref_failed_mask | 0: Mask the corresponding interrupt source; no interrupt by this source<br>1: The corresponding interrupt source can generate interrupt |          |          |          |                           | 0                          |

### I2C Slave Address Configuration Register

| Register (Abbrev): i2c_slave_addr_cfg<br>Address: 0x0F<br>Type: RW<br>Default Value: 0101_0xxx |                     |  |   |   |   |   |   |
|--|---------------------|--|---|---|---|---|---|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0   |
| reserved   | I2C_slave_addr[6:0] |  |   |   |   |   |   |
| Bit  | Name                | Description  |   |   |   |   | Def. Value  |
| 7  | reserved            | reserved   |   |   |   |   | 0   |
| 6:3  | I2C_slave_addr[6:3] | Upper 4 bits of the 7-bit I2C address. This field can also be written from the CPU, and the I2C device address will change for the next I2C access.<br>Note: There are no hardware restrictions on this field; the user is responsible for using an address that complies with the I2C standards.    |   |   |   |   | 1010  |
| 2:0  | I2C_slave_addr[2:0] | Lower 3 bits of the 7-bit I2C address. This register can also be written from the CPU, and the I2C device address will change for the next I2C access.<br>Note: There are no hardware restrictions on this field; the user is responsible for using an address that complies with the I2C standards. |   |   |   |   | Determined by I2C_AD[2:0] pins during reset or EEPROM |

## 4.2 Configuration Registers

For 82P337xx I/O Mapping, see section 8 82P337xx I/O Mapping

### Input {1:2} Configuration Register

| Register (Abbrev): in{1:2}_cnfg<br>Address: 0x11, 0x12<br>Type: RW<br>Default Value: 0000_0000 |                        |  |   |                   |   |   |            |
|--|------------------------|--|---|-------------------|---|---|------------|
| 7  | 6                      | 5  | 4 | 3                 | 2 | 1 | 0          |
| reserved   | in{1:2}_400hz_sel      | in{1:2}_bucket_id[1:0]   |   | in{1:2}_freq[3:0] |   |   |            |
| Bit  | Name                   | Description  |   |                   |   |   | Def. Value |
| 7  | reserved               | reserved   |   |                   |   |   | 0          |
| 6  | in{1:2}_400hz_sel      | 400 Hz select<br>0: 64+8 kHz<br>1: 64+8+0.4 kHz  |   |                   |   |   | 0          |
| 5:4  | in{1:2}_bucket_id[1:0] | 00: Activity monitor use leak bucket configuration 0<br>01: Activity monitor use leak bucket configuration 1<br>10: Activity monitor use leak bucket configuration 2<br>11: Activity monitor use leak bucket configuration 3 |   |                   |   |   | 00         |
| 3:0  | in{1:2}_freq[3:0]      | Always 0000; 8kHz  |   |                   |   |   | 0000       |

### Input {3:14} Configuration Register

| Register (Abbrev): in{3:14}_cnfg<br>Address: 0x13–0x1E<br>Type: RW<br>Default Value: 0000_1110 |                         |  |   |                    |   |   |            |
|--|-------------------------|--|---|--------------------|---|---|------------|
| 7  | 6                       | 5  | 4 | 3                  | 2 | 1 | 0          |
| in{3:14}_direct_div  | in{3:14}_lock_8k        | in{3:14}_bucket_id[1:0]  |   | in{3:14}_freq[3:0] |   |   |            |
| Bit  | Name                    | Description  |   |                    |   |   | Def. Value |
| 7  | in{3:14}_direct_div     | 0: Input goes directly to DPLL and Monitor<br>1: Input goes to DPLL and monitor after pre-divider  |   |                    |   |   | 0          |
| 6  | in{3:14}_lock_8k        | 0: Input goes directly to DPLL<br>1: Input goes to DPLL after pre-divider<br>If both direct_div and lock_8k are set to 1, lock_8k takes higher priority  |   |                    |   |   | 0          |
| 5:4  | in{3:14}_bucket_id[1:0] | 00: Input activity monitor use leak bucket configuration 0<br>01: Input activity monitor use leak bucket configuration 1<br>10: Input activity monitor use leak bucket configuration 2<br>11: Input activity monitor use leak bucket configuration 3 |   |                    |   |   | 00         |

### Input {3:14} Configuration Register

|  |                    |   |   |   |   |   |  |
|--|--------------------|---|---|---|---|---|--|
| Register (Abbrev): in{3:14}_cnfg<br>Address: 0x13-0x1E<br>Type: RW<br>Default Value: 0000_1110 |                    |   |   |   |   |   |  |
| 7  | 6                  | 5 | 4   | 3 | 2 | 1 | 0  |
| 3:0  | in{3:14}_freq[3:0] |   | 0000: 8 kHz only<br>0001: 1.544 MHz/2.048 MHz (depends on SONET/SDH mode)<br>0010: 6.48 MHz<br>0011: 19.44 MHz.<br>0100: 25.92 MHz<br>0101: 38.88 MHz<br>1001: 2 kHz<br>1010: 4 kHz<br>1011: 1 PPS<br>1100: 6.25 MHz<br>1110: 25 MHz<br>Others: reserved (do not use)<br>Note: Must be set to 8 kHz if going to DPLL2 |   |   |   | IN{3:4} -> 1110<br>IN{5:10} -> 0011<br>IN{11:14} -> 0001 |

### High Frequency Divider Configuration Register [7:0]

| Register (Abbrev): hf_div_cnfg[7:0]<br>Address: 0x1F<br>Type: RW<br>Default Value: 0000_0000 |                 |   |   |                 |   |                 |   |
|--|-----------------|---|---|-----------------|---|-----------------|---|
| 7  | 6               | 5   | 4 | 3               | 2 | 1               | 0 |
| in6_hf_div[1:0]  |                 | in5_hf_div[1:0]   |   | in4_hf_div[1:0] |   | in3_hf_div[1:0] |   |
| Bit  | Name            | Description   |   |                 |   | Def. Value      |   |
| 7:6  | in6_hf_div[1:0] | These bits determine whether the HF Divider is used and what the division factor is for input frequency division.<br>00: Bypassed<br>01: Divided by 4<br>10: Divided by 5<br>11: Reserved |   |                 |   | 00              |   |
| 5:4  | in5_hf_div[1:0] | These bits determine whether the HF Divider is used and what the division factor is for input frequency division.<br>00: Bypassed<br>01: Divided by 4<br>10: Divided by 5<br>11: Reserved |   |                 |   | 00              |   |
| 3:2  | in4_hf_div[1:0] | These bits determine whether the HF Divider is used and what the division factor is for input frequency division.<br>00: Bypassed<br>01: Divided by 4<br>10: Divided by 5<br>11: Reserved |   |                 |   | 00              |   |

### High Frequency Divider Configuration Register [7:0]

|  |                 |   |   |   |   |   |    |
|--|-----------------|---|---|---|---|---|----|
| Register (Abbrev): hf_div_cnfg[7:0]<br>Address: 0x1F<br>Type: RW<br>Default Value: 0000_0000 |                 |   |   |   |   |   |    |
| 7  | 6               | 5 | 4   | 3 | 2 | 1 | 0  |
| 1:0  | in3_hf_div[1:0] |   | These bits determine whether the HF Divider is used and what the division factor is for input frequency division.<br>00: Bypassed<br>01: Divided by 4<br>10: Divided by 5<br>11: Reserved |   |   |   | 00 |

### High Frequency Divider Configuration Register [11:8]

| Register (Abbrev): hf_div_cnfg[11:8]<br>Address: 0x20<br>Type: RW<br>Default Value: 0000_0000 |                 |   |   |                 |   |                 |            |
|---|-----------------|---|---|-----------------|---|-----------------|------------|
| 7   | 6               | 5   | 4 | 3               | 2 | 1               | 0          |
| reserved  |                 |   |   | in8_hf_div[1:0] |   | in7_hf_div[1:0] |            |
| Bit   | Name            | Description   |   |                 |   |                 | Def. Value |
| 7:4   | reserved        | reserved  |   |                 |   |                 | 0000       |
| 3:2   | in8_hf_div[1:0] | These bits determine whether the HF Divider is used and what the division factor is for input frequency division.<br>00: Bypassed<br>01: Divided by 4<br>10: Divided by 5<br>11: Reserved |   |                 |   |                 | 00         |
| 1:0   | in7_hf_div[1:0] | These bits determine whether the HF Divider is used and what the division factor is for input frequency division.<br>00: Bypassed<br>01: Divided by 4<br>10: Divided by 5<br>11: Reserved |   |                 |   |                 | 00         |

### Input Power-Down Configuration Register

|   |   |   |   |   |   |          |           |
|---|---|---|---|---|---|----------|-----------|
| Register (Abbrev): in_pdn_cnfg<br>Address: 0x21<br>Type: RW<br>Default Value: 0000_0000 |   |   |   |   |   |          |           |
| 7   | 6 | 5 | 4 | 3 | 2 | 1        | 0         |
| in[8:3]_pdn   |   |   |   |   |   | reserved | in1+2_pdn |



### Input Power-Down Configuration Register

| Register (Abbrev): in_pdn_cnfg<br>Address: 0x21<br>Type: RW<br>Default Value: 0000_0000 |             |   |   |   |   |   |            |
|---|-------------|---|---|---|---|---|------------|
| 7   | 6           | 5   | 4 | 3 | 2 | 1 | 0          |
| Bit   | Name        | Description   |   |   |   |   | Def. Value |
| 7:2   | in[8:3]_pdn | Input power down bits.<br>0: Not powered down (active/enabled)<br>1: Input powered down (inactive/disabled) |   |   |   |   | 0          |
| 1   | reserved    | reserved  |   |   |   |   | 0          |
| 0   | in1+2_pdn   | Input power down bits.<br>0: Not powered down (active/enabled)<br>1: Input powered down (inactive/disabled) |   |   |   |   | 0          |

### Input {3:14} FEC Divider Numerator P Register [15:0]

| Register (Abbrev): in{3:14}_fec_divp_cnfg[15:0]<br>Address: 0x2C, 0x32, 0x38, 0x3E, 0x44, 0x4A, 0x50, 0x56, 0x5C, 0x62, 0x68, 0x6E, 0x2D, 0x33, 0x39, 0x3F, 0x45, 0x4B, 0x51, 0x57, 0x5D, 0x63, 0x69, 0x6F<br>Type: RW<br>Default Value: 0000_0000 |                              |  |   |   |   |   |            |
|--|------------------------------|--|---|---|---|---|------------|
| 7  | 6                            | 5  | 4 | 3 | 2 | 1 | 0          |
| in{3:14}_fec_divp_cnfg[7:0]  |                              |  |   |   |   |   |            |
| in{3:14}_fec_divp_cnfg[15:8]   |                              |  |   |   |   |   |            |
| Bit  | Name                         | Description  |   |   |   |   | Def. Value |
| 7:0  | in{3:14}_fec_divp_cnfg[7:0]  | This field represents the value of the numerator of FEC divider. The numerator must be smaller than or equal to the denominator.<br>$\text{Freq\_out} = \text{fec\_divp\_cnfg} / \text{fec\_divq\_cnfg} * \text{Freq\_in}$ |   |   |   |   | 0000_0000  |
|  | in{3:14}_fec_divp_cnfg[15:8] |  |   |   |   |   |            |

### Input {3:14} FEC Divider Denominator Q Register [15:0]

| Register (Abbrev): in{3:14}_fec_divq_cnfg[15:0]<br>Address: 0x2E, 0x34, 0x3A, 0x40, 0x46, 0x4C, 0x52, 0x58, 0x5E, 0x64, 0x6A, 0x70, 0x2F, 0x35, 0x3B, 0x41, 0x47, 0x4D, 0x53, 0x59, 0x5F, 0x65, 0x6B, 0x71<br>Type: RW<br>Default Value: 0000_0000 |                              |  |   |   |   |   |            |
|--|------------------------------|--|---|---|---|---|------------|
| 7  | 6                            | 5  | 4 | 3 | 2 | 1 | 0          |
| in{3:14}_fec_divq_cnfg[7:0]  |                              |  |   |   |   |   |            |
| in{3:14}_fec_divq_cnfg[15:8]   |                              |  |   |   |   |   |            |
| Bit  | Name                         | Description  |   |   |   |   | Def. Value |
| 7:0  | in{3:14}_fec_divq_cnfg[7:0]  | This field represents the value of the denominator of FEC divider. The numerator must be smaller than or equal to the denominator.<br>$\text{Freq\_out} = \text{fec\_divp\_cnfg} / \text{fec\_divq\_cnfg} * \text{Freq\_in}$ |   |   |   |   | 0000_0000  |
|  | in{3:14}_fec_divq_cnfg[15:8] |  |   |   |   |   |            |

Input {3:14} Pre-divider Denominator N Register [14:0]

| Register (Abbrev): in{3:14}_pre_divn_cfg[7:0]<br>Address: 0x30, 0x36, 0x3C, 0x42, 0x48, 0x4E, 0x54, 0x5A, 0x60, 0x66, 0x6C, 0x72<br>0x31, 0x37, 0x3D, 0x43, 0x49, 0x4F, 0x55, 0x5B, 0x61, 0x67, 0x6D, 0x73<br>Type: RW<br>Default Value: 0000_0000 |                             |   |   |   |   |   |            |
|--|-----------------------------|---|---|---|---|---|------------|
| 7  | 6                           | 5   | 4 | 3 | 2 | 1 | 0          |
| in{3:14}_pre_divn_cfg[7:0]   |                             |   |   |   |   |   |            |
| reserved   | in{3:14}_pre_divn_cfg[14:8] |   |   |   |   |   |            |
| Bit  | Name                        | Description   |   |   |   |   | Def. Value |
| 7:0  | in{3:14}_pre_divn_cfg[7:0]  | This field represents the value by which to divide inputs that use the Pre_divider.<br>The input frequency will be divided by the value in this register plus 1 (for example, to divide 16, program a value of 15). |   |   |   |   | 0000_0000  |
| 7  | reserved                    | reserved  |   |   |   |   | 0          |
| 6:0  | in{3:14}_pre_divn_cfg[14:8] | This field represents the value by which to divide inputs that use the Pre_divider.<br>The input frequency will be divided by the value in this register plus 1 (for example, to divide 16, program a value of 15). |   |   |   |   | 000_0000   |

Page Register

| Register (Abbrev): page_reg<br>Address: 0x7F, 0xFF, 0x17F, 0x1FF, 0x27F, 0x2FF, 0x37F, 0x3FF<br>Type: RW<br>Default Value: 0000_0000 |           |  |   |   |           |   |            |
|--|-----------|--|---|---|-----------|---|------------|
| 7  | 6         | 5  | 4 | 3 | 2         | 1 | 0          |
| reserved   |           |  |   |   | page[2:0] |   |            |
| Bit  | Name      | Description  |   |   |           |   | Def. Value |
| 7:3  | reserved  | reserved   |   |   |           |   | 0000_0     |
| 2:0  | page[2:0] | This register contains the pointer to the page of memory to be written or read in the next register access.<br>This register is mapped onto every page of memory at No. 127, and therefore appears at the extended addresses x07F, x0FF, x17F, x1FF, x27F, x2FF, x37F and x3FF. If the external EEPROM is used, these memory-map addresses must contain the value of the next page (that is, x07F = x01, x0FF = x02, x17F = x03, ..., x37F = x07). |   |   |           |   | 000        |

### 4.3 Reference Monitor Registers

#### Frequency Monitor Factor Configuration Register

| Register (Abbrev): freq_mon_factor_cfg<br>Address: 0x80<br>Type: RW<br>Default Value: 0000_1011 |                          |  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
|---|--------------------------|--|---|----------------------|---|---|-----------------|--------------------------|-----------------|------|---|--------|------|---|--------|------|---|--------|------|---|--------|------|----|--------|------|----|-------|------|----|-------|------|-----|-------|------|-----|-------|------|-----|-------|------|------|-------|------|------|------|-----------|------|------|------|
| 7   | 6                        | 5  | 4 | 3                    | 2 | 1 | 0               |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| freq_mon_clk_sel  | in_noise_window          | reserved   |   | freq_mon_factor[3:0] |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| Bit   | Name                     | Description  |   |                      |   |   | Def. Value      |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 7   | freq_mon_clk_sel         | This bit selects the source of the clock to the frequency monitors, the AMI codecs, and the MPIO and CSRs.<br>0: Free-running clock that tracks crystal oscillator frequency<br>1: Clock that tracks output of dpll1   |   |                      |   |   | 0               |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 6   | in_noise_window          | For 1 PPS, 2 kHz, 4kHz, and 8kHz input, this bit determines whether the input clock whose edge respect to the reference clock is outside $\pm 5\%$ is enabled to be selected for DPLL.<br>0: Disabled<br>1: Enabled  |   |                      |   |   | 0               |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 5:4   | reserved                 | reserved   |   |                      |   |   | 00              |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 3:0   | freq_mon_factor[3:0]     | These bits determine the number of extra or missing edges by which a 16 second count of the number of input clock edges deviates from the nominal. The conversion of the count to ppm depends on the frequency of the clock. Shown is the conversion from count to ppm for a 19.44MHz clock.<br>The count is multiplied by the accept/reject thresholds in the <a href="#">Hard Frequency Monitor Threshold Configuration Register</a> and the <a href="#">Soft Frequency Monitor Threshold Configuration Register</a> to convert to them to ppm.<br><table border="1"> <thead> <tr> <th>freq_mon_factor</th> <th>Missing/Extra Edge count</th> <th>ppm at 19.44MHz</th> </tr> </thead> <tbody> <tr><td>0000</td><td>1</td><td>0.0032</td></tr> <tr><td>0001</td><td>2</td><td>0.0064</td></tr> <tr><td>0010</td><td>4</td><td>0.0129</td></tr> <tr><td>0011</td><td>8</td><td>0.0257</td></tr> <tr><td>0100</td><td>16</td><td>0.0514</td></tr> <tr><td>0101</td><td>32</td><td>0.103</td></tr> <tr><td>0110</td><td>64</td><td>0.206</td></tr> <tr><td>0111</td><td>128</td><td>0.412</td></tr> <tr><td>1000</td><td>256</td><td>0.823</td></tr> <tr><td>1001</td><td>512</td><td>1.646</td></tr> <tr><td>1010</td><td>1024</td><td>3.292</td></tr> <tr><td>1011</td><td>1184</td><td>3.81</td></tr> <tr><td>1100–1111</td><td>1430</td><td>4.60</td></tr> </tbody> </table> |   |                      |   |   | freq_mon_factor | Missing/Extra Edge count | ppm at 19.44MHz | 0000 | 1 | 0.0032 | 0001 | 2 | 0.0064 | 0010 | 4 | 0.0129 | 0011 | 8 | 0.0257 | 0100 | 16 | 0.0514 | 0101 | 32 | 0.103 | 0110 | 64 | 0.206 | 0111 | 128 | 0.412 | 1000 | 256 | 0.823 | 1001 | 512 | 1.646 | 1010 | 1024 | 3.292 | 1011 | 1184 | 3.81 | 1100–1111 | 1430 | 4.60 | 1011 |
| freq_mon_factor   | Missing/Extra Edge count | ppm at 19.44MHz  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0000  | 1                        | 0.0032   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0001  | 2                        | 0.0064   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0010  | 4                        | 0.0129   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0011  | 8                        | 0.0257   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0100  | 16                       | 0.0514   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0101  | 32                       | 0.103  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0110  | 64                       | 0.206  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 0111  | 128                      | 0.412  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 1000  | 256                      | 0.823  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 1001  | 512                      | 1.646  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 1010  | 1024                     | 3.292  |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 1011  | 1184                     | 3.81   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |
| 1100–1111   | 1430                     | 4.60   |   |                      |   |   |                 |                          |                 |      |   |        |      |   |        |      |   |        |      |   |        |      |    |        |      |    |       |      |    |       |      |     |       |      |     |       |      |     |       |      |      |       |      |      |      |           |      |      |      |

### Hard Frequency Monitor Threshold Configuration Register

| Register (Abbrev): hard_freq_mon_threshold_cfg<br>Address: 0x81<br>Type: RW<br>Default Value: 0010_0011 |                            |   |   |                            |   |   |            |
|---|----------------------------|---|---|----------------------------|---|---|------------|
| 7   | 6                          | 5   | 4 | 3                          | 2 | 1 | 0          |
| hard_accept_threshold[3:0]  |                            |   |   | hard_reject_threshold[3:0] |   |   |            |
| Bit   | Name                       | Description   |   |                            |   |   | Def. Value |
| 7:4   | hard_accept_threshold[3:0] | Accepting threshold of reference clock monitoring.<br>To calculate the limit in ppm, add one to the 4-bit value in the register and multiply by freq_mon_factor in the <a href="#">Frequency Monitor Factor Configuration Register</a> (default 3.81 ppm). The limit is symmetrical about zero. A value of 0010 (3) corresponds to an alarm limit of +/-11.43 ppm.  |   |                            |   |   | 0010       |
| 3:0   | hard_reject_threshold[3:0] | Rejection threshold of reference clocks monitoring.<br>To calculate the limit in ppm, add one to the 4-bit value in the register and multiply by freq_mon_factor in the <a href="#">Frequency Monitor Factor Configuration Register</a> (default 3.81 ppm). The limit is symmetrical about zero. A value of 0011 (3) corresponds to an alarm limit of +/-15.24 ppm. |   |                            |   |   | 0011       |

### Soft Frequency Monitor Threshold Configuration Register

| Register (Abbrev): soft_freq_mon_threshold_cfg<br>Address: 0x82, Type: RW<br>Default Value: 0010_0011 |                            |   |   |                            |   |   |            |
|---|----------------------------|---|---|----------------------------|---|---|------------|
| 7   | 6                          | 5   | 4 | 3                          | 2 | 1 | 0          |
| soft_accept_threshold[3:0]  |                            |   |   | soft_reject_threshold[3:0] |   |   |            |
| Bit   | Name                       | Description   |   |                            |   |   | Def. Value |
| 7:4   | soft_accept_threshold[3:0] | Accepting threshold of reference clock monitoring.<br>To calculate the limit in ppm, add one to the 4-bit value in the register and multiply by freq_mon_factor in the <a href="#">Frequency Monitor Factor Configuration Register</a> (default 3.81 ppm). The limit is symmetrical about zero. A value of 0010 (2) corresponds to an alarm limit of +/-11.43 ppm.  |   |                            |   |   | 0010       |
| 3:0   | soft_reject_threshold[3:0] | Rejection threshold of reference clocks monitoring<br>To calculate the limit in ppm, add one to the 4-bit value in the register, and multiply by freq_mon_factor in the <a href="#">Frequency Monitor Factor Configuration Register</a> (default 3.81 ppm). The limit is symmetrical about zero. A value of 0011 (3) corresponds to an alarm limit of +/-15.24 ppm. |   |                            |   |   | 0011       |

### Upper Threshold {0:3} Configuration Register

| Register (Abbrev): upper_threshold_{0:3}_cnfg<br>Address: 0x83, 0x87, 0x8B, 0x8F<br>Type: RW<br>Default Value: 0000_0110 |                                 |  |   |   |   |   |   |            |
|--|---------------------------------|--|---|---|---|---|---|------------|
| 7  | 6                               | 5  | 4 | 3 | 2 | 1 | 0 |            |
| upper_threshold_{0:3}_cnfg[7:0]  |                                 |  |   |   |   |   |   |            |
| Bit  | Name                            | Description  |   |   |   |   |   | Def. Value |
| 7  | upper_threshold_{0:3}_cnfg[7:0] | These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold (6), a no-activity alarm is raised. |   |   |   |   |   | 0000_0110  |

### Lower Threshold {0:3} Configuration Register

| Register (Abbrev): lower_threshold_{0:3}_cnfg<br>Address: 0x84, 0x88, 0x8C, 0x90<br>Type: RW<br>Default Value: 0000_0100 |                                 |  |   |   |   |   |   |            |
|--|---------------------------------|--|---|---|---|---|---|------------|
| 7  | 6                               | 5  | 4 | 3 | 2 | 1 | 0 |            |
| lower_threshold_{0:3}_cnfg[7:0]  |                                 |  |   |   |   |   |   |            |
| Bit  | Name                            | Description  |   |   |   |   |   | Def. Value |
| 7  | lower_threshold_{0:3}_cnfg[7:0] | These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold (4), the no-activity alarm is cleared. |   |   |   |   |   | 0000_0100  |

### Bucket Size {0:3} Configuration Register

| Register (Abbrev): bucket_size_{0:3}_cnfg<br>Address: 0x85, 0x89, 0x8D, 0x91<br>Type: RW<br>Default Value: 0000_1000 |                             |  |   |   |   |   |   |            |
|--|-----------------------------|--|---|---|---|---|---|------------|
| 7  | 6                           | 5  | 4 | 3 | 2 | 1 | 0 |            |
| bucket_size_{0:3}_cnfg[7:0]  |                             |  |   |   |   |   |   |            |
| Bit  | Name                        | Description  |   |   |   |   |   | Def. Value |
| 7:0  | bucket_size_{0:3}_cnfg[7:0] | These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reaches the bucket size (8), the accumulator will stop increasing even if further events are detected. |   |   |   |   |   | 0000_1000  |

### Decay Rate {0:3} Configuration Register

| Register (Abbrev): decay_rate_{0:3}_cnfg<br>Address: 0x86, 0x8A, 0x8E, 0x92<br>Type: RW<br>Default Value: 0000_0001 |                            |   |   |   |   |                            |            |
|---|----------------------------|---|---|---|---|----------------------------|------------|
| 7   | 6                          | 5   | 4 | 3 | 2 | 1                          | 0          |
| reserved  |                            |   |   |   |   | decay_rate_{0:3}_cnfg[1:0] |            |
| Bit   | Name                       | Description   |   |   |   |                            | Def. Value |
| 7:2   | reserved                   | reserved  |   |   |   |                            | 0000_00    |
| 1:0   | decay_rate_{0:3}_cnfg[1:0] | These bits set a decay rate for the internal leaky bucket accumulator:<br>00: The accumulator decreases by 1 every 128 ms with no event detected.<br>01: The accumulator decreases by 1 every 256 ms with no event detected.<br>10: The accumulator decreases by 1 every 512 ms with no event detected.<br>11: The accumulator decreases by 1 every 1024 ms with no event detected. |   |   |   |                            | 01         |

### Input {1:14} Frequency Read Status Register

| Register (Abbrev): in{1:14}_freq_read_sts<br>Address: 0x93, 0x94, 0x95, 0x96, 0x97, 0x98, 0x99, 0x9A, 0x9B, 0x9C, 0x9D, 0x9E, 0x9F, 0xA0<br>Type: RO<br>Default Value: 0000_0000 |                          |   |   |   |   |   |            |
|--|--------------------------|---|---|---|---|---|------------|
| 7  | 6                        | 5   | 4 | 3 | 2 | 1 | 0          |
| in{1:14}_freq_value[7:0]   |                          |   |   |   |   |   |            |
| Bit  | Name                     | Description   |   |   |   |   | Def. Value |
| 7:0  | in{1:14}_freq_value[7:0] | This is 8-bit 2's complement signed integer. To calculate the offset in ppm of the selected input, the value should be multiplied by freq_mon_factor in the <a href="#">Frequency Monitor Factor Configuration Register</a> (default 3.81 ppm). |   |   |   |   | 0000_0000  |

### Remote Input Valid Configuration Register [8:1]

| Register (Abbrev): remote_input_valid_cnfg[8:1]<br>Address: 0xA1<br>Type: RW<br>Default Value: 1111_1111 |                        |   |   |   |   |   |            |
|--|------------------------|---|---|---|---|---|------------|
| 7  | 6                      | 5   | 4 | 3 | 2 | 1 | 0          |
| remote_in[8:1]_valid   |                        |   |   |   |   |   |            |
| Bit  | Name                   | Description   |   |   |   |   | Def. Value |
| 7:0  | remote_in[8:1]_invalid | 0: The corresponding input is allowed.<br>1: The corresponding input is disallowed. |   |   |   |   | 1          |

### Remote Input Valid Configuration Register [14:9]

| Register (Abbrev): remote_input_valid_cfg[14:9]<br>Address: 0xA2<br>Type: RW<br>Default Value: 0011_1111 |                         |   |   |   |   |   |            |
|--|-------------------------|---|---|---|---|---|------------|
| 7  | 6                       | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved   |                         | remote_in[14:9]_valid   |   |   |   |   |            |
| Bit  | Name                    | Description   |   |   |   |   | Def. Value |
| 7:6  | reserved                | reserved  |   |   |   |   | 00         |
| 5:0  | remote_in[14:9]_invalid | 0: The corresponding input is allowed.<br>1: The corresponding input is disallowed. |   |   |   |   | 1          |

### Phase Alarm Time Configuration Register

| Register (Abbrev): phase_alarm_time_cfg<br>Address: 0xA3<br>Type: RW<br>Default Value: 0011_0010 |                                 |   |   |   |   |   |            |
|--|---------------------------------|---|---|---|---|---|------------|
| 7  | 6                               | 5   | 4 | 3 | 2 | 1 | 0          |
| phase_alarm_multi_factor[1:0]  |                                 | phase_alarm_time_out_value[5:0]   |   |   |   |   |            |
| Bit  | Name                            | Description   |   |   |   |   | Def. Value |
| 7:6  | phase_alarm_multi_factor[1:0]   | 00: 2<br>01: 4<br>10: 8<br>11: 16   |   |   |   |   | 00         |
| 5:0  | phase_alarm_time_out_value[5:0] | This unsigned 6-bit integer represents the length of time before phase alarm (unlock) will be raised on an input.<br>This time value is the time that the state machine will spend in pre-locked, pre-locked2, or lost-phase modes before setting the phase alarm on the selected input.<br>phase_alarm_multi_factor * phase_alarm_time_out_value= xxx Second |   |   |   |   | 11_0010    |

### Loss of Signal Status Register

| Register (Abbrev): los_sts<br>Address: 0xA4<br>Type: RO<br>Default Value: 0000_0000 |                  |                                |   |          |   |   |                             |
|---|------------------|--------------------------------|---|----------|---|---|-----------------------------|
| 7   | 6                | 5                              | 4 | 3        | 2 | 1 | 0                           |
| los_pin_sts[3:0]  |                  |                                |   | reserved |   |   |                             |
| Bit   | Name             | Description                    |   |          |   |   | Def. Value                  |
| 7:4   | los_pin_sts[3:0] | Represents los_pin[3:0] status |   |          |   |   | Determined by LOS[3:0] pins |
| 3:0   | reserved         | reserved                       |   |          |   |   | 0000                        |

### Input {1:14} Status Register

| Register (Abbrev): in{1:14}_sts<br>Address: 0xA5, 0xA6, 0xA7, 0xA8, 0xA9, 0xAA, 0xAB, 0xAC, 0xAD, 0xAE, 0xAF, 0xB0, 0xB1, 0xB2<br>Type: RO<br>Default Value: 0001_0100 |                                |  |                          |                          |                         |          |                                |
|--|--------------------------------|--|--------------------------|--------------------------|-------------------------|----------|--------------------------------|
| 7  | 6                              | 5  | 4                        | 3                        | 2                       | 1        | 0                              |
| reserved   | in{1:14}_valid_dp11            | in{1:14}_valid_dp12  | in{1:14}_freq_hard_alarm | in{1:14}_freq_soft_alarm | in{1:14}_activity_alarm | reserved | in{1:14}_phase_lock_alarm_dp11 |
| Bit  | Name                           | Description  |                          |                          |                         |          | Def. Value                     |
| 7  | reserved                       | reserved   |                          |                          |                         |          | 0                              |
| 6  | in{1:14}_valid_dp11            | Indicates if reference is valid for dp11.<br>0: Invalid<br>1: Valid    |                          |                          |                         |          | 0                              |
| 5  | in{1:14}_valid_dp12            | Indicates if reference is valid for dp12.<br>0: Invalid<br>1: Valid    |                          |                          |                         |          | 0                              |
| 4  | in{1:14}_freq_hard_alarm       | 0: No alarm.<br>1: The corresponding alarm is set.                     |                          |                          |                         |          | 1                              |
| 3  | in{1:14}_freq_soft_alarm       | 0: No alarm.<br>1: The corresponding alarm is set.                     |                          |                          |                         |          | 0                              |
| 2  | in{1:14}_activity_alarm        | 0: No alarm.<br>1: The corresponding alarm is set.                     |                          |                          |                         |          | 1                              |
| 1  | reserved                       | reserved   |                          |                          |                         |          | 0                              |
| 0  | in{1:14}_phase_lock_alarm_dp11 | Indicates phase lock alarm for dp11<br>0: No alarm<br>1: Alarm is set. |                          |                          |                         |          | 0                              |

### Input {1:2} LOS Sync Configuration Register

| Register (Abbrev): in{1:2}_los_sync_cfg<br>Address: 0xB3, 0xB4<br>Type: RW<br>Default Value: 0000_0000 |                |  |   |          |   |   |            |
|--|----------------|--|---|----------|---|---|------------|
| 7  | 6              | 5  | 4 | 3        | 2 | 1 | 0          |
| reserved   | in{1:2}_los_en | in{1:2}_los_sel[1:0]   |   | reserved |   |   |            |
| Bit  | Name           | Description  |   |          |   |   | Def. Value |
| 7  | reserved       | reserved   |   |          |   |   | 0          |
| 6  | in{1:2}_los_en | 0: No LOS pin associated with the input<br>1: Selected LOS pin associated with the input |   |          |   |   | 0          |



### Input {1:2} LOS Sync Configuration Register

|   |                      |   |  |   |   |   |      |
|---|----------------------|---|--|---|---|---|------|
| Register (Abbrev): in{1:2}_los_sync_cnfg<br>Address: 0xB3, 0xB4<br>Type: RW<br>Default Value: 0000_0000 |                      |   |  |   |   |   |      |
| 7   | 6                    | 5 | 4  | 3 | 2 | 1 | 0    |
| 5:4   | in{1:2}_los_sel[1:0] |   | 00: LOS0 pin<br>01: LOS1 pin<br>10: LOS2 pin<br>11: LOS3 pin |   |   |   | 00   |
| 3:0   | reserved             |   | reserved   |   |   |   | 0000 |

### Input {3:14} LOS Sync Configuration Register

| Register (Abbrev): in{3:14}_los_sync_cnfg<br>Address: 0xB5, 0xB6, 0xB7, 0xB8, 0xB9, 0xBA, 0xBB, 0xBC, 0xBD, 0xBE, 0xBF, 0xC0<br>Type: RW<br>Default Value: 0000_0000 |                        |   |   |                        |   |   |            |
|--|------------------------|---|---|------------------------|---|---|------------|
| 7  | 6                      | 5   | 4 | 3                      | 2 | 1 | 0          |
| reserved   | in{3:14}_los_en        | in{3:14}_los_sel[1:0]   |   | in{3:14}_sync_sel[3:0] |   |   |            |
| Bit  | Name                   | Description   |   |                        |   |   | Def. Value |
| 7  | reserved               | reserved  |   |                        |   |   | 0          |
| 6  | in{3:14}_los_en        | 0: No LOS pin associated with the input<br>1: Selected LOS pin associated with the input  |   |                        |   |   | 0          |
| 5:4  | in{3:14}_los_sel[1:0]  | 00: LOS0 pin<br>01: LOS1 pin<br>10: LOS2 pin<br>11: LOS3 pin  |   |                        |   |   | 00         |
| 3:0  | in{3:14}_sync_sel[3:0] | Specifies which input is used as a sync when this input is selected as a clock input.<br>0000: Reserved<br>0001: IN1 used as sync<br>...<br>1110: IN14 used as sync<br>1111: Reserved<br>The frequency of the SYNC must be specified in the <a href="#">dpll1 Input Mode Configuration Register</a> . |   |                        |   |   | 0000       |

### Input 4-1 Sync Phase Configuration Register

| Register (Abbrev): in{1:4}_sync_phase_cfg<br>Address: 0xC1<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |                     |   |                     |   |
|--|---------------------|--|---|---------------------|---|---------------------|---|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1                   | 0 |
| in4_sync_phase[1:0]  |                     | in3_sync_phase[1:0]  |   | in2_sync_phase[1:0] |   | in1_sync_phase[1:0] |   |
| Bit  | Name                | Description  |   |                     |   | Def. Value          |   |
| 7:6  | in4_sync_phase[1:0] | These bits set the sampling of the selected SYNC input to synchronize the frame sync output signal. Nominally, the falling edge of SYNC is aligned with the rising edge of the DPLL selected input clock.<br>00: On target<br>01: 0.5 UI early<br>10: 1.0 UI late<br>11: 0.5 UI late |   |                     |   | 00                  |   |
| 5:4  | in3_sync_phase[1:0] | See in4_sync_phase[1:0] description.   |   |                     |   | 00                  |   |
| 3:2  | in2_sync_phase[1:0] | See in4_sync_phase[1:0] description.   |   |                     |   | 00                  |   |
| 1:0  | in1_sync_phase[1:0] | See in4_sync_phase[1:0] description.   |   |                     |   | 00                  |   |

### Input 8-5 Sync Phase Configuration Register

| Register (Abbrev): in8-5_sync_phase_cfg<br>Address: 0xC2<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |                     |   |                     |   |
|--|---------------------|--|---|---------------------|---|---------------------|---|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1                   | 0 |
| in8_sync_phase[1:0]  |                     | in7_sync_phase[1:0]  |   | in6_sync_phase[1:0] |   | in5_sync_phase[1:0] |   |
| Bit  | Name                | Description  |   |                     |   | Def. Value          |   |
| 7:6  | in8_sync_phase[1:0] | These bits set the sampling of the selected SYNC input to synchronize the frame sync output signal. Nominally, the falling edge of SYNC is aligned with the rising edge of the DPLL selected input clock.<br>00: On target<br>01: 0.5 UI early<br>10: 1 UI late<br>11: 0.5 UI late |   |                     |   | 00                  |   |
| 5:4  | in7_sync_phase[1:0] | See in8_sync_phase[1:0] description.   |   |                     |   | 00                  |   |
| 3:2  | in6_sync_phase[1:0] | See in8_sync_phase[1:0] description.   |   |                     |   | 00                  |   |
| 1:0  | in5_sync_phase[1:0] | See in8_sync_phase[1:0] description.   |   |                     |   | 00                  |   |

Input 12–9 Sync Phase Configuration Register

| Register (Abbrev): in12–9_sync_phase_cnfg<br>Address: 0xC3<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |                      |   |                     |            |
|--|----------------------|---|---|----------------------|---|---------------------|------------|
| 7  | 6                    | 5   | 4 | 3                    | 2 | 1                   | 0          |
| in12_sync_phase[1:0]   |                      | in11_sync_phase[1:0]  |   | in10_sync_phase[1:0] |   | in9_sync_phase[1:0] |            |
| Bit  | Name                 | Description   |   |                      |   |                     | Def. Value |
| 7:6  | in12_sync_phase[1:0] | These bits set the sampling of the selected SYNC input to synchronize the frame sync output signal. Nominally, the falling edge of YNC is aligned with the rising edge of the DPLL selected input clock.<br>00: On target.<br>01: 0.5 UI early.<br>10: 1 UI late.<br>11: 0.5 UI late. |   |                      |   |                     | 00         |
| 5:4  | in11_sync_phase[1:0] | See in12_sync_phase[1:0] description.   |   |                      |   |                     | 00         |
| 3:2  | in10_sync_phase[1:0] | See in12_sync_phase[1:0] description.   |   |                      |   |                     | 00         |
| 1:0  | in9_sync_phase[1:0]  | See in12_sync_phase[1:0] description.   |   |                      |   |                     | 00         |

Input 14–13 Sync Phase Configuration Register

| Register (Abbrev): in14–13_sync_phase_cnfg<br>Address: 0xC4<br>Type: RW<br>Default Value: 0000_0000 |                      |  |   |                      |   |                      |            |
|---|----------------------|--|---|----------------------|---|----------------------|------------|
| 7   | 6                    | 5  | 4 | 3                    | 2 | 1                    | 0          |
| reserved  |                      |  |   | in14_sync_phase[1:0] |   | in13_sync_phase[1:0] |            |
| Bit   | Name                 | Description  |   |                      |   |                      | Def. Value |
| 7:4   | reserved             | reserved   |   |                      |   |                      | 0000       |
| 3:2   | in14_sync_phase[1:0] | These bits set the sampling of the selected SYNC input to synchronize the frame sync output signal. Nominally, the falling edge of SYNC is aligned with the rising edge of the DPLL selected input clock.<br>00: On target<br>01: 0.5 UI early<br>10: 1 UI late<br>11: 0.5 UI late |   |                      |   |                      | 00         |
| 1:0   | in13_sync_phase[1:0] |  |   |                      |   |                      | 00         |

### Input {3:14} Phase Offset Configuration Register

| Register (Abbrev): in{3:14}_phase_offset_cfg<br>Address: 0xC5, 0xC6, 0xC7, 0xC8, 0xC9, 0xCA, 0xCB, 0xCC, 0xCD, 0xCE, 0xCF, 0xD0<br>Type: RW<br>Default Value: 0000_0000 |                       |   |   |   |   |   |   |            |
|---|-----------------------|---|---|---|---|---|---|------------|
| 7   | 6                     | 5   | 4 | 3 | 2 | 1 | 0 |            |
| in3_phase_offset[7:0]   |                       |   |   |   |   |   |   |            |
| Bit   | Name                  | Description   |   |   |   |   |   | Def. Value |
| 7:0   | in3_phase_offset[7:0] | Input-to-output phase offset for INx input. This offset is automatically applied when the input is selected.<br>Value is 2's complement with a resolution of 1 lsb = 0.61 ns. |   |   |   |   |   | 0000_0000  |

## 4.4 DPLL1 Registers

### dpll1 Priority Table Status Register [7:0]

| Register (Abbrev): dpll1_priority_table_sts[7:0]<br>Address: 0x100<br>Type: RO<br>Default Value: 0000_0000 |                              |   |   |                            |   |   |   |            |
|--|------------------------------|---|---|----------------------------|---|---|---|------------|
| 7  | 6                            | 5   | 4 | 3                          | 2 | 1 | 0 |            |
| dpll1_highest_valid_ref[3:0]   |                              |   |   | dpll1_current_sel_ref[3:0] |   |   |   |            |
| Bit  | Name                         | Description   |   |                            |   |   |   | Def. Value |
| 7:4  | dpll1_highest_valid_ref[3:0] | Indicates the id of the input reference of the first priority and valid. 0000 means no valid input available. |   |                            |   |   |   | 0000       |
| 3:0  | dpll1_current_sel_ref[3:0]   | Indicates the id of the current selected input reference. 0000 means no valid input available.                |   |                            |   |   |   | 0000       |

### dpll1 Priority Table Status Register [15:8]

| Register (Abbrev): dpll1_priority_table_sts[15:8]<br>Address: 0x101<br>Type: RO<br>Default Value: 0000_0000 |                          |  |   |                          |   |   |   |            |
|---|--------------------------|--|---|--------------------------|---|---|---|------------|
| 7   | 6                        | 5  | 4 | 3                        | 2 | 1 | 0 |            |
| dpll1_3rd_valid_ref[3:0]  |                          |  |   | dpll1_2nd_valid_ref[3:0] |   |   |   |            |
| Bit   | Name                     | Description  |   |                          |   |   |   | Def. Value |
| 7:4   | dpll1_3rd_valid_ref[3:0] | Indicates the id of the input reference of the third priority and valid. 0000 means no valid input available.  |   |                          |   |   |   | 0000       |
| 3:0   | dpll1_2nd_valid_ref[3:0] | Indicates the id of the input reference of the second priority and valid. 0000 means no valid input available. |   |                          |   |   |   | 0000       |

### dp11 Operating Status Register

| Register (Abbrev): dp11_operating_sts<br>Address: 0x102<br>Type: RO<br>Default Value: 100X_0001 |                              |   |                   |                |                              |   |  |
|---|------------------------------|---|-------------------|----------------|------------------------------|---|--|
| 7   | 6                            | 5   | 4                 | 3              | 2                            | 1 | 0  |
| dp11_exsync_mon_alarm   | reserved                     | dp11_dp11_soft_alarm  | dp11_master_slave | dp11_dp11_lock | dp11_dp11_operating_sts[2:0] |   |  |
| Bit   | Name                         | Description   |                   |                |                              |   | Def. Value                                     |
| 7   | dp11_exsync_mon_alarm        | 0: No alarm; ex_sync within specification<br>1: Alarm; ex_sync out of specification   |                   |                |                              |   | 1  |
| 6   | reserved                     | reserved  |                   |                |                              |   | 0  |
| 5   | dp11_dp11_soft_alarm         | 0: No alarm; dp11 within "soft threshold"<br>1: Alarm; dp11 out of "soft threshold"   |                   |                |                              |   | 0  |
| 4   | dp11_master_slave            | This bit indicates the master/slave value of the MS/SL pin.<br>0: Slave<br>1: Master  |                   |                |                              |   | Determined by MS/SL pin during reset or EEPROM |
| 3   | dp11_dp11_lock               | 0: dp11 out of phase locked<br>1: dp11 phase locked   |                   |                |                              |   | 0  |
| 2:0   | dp11_dp11_operating_sts[2:0] | 000: Not used<br>001: Free Run<br>010: Holdover<br>011: Not used<br>100: Locked<br>101: Pre-locked2<br>110: Pre_locked<br>111: Phase Lost |                   |                |                              |   | 001  |

### dp11 Current DPLL Frequency Status Register [39:0]

| Register (Abbrev): dp11_current_dp11_freq_sts[39:0]<br>Address: 0x103, 0x104, 0x105, 0x106, 0x107<br>Type: RO<br>Default Value: 0000_0000 |                                   |   |   |   |   |   |            |
|---|-----------------------------------|---|---|---|---|---|------------|
| 7   | 6                                 | 5   | 4 | 3 | 2 | 1 | 0          |
| dp11_current_dp11_freq_sts[7:0]   |                                   |   |   |   |   |   |            |
| Bit   | Name                              | Description   |   |   |   |   | Def. Value |
| 7:0   | dp11_current_dp11_freq_sts[7:0]   | This value is 2's complement signed number. Total range is +/-92 ppm, LSB is 1.68e-10 ppm.<br>This value multiplied by 1.68e-10 gives the value in ppm. |   |   |   |   | 0000_0000  |
|   | dp11_current_dp11_freq_sts[15:8]  |   |   |   |   |   |            |
|   | dp11_current_dp11_freq_sts[23:16] |   |   |   |   |   |            |
|   | dp11_current_dp11_freq_sts[31:24] |   |   |   |   |   |            |
|   | dp11_current_dp11_freq_sts[39:32] |   |   |   |   |   |            |

dpII1 Current DPLL Phase Status Register [19:0]

| Register (Abbrev): dpII1_current_dpII_phase_sts[19:0]<br>Address: 0x108, 0x109, 0x10A<br>Type: RO<br>Default Value: 0000_0000 |                                     |   |            |   |   |   |   |
|---|-------------------------------------|---|------------|---|---|---|---|
| 7   | 6                                   | 5   | 4          | 3 | 2 | 1 | 0 |
| dpII1_current_dpII_phase_sts[7:0]   |                                     |   |            |   |   |   |   |
| Bit   | Name                                | Description   | Def. Value |   |   |   |   |
| 7:0   | dpII1_current_dpII_phase_sts[7:0]   | current_dpII_phase_sts[19:0]: current dpII phase error<br>Signed 2's complement number; LSB is 0.61 ns. | 0000_0000  |   |   |   |   |
| 7:0   | dpII1_current_dpII_phase_sts[15:8]  | current_dpII_phase_sts[19:0]: current dpII phase error<br>Signed 2's complement number; LSB is 0.61 ns. | 0000_0000  |   |   |   |   |
| 7:5   | reserved                            | reserved  | 000        |   |   |   |   |
| 4:0   | dpII1_current_dpII_phase_sts[19:16] | current_dpII_phase_sts[19:0]: current dpII phase error<br>Signed 2's complement number; LSB is 0.61 ns. | 0_0000     |   |   |   |   |

dpII1 Input Mode Configuration Register

| Register (Abbrev): dpII1_input_mode_cfg<br>Address: 0x116<br>Type: RW<br>Default Value: 1010_0000 |                        |  |                      |   |          |   |                      |
|---|------------------------|--|----------------------|---|----------|---|----------------------|
| 7   | 6                      | 5  | 4                    | 3 | 2        | 1 | 0                    |
| dpII1_auto_extsync_en   | dpII1_extsync_en       | dpII1_ph_alarm_timeout   | dpII1_sync_freq[1:0] |   | reserved |   | dpII1_revertive_mode |
| Bit   | Name                   | Description  | Def. Value           |   |          |   |                      |
| 7   | dpII1_auto_extsync_en  | 0: External Frame Sync enabled/disabled depending on extsync_en bit<br>1: External Frame Sync enabled if extsync_en = 1 and dpII1 locked to source assigned to SYNC_REF_INPUT  | 1                    |   |          |   |                      |
| 6   | dpII1_extsync_en       | 0: No external Sync signal; EX_SYNC pin is ignored<br>1: With external Sync signal; EX_SYNC pin is considered  | 0                    |   |          |   |                      |
| 5   | dpII1_ph_alarm_timeout | 0: Phase alarm on sources only cancelled by software<br>1: Phase alarms on sources automatically time out. The time out value is defined in the phase_alarm_time_cfg register. | 1                    |   |          |   |                      |
| 4:3   | dpII1_sync_freq[1:0]   | These bits set the frequency of the frame sync signal input on the selected INx pin.<br>00: 8 kHz<br>01: 1 pps<br>10: 4 kHz<br>11: 2 kHz                                       | 00                   |   |          |   |                      |
| 2:1   | reserved               | reserved   | 00                   |   |          |   |                      |

### dp11 Input Mode Configuration Register

|  |                     |   |  |   |   |   |   |
|--|---------------------|---|--|---|---|---|---|
| Register (Abbrev): dp11_input_mode_cfg<br>Address: 0x116<br>Type: RW<br>Default Value: 1010_0000 |                     |   |  |   |   |   |   |
| 7  | 6                   | 5 | 4  | 3 | 2 | 1 | 0 |
| 0  | dp11_revertive_mode |   | This bit selects Revertive or Non-Revertive switching.<br>0: Non-Revertive switching. (default)<br>1: Revertive switching. |   |   |   | 0 |

### dp11 Monitor Software Register

| Register (Abbrev): dp11_mon_sw_pbo_cfg<br>Address: 0x117<br>Type: RW<br>Default Value: 0000_0000 |                            |                        |  |                            |                        |                       |                       |
|--|----------------------------|------------------------|--|----------------------------|------------------------|-----------------------|-----------------------|
| 7  | 6                          | 5                      | 4  | 3                          | 2                      | 1                     | 0                     |
| reserved   |                            | dp11_ultra_fast_switch | reserved   | dp11_hitless_switch_freeze | dp11_hitless_switch_en | dp11_freq_mon_soft_en | dp11_freq_mon_hard_en |
| Bit  | Name                       |                        | Description  |                            |                        |                       | Def. Value            |
| 7:6  | reserved                   |                        | reserved   |                            |                        |                       | 00                    |
| 5  | dp11_ultra_fast_switch     |                        | Bit to enable Ultra-fast switching mode.<br>0: Currently selected input only disqualified by leaky bucket or frequency monitors<br>1: Currently selected input disqualified after less than 3 missing input cycles |                            |                        |                       | 0                     |
| 4  | reserved                   |                        | reserved   |                            |                        |                       | 0                     |
| 3  | dp11_hitless_switch_freeze |                        | 0: Hitless switch not frozen<br>1: Hitless switch frozen; no further hitless switching events will occur   |                            |                        |                       | 0                     |
| 2  | dp11_hitless_switch_en     |                        | 0: Hitless switch disabled<br>1: Hitless switch enabled  |                            |                        |                       | 0                     |
| 1  | dp11_freq_mon_soft_en      |                        | 0: Soft frequency monitor alarms disabled<br>1: Soft frequency monitor alarms enabled  |                            |                        |                       | 0                     |
| 0  | dp11_freq_mon_hard_en      |                        | 0: Hard frequency monitor alarms disabled<br>1: Hard frequency monitor alarms enabled  |                            |                        |                       | 0                     |

### dpII1 Input 1/2 Select Priority Configuration Register

| Register (Abbrev): dpII1_in1_in2_sel_priority_cfg<br>Address: 0x118<br>Type: RW<br>Default Value: 0011_0010 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpII1_in2_priority[3:0]   |                         |   |   | dpII1_in1_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpII1_in2_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                         |   |   | 0011       |
| 3:0   | dpII1_in1_priority[3:0] |   |   |                         |   |   | 0010       |

### dpII1 Input 3/4 Select Priority Configuration Register

| Register (Abbrev): dpII1_in3_in4_sel_priority_cfg<br>Address: 0x119<br>Type: RW<br>Default Value: 0101_0100 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpII1_in4_priority[3:0]   |                         |   |   | dpII1_in3_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpII1_in4_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number is, the higher the priority is. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                         |   |   | 0101       |
| 3:0   | dpII1_in3_priority[3:0] |   |   |                         |   |   | 0100       |

### dpII1 Input 5/6 Select Priority Configuration Register

| Register (Abbrev): dpII1_in5_in6_sel_priority_cfg<br>Address: 0x11A<br>Type: RW<br>Default Value: 0111_0110 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpII1_in6_priority[3:0]   |                         |   |   | dpII1_in5_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpII1_in6_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number is, the higher the priority is. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                         |   |   | 0111       |
| 3:0   | dpII1_in5_priority[3:0] |   |   |                         |   |   | 0110       |



### dpII1 Input 7/8 Select Priority Configuration Register

| Register (Abbrev): dpII1_in7_in8_sel_priority_cfg<br>Address: 0x11B<br>Type: RW<br>Default Value: 1001_1000 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpII1_in8_priority[3:0]   |                         |   |   | dpII1_in7_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpII1_in8_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number is, the higher the priority is. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                         |   |   | 1001       |
| 3:0   | dpII1_in7_priority[3:0] |   |   |                         |   |   | 1000       |

### dpII1 Input 9/10 Select Priority Configuration Register

| Register (Abbrev): dpII1_in9_in10_sel_priority_cfg<br>Address: 0x11C<br>Type: RW<br>Default Value: 1011_1010 |                          |   |   |                         |   |   |            |
|--|--------------------------|---|---|-------------------------|---|---|------------|
| 7  | 6                        | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpII1_in10_priority[3:0]   |                          |   |   | dpII1_in9_priority[3:0] |   |   |            |
| Bit  | Name                     | Description   |   |                         |   |   | Def. Value |
| 7:4  | dpII1_in10_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number is, the higher the priority is. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                         |   |   | 1011       |
| 3:0  | dpII1_in9_priority[3:0]  |   |   |                         |   |   | 1010       |

### dpII1 Input 11/12 Select Priority Configuration Register

| Register (Abbrev): dpII1_in11_in12_sel_priority_cfg<br>Address: 0x11D<br>Type: RW<br>Default Value: 1101_1100 |                          |   |   |                          |   |   |            |
|---|--------------------------|---|---|--------------------------|---|---|------------|
| 7   | 6                        | 5   | 4 | 3                        | 2 | 1 | 0          |
| dpII1_in12_priority[3:0]  |                          |   |   | dpII1_in11_priority[3:0] |   |   |            |
| Bit   | Name                     | Description   |   |                          |   |   | Def. Value |
| 7:4   | dpII1_in12_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number is, the higher the priority is. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                          |   |   | 1101       |
| 3:0   | dpII1_in11_priority[3:0] |   |   |                          |   |   | 1100       |

### dpII1 Input 13/14 Select Priority Configuration Register

| Register (Abbrev): dpII1_in13_in14_sel_priority_cfg<br>Address: 0x11E<br>Type: RW<br>Default Value: 1111_1110 |                          |   |   |                          |   |   |            |
|---|--------------------------|---|---|--------------------------|---|---|------------|
| 7   | 6                        | 5   | 4 | 3                        | 2 | 1 | 0          |
| dpII1_in14_priority[3:0]  |                          |   |   | dpII1_in13_priority[3:0] |   |   |            |
| Bit   | Name                     | Description   |   |                          |   |   | Def. Value |
| 7:4   | dpII1_in14_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number is, the higher the priority is. If set to 0b0000, the corresponding input is disabled for auto or manual ref selection. |   |                          |   |   | 1111       |
| 3:0   | dpII1_in13_priority[3:0] |   |   |                          |   |   | 1110       |

### dpII1 Input Select Configuration Register

| Register (Abbrev): dpII1_input_sel_cfg<br>Address: 0x11F<br>Type: RW<br>Default Value: 0000_0000 |                      |  |   |                      |   |   |            |
|--|----------------------|--|---|----------------------|---|---|------------|
| 7  | 6                    | 5  | 4 | 3                    | 2 | 1 | 0          |
| reserved   |                      |  |   | dpII1_input_sel[3:0] |   |   |            |
| Bit  | Name                 | Description  |   |                      |   |   | Def. Value |
| 7:4  | reserved             | reserved   |   |                      |   |   | 0000       |
| 3:0  | dpII1_input_sel[3:0] | 0000: Automatic Input selection<br>0001: dpII1 forced to select IN1<br>0010: dpII1 forced to select IN2<br>0011: dpII1 forced to select IN3<br>0100: dpII1 forced to select IN4<br>0101: dpII1 forced to select IN5<br>0110: dpII1 forced to select IN6<br>0111: dpII1 forced to select IN7<br>1000: dpII1 forced to select IN8<br>1001: dpII1 forced to select IN9<br>1010: dpII1 forced to select IN10<br>1011: dpII1 forced to select IN11<br>1100: dpII1 forced to select IN12<br>1101: dpII1 forced to select IN13<br>1110: dpII1 forced to select IN14<br>1111: Not used |   |                      |   |   | 0000       |

### dp11 Operating Mode Configuration Register

| Register (Abbrev): dp11_operating_mode_cnfg<br>Address: 0x120<br>Type: RW<br>Default Value: 0000_0000 |                               |                   |  |   |   |   |            |
|---|-------------------------------|-------------------|--|---|---|---|------------|
| 7   | 6                             | 5                 | 4  | 3 | 2 | 1 | 0          |
| dp11_comb_mode_sel[1:0]   |                               | dp11_comb_mode_en | dp11_operating_mode_cnfg[4:0]  |   |   |   |            |
| Bit   | Name                          |                   | Description  |   |   |   | Def. Value |
| 7:6   | reserved                      |                   | reserved   |   |   |   | 0000_00    |
| 5   | reserved                      |                   | reserved   |   |   |   | 0000_00    |
| 4:0   | dp11_operating_mode_cnfg[4:0] |                   | 00000: Automatic<br>00001: Free Run<br>00010: Holdover<br>00100: Locked<br>00101: Pre-Locked2<br>00110: Pre-Locked<br>00111: Phase lost<br>01010: Write-Frequency, the dp11's loop filter output is replaced by the value from the <a href="#">dp11 Holdover Frequency Configuration Register</a> . that is updated by external processor.<br>10010: Write-Phase, the dp11's phase detector output is replaced with the value from <a href="#">dp11 Phase Offset Configuration Register [28:0]</a> that is updated by external processor.<br>Others: Reserved (do not use) |   |   |   | 0_0000     |

### dp11 Feedback Select Configuration Register

| Register (Abbrev): dp11_fb_sel_cnfg<br>Address: 0x121<br>Type: RW<br>Default Value: 0000_0000 |          |   |             |                  |   |   |            |
|---|----------|---|-------------|------------------|---|---|------------|
| 7   | 6        | 5 | 4           | 3                | 2 | 1 | 0          |
| reserved  |          |   |             | dp11_fb_sel[3:0] |   |   |            |
| Bit   | Name     |   | Description |                  |   |   | Def. Value |
| 7:4   | reserved |   | reserved    |                  |   |   | 0000       |

### dpII1 Feedback Select Configuration Register

|  |                   |   |  |   |   |   |      |
|--|-------------------|---|--|---|---|---|------|
| Register (Abbrev): dpII1_fb_sel_cnfg<br>Address: 0x121<br>Type: RW<br>Default Value: 0000_0000 |                   |   |  |   |   |   |      |
| 7  | 6                 | 5 | 4  | 3 | 2 | 1 | 0    |
| 3:0  | dpII1_fb_sel[3:0] |   | 0000: Normal internal feedback mode<br>0001: IN1 used as fb<br>0010: IN2 used as fb<br>0011: IN3 used as fb<br>0100: IN4 used as fb<br>0101: IN5 used as fb<br>0110: IN6 used as fb<br>0111: IN7 used as fb<br>1000: IN8 used as fb<br>1001: IN9 used as fb<br>1010: IN10 used as fb<br>1011: IN11 used as fb<br>1100: IN12 used as fb<br>1101: IN13 used as fb<br>1110: IN14 used as fb<br>1111: Reserved |   |   |   | 0000 |

### dpII1 Update Event Configuration Register

| Register (Abbrev): dpII1_update_event_cnfg<br>Address: 0x122<br>Type: RW<br>Default Value: 0000_0000 |                              |   |   |   |   |                              |            |
|--|------------------------------|---|---|---|---|------------------------------|------------|
| 7  | 6                            | 5   | 4 | 3 | 2 | 1                            | 0          |
| reserved   |                              |   |   |   |   | dpII1_update_event_cnfg[1:0] |            |
| Bit  | Name                         | Description   |   |   |   |                              | Def. Value |
| 7:2  | reserved                     | reserved  |   |   |   |                              | 0000_00    |
| 1:0  | dpII1_update_event_cnfg[1:0] | 00: Internal 1 PPS<br>01: Input from ex_sync<br>10: Read/write event of the corresponding registers<br>11: Event each time internal timer roll-over |   |   |   |                              | 00         |

### dpII1 DPLL Path Configuration Register

| Register (Abbrev): dpII1_dpII_path_cfg<br>Address: 0x123<br>Type: RW<br>Default Value: 0000_xxxx |                                    |   |   |                                    |   |                               |   |
|--|------------------------------------|---|---|------------------------------------|---|-------------------------------|---|
| 7  | 6                                  | 5   | 4 | 3                                  | 2 | 1                             | 0   |
| reserved   |                                    |   |   | dpII1_gsm_obsai_16e1_16t1_sel[1:0] |   | dpII1_12e1_gps_e3_t3_sel[1:0] |   |
| Bit  | Name                               | Description   |   |                                    |   |                               | Def. Value  |
| 7:4  | reserved                           | reserved  |   |                                    |   |                               | 0000  |
| 3:2  | dpII1_gsm_obsai_16e1_16t1_sel[1:0] | These bits select an output clock from the DPLL 16E1/16T1/GSM/OBSAI path.<br>00: 16E1 = 32.768 MHz (SDH)<br>01: 16T1 = 24.704 MHz (SONET)<br>10: GSM = 26.000 MHz<br>11: OBSAI = 30.720 MHz |   |                                    |   |                               | 0x, where 'x' is determined by SONET/SDH pin during reset |
| 1:0  | dpII1_12e1_gps_e3_t3_sel[1:0]      | These bits select an output clock from the DPLL 12E1/GPS/E3/T3 path.<br>00: 12E1 = 24.576 MHz (SDH)<br>01: GPS = 40.000 MHz (SONET)<br>10: E3 = 34.368 MHz<br>11: T3 = 44.736 MHz           |   |                                    |   |                               | 0x, where 'x' is determined by SONET/SDH pin during reset |

### dpII1 DPLL Start Bandwidth Damping Configuration Register

| Register (Abbrev): dpII1_dpII_start_bw_damping_cfg<br>Address: 0x124<br>Type: RW<br>Default Value: 0110_1111 |                               |   |   |                          |   |   |            |
|--|-------------------------------|---|---|--------------------------|---|---|------------|
| 7  | 6                             | 5   | 4 | 3                        | 2 | 1 | 0          |
| dpII1_dpII_start_damping[2:0]  |                               |   |   | dpII1_dpII_start_bw[4:0] |   |   |            |
| Bit  | Name                          | Description   |   |                          |   |   | Def. Value |
| 7:5  | dpII1_dpII_start_damping[2:0] | 000: Reserved<br>001: 1.2<br>010: 2.5<br>011: 5<br>100: 10<br>101: 20<br>110: Reserved<br>111: Reserved |   |                          |   |   | 011        |

dpII1 DPLL Start Bandwidth Damping Configuration Register

|   |                          |   |  |   |   |   |        |
|---|--------------------------|---|--|---|---|---|--------|
| Register (Abbrev): dpII1_dpII_start_bw_damping_cnfg<br>Address: 0x124<br>Type: RW<br>Default Value: 0110_1111 |                          |   |  |   |   |   |        |
| 7   | 6                        | 5 | 4  | 3 | 2 | 1 | 0      |
| 4:0   | dpII1_dpII_start_bw[4:0] |   | 00000: 0.090 MHz<br>00001: 0.27 MHz<br>00010: 0.90 MHz<br>00011: 2.9 MHz<br>00100: 4.3 MHz<br>00101: 8.7 MHz<br>00110: 17 MHz<br>00111: 35 MHz<br>01000: 69 MHz<br>01001: 92 MHz<br>01010: 277 MHz<br>01011: 554 MHz<br>01100: 1.1 Hz<br>01101: 2.2 Hz<br>01110: 4.4 Hz<br>01111: 8.9 Hz<br>10000: 18 Hz<br>10001: 35 Hz<br>10010: 71 Hz<br>10011: 142 Hz<br>10100: 283 Hz<br>10101: 567 Hz<br>10110-11111: Reserved |   |   |   | 0_1111 |

dpII1 DPLL Acquired Bandwidth Damping Configuration Register

| Register (Abbrev): dpII1_dpII_acq_bw_damping_cnfg<br>Address: 0x125<br>Type: RW<br>Default Value: 0110_1111 |                             |   |                        |   |   |   |            |
|---|-----------------------------|---|------------------------|---|---|---|------------|
| 7   | 6                           | 5   | 4                      | 3 | 2 | 1 | 0          |
| dpII1_dpII_acq_damping[2:0]   |                             |   | dpII1_dpII_acq_bw[4:0] |   |   |   |            |
| Bit   | Name                        | Description   |                        |   |   |   | Def. Value |
| 7:5   | dpII1_dpII_acq_damping[2:0] | 000: Reserved<br>001: 1.2<br>010: 2.5<br>011: 5<br>100: 10<br>101: 20<br>110: Reserved<br>111: Reserved |                        |   |   |   | 011        |

dpII1 DPLL Acquired Bandwidth Damping Configuration Register

|  |                        |   |  |   |   |   |        |
|--|------------------------|---|--|---|---|---|--------|
| Register (Abbrev): dpII1_dpII_acq_bw_damping_cfg<br>Address: 0x125<br>Type: RW<br>Default Value: 0110_1111 |                        |   |  |   |   |   |        |
| 7  | 6                      | 5 | 4  | 3 | 2 | 1 | 0      |
| 4:0  | dpII1_dpII_acq_bw[4:0] |   | 00000: 0.090 MHz<br>00001: 0.27 MHz<br>00010: 0.90 MHz<br>00011: 2.9 MHz<br>00100: 4.3 MHz<br>00101: 8.7 MHz<br>00110: 17 MHz<br>00111: 35 MHz<br>01000: 69 MHz<br>01001: 92 MHz<br>01010: 277 MHz<br>01011: 554 MHz<br>01100: 1.1 Hz<br>01101: 2.2 Hz<br>01110: 4.4 Hz<br>01111: 8.9 Hz<br>10000: 18 Hz<br>10001: 35 Hz<br>10010: 71 Hz<br>10011: 142 Hz<br>10100: 283 Hz<br>10101: 567 Hz<br>10110–11111: Reserved |   |   |   | 0_1111 |

dpII1 DPLL Locked Bandwidth Configuration Register

|   |                                |   |   |   |   |   |            |
|---|--------------------------------|---|---|---|---|---|------------|
| Register (Abbrev): dpII1_dpII_locked_bw_damping_cfg<br>Address: 0x126<br>Type: RW<br>Default Value: 0110_1111 |                                |   |   |   |   |   |            |
| 7   | 6                              | 5 | 4   | 3 | 2 | 1 | 0          |
| dpII1_dpII_locked_damping[2:0]  |                                |   | dpII1_dpII_locked_bw[4:0]   |   |   |   |            |
| Bit   | Name                           |   | Description   |   |   |   | Def. Value |
| 7:5   | dpII1_dpII_locked_damping[2:0] |   | 000: Reserved<br>001: 1.2<br>010: 2.5<br>011: 5<br>100: 10<br>101: 20<br>110: Reserved<br>111: Reserved |   |   |   | 011        |

dpII1 DPLL Locked Bandwidth Configuration Register

|  |                           |   |  |   |   |   |        |
|--|---------------------------|---|--|---|---|---|--------|
| Register (Abbrev): dpII1_dpII_locked_bw_damping_cnfg<br>Address: 0x126<br>Type: RW<br>Default Value: 0110_1111 |                           |   |  |   |   |   |        |
| 7  | 6                         | 5 | 4  | 3 | 2 | 1 | 0      |
| 4:0  | dpII1_dpII_locked_bw[4:0] |   | 00000: 0.090 MHz<br>00001: 0.27 MHz<br>00010: 0.90 MHz<br>00011: 2.9 MHz<br>00100: 4.3 MHz<br>00101: 8.7 MHz<br>00110: 17 MHz<br>00111: 35 MHz<br>01000: 69 MHz<br>01001: 92 MHz<br>01010: 277 MHz<br>01011: 554 MHz<br>01100: 1.1 Hz<br>01101: 2.2 Hz<br>01110: 4.4 Hz<br>01111: 8.9 Hz<br>10000: 18 Hz<br>10001: 35 Hz<br>10010: 71 Hz<br>10011: 142 Hz<br>10100: 283 Hz<br>10101: 567 Hz<br>10110-11111: Reserved |   |   |   | 0_1111 |

dpII1 Bandwidth Overshoot Configuration Register

| Register (Abbrev): dpII1_bw_overshoot_cnfg<br>Address: 0x127<br>Type: RW<br>Default Value: 1100_1111 |                                     |  |                                    |                   |                        |            |   |
|--|-------------------------------------|--|------------------------------------|-------------------|------------------------|------------|---|
| 7  | 6                                   | 5  | 4                                  | 3                 | 2                      | 1          | 0 |
| dpII1_pps_freerun_fast_freq_lock_en  | dpII1_pps_freerun_fast_ph_lock_en   | dpII1_pps_holdover_fast_freq_lock_en   | dpII1_pps_holdover_fast_ph_lock_en | dpII1_auto_bw_sel | dpII1_t0_ph_limit[2:0] |            |   |
| Bit  | Name                                | Description  |                                    |                   |                        | Def. Value |   |
| 7  | dpII1_pps_freerun_fast_freq_lock_en | 0: Disable fast frequency lock of 1 PPS.<br>1: Enable fast frequency lock mode when the loop start locks to 1 PPS from freerun.    |                                    |                   |                        | 1          |   |
| 6  | dpII1_pps_freerun_fast_ph_lock_en   | Enable Phase Snap mode for 1PPS when exiting Freerun.<br>0: Disable fast phase lock of 1PPS.<br>1: Enable fast phase lock of 1PPS. |                                    |                   |                        | 1          |   |



### dp11 Bandwidth Overshoot Configuration Register

|   |                                     |   |  |   |   |   |     |
|---|-------------------------------------|---|--|---|---|---|-----|
| Register (Abbrev): dp11_bw_overshoot_cnfg<br>Address: 0x127<br>Type: RW<br>Default Value: 1100_1111 |                                     |   |  |   |   |   |     |
| 7   | 6                                   | 5 | 4  | 3 | 2 | 1 | 0   |
| 5   | dp11_pps_holdover_fast_freq_lock_en |   | Enable Frequency Snap mode for 1PPS when exiting Freerun.<br>0: Disable fast phase lock of 1PPS.<br>1: Enable fast phase lock mode when the loop relocks to 1PPS from Holdover.  |   |   |   | 0   |
| 4   | dp11_pps_holdover_fast_ph_lock_en   |   | 0: Disable fast phase lock of 1PPS.<br>1: Enable fast phase lock mode when the loop relocks to 1PPS from Holdover.   |   |   |   | 0   |
| 3   | dp11_auto_bw_sel                    |   | 0: Always use locked bandwidth and damping factor.<br>1: Automatically select among start, acq, and locked bandwidth and damping factor  |   |   |   | 1   |
| 2:0   | dp11_ph_limit[2:0]                  |   | DPLL Phase slope selection.<br>000: GR-1244 ST3: 61 $\mu$ s/s<br>001: GR-1244 ST2, 3E, ST3 (objective): 885 ns/s<br>010: G.813 opt1, G.8262: 7.5 $\mu$ s/s<br>011: No limitation<br>100: 1 ns/s<br>101: 5 ns/s<br>110: 10 ns/s<br>111: Programmable through the <a href="#">dp11 Program Limit Configuration Register [23:0]</a> . |   |   |   | 111 |

### dp11 Phase Loss Coarse Limit Configuration Register

| Register (Abbrev): dp11_phase_loss_coarse_limit_cnfg<br>Address: 0x128<br>Type: RW<br>Default Value: 1000_0101 |                                 |   |                              |                                   |   |   |            |
|--|---------------------------------|---|------------------------------|-----------------------------------|---|---|------------|
| 7  | 6                               | 5   | 4                            | 3                                 | 2 | 1 | 0          |
| dp11_coarse_phase_loss_limit_en  | dp11_wide_range_en              | dp11_multi_phase_app  | dp11_multi_phase_8k_4k_2k_en | dp11_phase_loss_coarse_limit[3:0] |   |   |            |
| Bit  | Name                            | Description   |                              |                                   |   |   | Def. Value |
| 7  | dp11_coarse_phase_loss_limit_en | 0: Phase loss not triggered by the coarse phase lock detector<br>1: Phase loss triggered when the phase error exceeds the limit programmed in phase_loss_coarse_limit [3:0]   |                              |                                   |   |   | 1          |
| 6  | dp11_wide_range_en              | 0: Wide range (coarse) phase detector off<br>1: Wide range (coarse) phase detector on   |                              |                                   |   |   | 0          |
| 5  | dp11_multi_phase_app            | 0: DPLL phase detector limited to +/-360 degree (+/- 1 UI). However, it will still remember its original phase position over many thousands of UI if wide_range_en is set.<br>1: DPLL phase detector also uses the full coarse phase detector result. |                              |                                   |   |   | 0          |

### dpII1 Phase Loss Coarse Limit Configuration Register

|  |                                    |   |   |   |   |   |      |
|--|------------------------------------|---|---|---|---|---|------|
| Register (Abbrev): dpII1_phase_loss_coarse_limit_cfg<br>Address: 0x128<br>Type: RW<br>Default Value: 1000_0101 |                                    |   |   |   |   |   |      |
| 7  | 6                                  | 5 | 4   | 3 | 2 | 1 | 0    |
| 4  | dpII1_multi_ph_8k_4k_2k_en         |   | This bit, together with wide_range_en and ph_loss_coarse_limit[3:0], determines the coarse phase limit when the selected input clock is of 2 kHz, 4 kHz, or 8 kHz.<br>0: ph_loss_coarse_limit always set to +/-1 UI<br>1: ph_loss_coarse_limit is set to +/-1 UI if wide_range_en is set to 0. ph_loss_coarse_limit is according to ph_loss_coarse_limit[3:0] if wide_range_en is set to 1. |   |   |   | 0    |
| 3:0  | dpII1_phase_loss_coarse_limit[3:0] |   | 0000: +/- 1 UI<br>0001: +/- 3 UI<br>0010: +/- 7 UI<br>0011: +/- 15 UI<br>0100: +/- 31 UI<br>0101: +/- 63 UI<br>0110: +/- 127 UI<br>0111: +/- 255 UI<br>1000: +/- 511 UI<br>1001: +/- 1023 UI<br>1010: +/- 2047 UI (reserved)<br>1011: +/- 4095 UI (reserved)<br>1100–1111: +/- 8191 UI (reserved)   |   |   |   | 0101 |

### dpII1 Phase Loss Fine Limit Configuration Register

| Register (Abbrev): dpII1_phase_loss_fine_limit_cfg<br>Address: 0x129<br>Type: RW<br>Default Value: 1000_0010 |                                |   |   |   |                                  |   |            |
|--|--------------------------------|---|---|---|----------------------------------|---|------------|
| 7  | 6                              | 5   | 4 | 3 | 2                                | 1 | 0          |
| dpII1_fine_phase_loss_limit_en   | dpII1_fast_loss_switch         | reserved  |   |   | dpII1_phase_loss_fine_limit[2:0] |   |            |
| Bit  | Name                           | Description   |   |   |                                  |   | Def. Value |
| 7  | dpII1_fine_phase_loss_limit_en | 0: Disable<br>1: Enable   |   |   |                                  |   | 1          |
| 6  | dpII1_fast_loss_switch         | This bit controls whether the occurrence of the fast loss will result in the DPLL unlocked.<br>0: Does not result in the DPLL unlocked. DPLL will enter Temp-Holdover mode automatically.<br>1: Results in the DPLL unlocked. DPLL will enter Lost-Phase mode if the DPLL operating mode is set to auto mode. |   |   |                                  |   | 0          |
| 5:3  | reserved                       | reserved  |   |   |                                  |   | 00_0       |

dp11 Phase Loss Fine Limit Configuration Register

|   |                                 |   |  |   |   |   |     |
|---|---------------------------------|---|--|---|---|---|-----|
| Register (Abbrev): dp11_phase_loss_fine_limit_cfg<br>Address: 0x129<br>Type: RW<br>Default Value: 1000_0010 |                                 |   |  |   |   |   |     |
| 7   | 6                               | 5 | 4  | 3 | 2 | 1 | 0   |
| 2:0   | dp11_phase_loss_fine_limit[2:0] |   | The limits define the phase loss hysteresis window; +/- phase locked - phase lost. The phase detector error has to be within the phase locked window for 2 seconds before the device indicates phase lock. If it is outside the reject window at any time then fine phase loss is immediately asserted.<br><br>000: Do not use. Indicates phase loss continuously<br>001: +/-45–90°, small phase window for phase lock indication<br>010: +/-90–180°, normal phase window for phase lock indication<br>011: +/-180–360°<br>100: +/-20–25 ns<br>101: +/- 60–65 ns<br>110: +/- 120–125 ns<br>111: +/- 950–955 ns |   |   |   | 010 |

dp11 Holdover Mode Configuration Register [7:0]

| Register (Abbrev): dp11_holdover_mode_cfg[7:0]<br>Address: 0x12A<br>Type: RW<br>Default Value: 0000_0001 |                     |  |   |                     |   |                    |            |
|--|---------------------|--|---|---------------------|---|--------------------|------------|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1                  | 0          |
| reserved   |                     |  |   | dp11_hist_mode[1:0] |   | dp11_avg_mode[1:0] |            |
| Bit  | Name                | Description  |   |                     |   |                    | Def. Value |
| 7:4  | reserved            | reserved   |   |                     |   |                    | 0000       |
| 3:2  | dp11_hist_mode[1:0] | 00: Current averaged value<br>01: Averaged value 1 second before<br>10: Averaged value 10 seconds before<br>11: Averaged value 60 seconds before |   |                     |   |                    | 00         |
| 1:0  | dp11_avg_mode[1:0]  | Holdover average filter bandwidth (approximate)<br>00: 0.18 MHz<br>01: 1.5 MHz<br>10: 12 MHz<br>11: 0.5 Hz                                       |   |                     |   |                    | 01         |

dp11 Holdover Mode Configuration Register [15:8]

| Register (Abbrev): dp11_holdover_mode_cfg[15:8]<br>Address: 0x12B<br>Type: RW<br>Default Value: 0100_0100 |                              |  |               |                              |   |          |            |
|---|------------------------------|--|---------------|------------------------------|---|----------|------------|
| 7   | 6                            | 5  | 4             | 3                            | 2 | 1        | 0          |
| dp11_man_holdover   | dp11_auto_avg                | reserved   | dp11_read_avg | dp11_temp_holdover_mode[1:0] |   | reserved |            |
| Bit   | Name                         | Description  |               |                              |   |          | Def. Value |
| 7   | dp11_man_holdover            | 0: Holdover frequency is determined automatically, see auto_avg, dp11_avg_mode[1:0], and dp11_hist_mode[1:0]<br>1: Holdover frequency is from holdover_freq_cfg register   |               |                              |   |          | 0          |
| 6   | dp11_auto_avg                | 0: Instantaneous value is used as holdover frequency<br>1: Averaged value is used as holdover frequency  |               |                              |   |          | 1          |
| 5   | reserved                     | reserved   |               |                              |   |          | 0          |
| 4   | dp11_read_avg                | 0: The value read from <a href="#">dp11 Holdover Frequency Configuration Register</a> is the value written into it.<br>1: The value read from <a href="#">dp11 Holdover Frequency Configuration Register</a> is either the averaged value according to dp11_avg_mode[1:0]. |               |                              |   |          | 0          |
| 3:2   | dp11_temp_holdover_mode[1:0] | 00: Temp holdover frequency is the same as holdover mode<br>01: Temp holdover frequency is using instantaneous value<br>1x: Temp holdover frequency is using averaged value according to dp11_avg_mode[1:0]  |               |                              |   |          | 01         |
| 1:0   | reserved                     | reserved   |               |                              |   |          | 00         |

dpII1 Holdover Frequency Configuration Register

| Register (Abbrev): dpII1_holdover_freq_cfg[39:0]<br>Address: 0x12C, 0x12D, 0x12E, 0x12F, 0x130<br>Type: RW<br>Default Value: 0000_0000 |                                |  |            |   |   |   |   |
|--|--------------------------------|--|------------|---|---|---|---|
| 7  | 6                              | 5  | 4          | 3 | 2 | 1 | 0 |
| dpII1_holdover_freq_cfg[7:0]   |                                |  |            |   |   |   |   |
| dpII1_holdover_freq_cfg[15:8]  |                                |  |            |   |   |   |   |
| dpII1_holdover_freq_cfg[23:16]   |                                |  |            |   |   |   |   |
| dpII1_holdover_freq_cfg[31:24]   |                                |  |            |   |   |   |   |
| dpII1_holdover_freq_cfg[39:32]   |                                |  |            |   |   |   |   |
| Bit  | Name                           | Description  | Def. Value |   |   |   |   |
| 7:0  | dpII1_holdover_freq_cfg[7:0]   | This value is 2's complement signed number. Total range is +/-92 ppm, LSB is 1.68e-10 ppm. This value multiplied by 1.68e-10 gives the value in ppm.<br>In normal automatic holdover mode, this 40-bit value is read-only, giving the current, calculated, holdover value.<br>In manual holdover mode (man_holdover = 0), this 40-bit value is read-write, setting the Manual Holdover ppm offset.<br>In write-DCO mode (operating_mode_cfg is set to Write-Frequency), this 40-bit value is read-write, setting the DCO frequency offset from its center value. | 0000_0000  |   |   |   |   |
|  | dpII1_holdover_freq_cfg[15:8]  |  |            |   |   |   |   |
|  | dpII1_holdover_freq_cfg[23:16] |  |            |   |   |   |   |
|  | dpII1_holdover_freq_cfg[31:24] |  |            |   |   |   |   |
|  | dpII1_holdover_freq_cfg[39:32] |  |            |   |   |   |   |

dpII1 DPLL Frequency Soft Limit Configuration Register

| Register (Abbrev): dpII1_dpII_freq_soft_limit_cfg<br>Address: 0x131<br>Type: RW<br>Default Value: 1000_1100 |                                |  |            |   |   |   |   |
|---|--------------------------------|--|------------|---|---|---|---|
| 7   | 6                              | 5  | 4          | 3 | 2 | 1 | 0 |
| dpII1_freq_limit_ph_loss  | dpII1_dpII_soft_limit_cfg[6:0] |  |            |   |   |   |   |
| Bit   | Name                           | Description  | Def. Value |   |   |   |   |
| 7   | dpII1_freq_limit_ph_loss       | This bit determines whether the DPLL in hard alarm status will result in it unlocked.<br>0: Disabled<br>1: Enabled | 1          |   |   |   |   |
| 6:0   | dpII1_dpII_soft_limit_cfg[6:0] | Soft frequency threshold. Unsigned number, LSB is 0.724 ppm, total range is 92 ppm.                                | 000_1100   |   |   |   |   |

dpII1 DPLL Frequency Hard Limit Configuration Register [7:0]

| Register (Abbrev): dpII1_dpII_freq_hard_limit_cfg[7:0]<br>Address: 0x132<br>Type: RW<br>Default Value: 1010_1011 |                                |  |   |   |   |   |            |
|--|--------------------------------|--|---|---|---|---|------------|
| 7  | 6                              | 5  | 4 | 3 | 2 | 1 | 0          |
| dpII1_dpII_hard_limit_cfg[7:0]   |                                |  |   |   |   |   |            |
| Bit  | Name                           | Description  |   |   |   |   | Def. Value |
| 7:0  | dpII1_dpII_hard_limit_cfg[7:0] | Hard frequency threshold. Unsigned number, LSB is 0.0014 ppm, total range is 92 ppm. |   |   |   |   | 1010_1011  |

dpII1 DPLL Frequency Hard Limit Configuration Register [15:8]

| Register (Abbrev): dpII1_dpII_freq_hard_limit_cfg[15:8]<br>Address: 0x133<br>Type: RW<br>Default Value: 1010_1011 |                                 |  |   |   |   |   |            |
|---|---------------------------------|--|---|---|---|---|------------|
| 7   | 6                               | 5  | 4 | 3 | 2 | 1 | 0          |
| dpII1_dpII_hard_limit_cfg[15:8]   |                                 |  |   |   |   |   |            |
| Bit   | Name                            | Description  |   |   |   |   | Def. Value |
| 7:0   | dpII1_dpII_hard_limit_cfg[15:8] | Hard frequency threshold. Unsigned number, LSB is 0.0014 ppm, total range is 92 ppm. |   |   |   |   | 1010_1011  |

dpII1 Frame/Multi-Frame Sync Configuration Register

| Register (Abbrev): dpII1_fr_mfr_sync_cfg<br>Address: 0x13E<br>Type: RW<br>Default Value: 0110_0000 |                       |  |                            |                   |                    |                   |                     |
|--|-----------------------|--|----------------------------|-------------------|--------------------|-------------------|---------------------|
| 7  | 6                     | 5  | 4                          | 3                 | 2                  | 1                 | 0                   |
| dpII1_in_2k_4k_8k_inv  | dpII1_8k_1pps_sel     | dpII1_2k_1pps_sel  | dpII1_fr_mfrsync_c_pul_pos | dpII1_8k_1pps_inv | dpII1_frsync_pulse | dpII1_2k_1pps_inv | dpII1_mfrsync_pulse |
| Bit  | Name                  | Description  |                            |                   |                    |                   | Def. Value          |
| 7  | dpII1_in_2k_4k_8k_inv | This bit determines whether the input clock or sync is inverted. Input must be 1 Hz, 2 kHz, 4 kHz, or 8 kHz. Selected input's <a href="#">in{3:14}_direct_div</a> bit must be 0.<br>0: Not inverted<br>1: Inverted |                            |                   |                    |                   | 0                   |
| 6  | dpII1_8k_1pps_sel     | This bit determines whether an 8 kHz or a 1 PPS signal is enabled to be output on FRSYNC_8K_1PPS.<br>0: 1 PPS<br>1: 8 kHz  |                            |                   |                    |                   | 1                   |

dpll1 Frame/Multi-Frame Sync Configuration Register

| Register (Abbrev): dpll1_fr_mfr_sync_cfg<br>Address: 0x13E<br>Type: RW<br>Default Value: 0110_0000 |                          |   |  |   |   |   |   |
|--|--------------------------|---|--|---|---|---|---|
| 7  | 6                        | 5 | 4  | 3 | 2 | 1 | 0 |
| 5  | dpll1_2k_1pps_sel        |   | This bit determines whether a 2 kHz or a 1 PPS signal is enabled to be output on MFRSYNC_2K_1PPS.<br>0: 1 PPS<br>1: 2 kHz  |   |   |   | 1 |
| 4  | dpll1_fr_mfrsync_pul_pos |   | This bit is valid only when FRSYNC_8K_1PPS and/or MFRSYNC_2K_1PPS output 8 kHz and/or 2 kHz pulse respectively; that is, when one of the frsync_pulse bit and the mfrsync_pulse bit is 1, or when the frsync_pulse bit and the mfrsync_pulse are both 1. It determines the pulse position referring to the standard 50:50 duty cycle.<br>0: Pulsed on the falling edge of the standard 50:50 duty cycle position<br>1: Pulsed on the rising edge of the standard 50:50 duty cycle position |   |   |   | 0 |
| 3  | dpll1_8k_1pps_inv        |   | This bit determines whether the output on FRSYNC_8K_1PPS is inverted.<br>0: Not inverted<br>1: Inverted  |   |   |   | 0 |
| 2  | dpll1_frsync_pulse       |   | If FRSYNC_8K_1PPS is 8 kHz, then this bit determines whether the output on FRSYNC_8K_1PPS is 50:50 duty cycle or pulsed.<br>0: 50:50 duty cycle<br>1: Pulsed. The pulse width is defined by the period of the output on OUT1 (OUT1 should not have any phase adjustment in this case).   |   |   |   | 0 |
| 1  | dpll1_2k_1pps_inv        |   | This bit determines whether the output on MFRSYNC_2K_1PPS is inverted.<br>0: Not inverted<br>1: Inverted   |   |   |   | 0 |
| 0  | dpll1_mfrsync_pulse      |   | If FRSYNC_2K_1PPS is 2 kHz then this bit determines whether the output on MFRSYNC_2K_1PPS is 50:50 duty cycle or pulsed.<br>0: 50:50 duty cycle<br>1: Pulsed. The pulse width is defined by the period of the output on OUT1 (OUT1 should not have any phase adjustment in this case).   |   |   |   | 0 |

### dpII1 Sync Monitor Configuration Register

| Register (Abbrev): dpII1_sync_monitor_cnfg<br>Address: 0x13F<br>Type: RW<br>Default Value: 0010_1011 |                               |   |   |          |   |   |            |
|--|-------------------------------|---|---|----------|---|---|------------|
| 7  | 6                             | 5   | 4 | 3        | 2 | 1 | 0          |
| dpII1_sync_bypass  | dpII1_sync_monitor_limit[2:0] |   |   | reserved |   |   |            |
| Bit  | Name                          | Description   |   |          |   |   | Def. Value |
| 7  | dpII1_sync_bypass             | Ex sync enable/disable control<br>0: ex_sync is enabled or not is determined by <a href="#">dpII1_auto_extsync_en</a> and <a href="#">dpII1_extsync_en</a> .<br>1: ex_sync is enabled if no ex_sync_alarm   |   |          |   |   | 0          |
| 6:4  | dpII1_sync_monitor_limit[2:0] | These bits set the limit for the external sync alarm.<br>000: Sync alarm raised beyond +/- 1 UI<br>001: Sync alarm raised beyond +/- 2 UI<br>010: Sync alarm raised beyond +/- 3 UI<br>011: Sync alarm raised beyond +/- 4 UI<br>100: Sync alarm raised beyond +/- 5 UI<br>101: Sync alarm raised beyond +/- 6 UI<br>110: Sync alarm raised beyond +/- 7 UI<br>111: Sync alarm raised beyond +/- 8 UI |   |          |   |   | 010        |
| 3:0  | reserved                      | reserved  |   |          |   |   | 1011       |

### dpII1 Sync Edge Configuration Register

| Register (Abbrev): dpII1_sync_edge_cnfg<br>Address: 0x140<br>Type: RW<br>Default Value: 0000_0000 |                 |  |   |   |   |          |                 |
|---|-----------------|--|---|---|---|----------|-----------------|
| 7   | 6               | 5  | 4 | 3 | 2 | 1        | 0               |
| reserved  |                 |  |   |   |   | reserved | dpII1_sync_edge |
| Bit   | Name            | Description  |   |   |   |          | Def. Value      |
| 7:1   | reserved        | reserved   |   |   |   |          | 0000_00         |
| 0   | dpII1_sync_edge | This bit sets the alignment of the external sync inputs (falling or rising edge) |   |   |   |          | 0               |



dpII1 Phase Offset Configuration Register [28:0]

| Register (Abbrev): dpII1_phase_offset_cfg[28:0]<br>Address: 0x143, 0x144, 0x145, 0x146<br>Type: RW<br>Default Value: 0000_0000 |                               |  |   |   |   |   |   |            |
|--|-------------------------------|--|---|---|---|---|---|------------|
| 7  | 6                             | 5  | 4 | 3 | 2 | 1 | 0 |            |
| dpII1_phase_offset_cfg[7:0]  |                               |  |   |   |   |   |   |            |
| Bit  | Name                          | Description  |   |   |   |   |   | Def. Value |
| 7:0  | dpII1_phase_offset_cfg[7:0]   | 2's complement number, LSB is 0.0745 ps. Total range is $\pm 20$ $\mu$ s.  |   |   |   |   |   | 0000_0000  |
|  | dpII1_phase_offset_cfg[15:8]  | 2's complement number, LSB is 0.0745 ps. Total range is $\pm 20$ $\mu$ s.  |   |   |   |   |   |            |
|  | dpII1_phase_offset_cfg[23:16] | 2's complement number, LSB is 0.0745 ps. Total range is $\pm 20$ $\mu$ s.  |   |   |   |   |   |            |
| 7  | dpII1_ph_offset_en            | This bit determines whether the input-to-output phase offset is enabled.<br>If the device is configured as the master, the input-to-output phase offset depends on this bit.<br>0: Disabled<br>1: Enabled<br>If the device is configured as the slave, the input-to-output phase offset is always enabled. |   |   |   |   |   | 0          |
| 6:5  | reserved                      | reserved   |   |   |   |   |   | 00         |
| 4:0  | dpII1_phase_offset_cfg[28:24] | 2's complement number, LSB is 0.0745 ps. Total range is $\pm 20$ $\mu$ s.  |   |   |   |   |   | 0_0000     |

dpII1 Timer Interval Register [7:0]

| Register (Abbrev): dpII1_timer_interval[7:0]<br>Address: 0x147<br>Type: RW<br>Default Value: 0000_0000 |          |             |   |   |   |   |   |            |
|--|----------|-------------|---|---|---|---|---|------------|
| 7  | 6        | 5           | 4 | 3 | 2 | 1 | 0 |            |
| reserved   |          |             |   |   |   |   |   |            |
| Bit  | Name     | Description |   |   |   |   |   | Def. Value |
| 7:0  | reserved | reserved    |   |   |   |   |   | 00         |

dpII1 Timer Interval Register [13:8]

| Register (Abbrev): dpII1_timer_interval[13:8]<br>Address: 0x148<br>Type: RW<br>Default Value: 0000_0000 |          |             |   |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0 |            |
| reserved  |          |             |   |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   |   | Def. Value |
| 7:0   | reserved | reserved    |   |   |   |   |   | 00         |

### dpII1 System Time Status Register

| Register (Abbrev): dpII1_sys_time_sts[31:0]<br>Address: 0x149, 0x14A, 0x14B, 0x14C<br>Type: RO<br>Default Value: 0000_0000 |          |             |   |   |   |   |            |
|--|----------|-------------|---|---|---|---|------------|
| 7  | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved   |          |             |   |   |   |   |            |
| Bit  | Name     | Description |   |   |   |   | Def. Value |
| 7:0  | reserved | reserved    |   |   |   |   | 00         |

### dpII1 Bandwidth Software Time 1 Configuration Register

| Register (Abbrev): dpII1_bw_sw_time1_cnfg<br>Address: 0x14D<br>Type: RW<br>Default Value: 0000_0010 |                             |  |   |   |   |   |            |
|---|-----------------------------|--|---|---|---|---|------------|
| 7   | 6                           | 5  | 4 | 3 | 2 | 1 | 0          |
| dpII1_bw_sw_time1_cnfg[7:0]   |                             |  |   |   |   |   |            |
| Bit   | Name                        | Description  |   |   |   |   | Def. Value |
| 7:0   | dpII1_bw_sw_time1_cnfg[7:0] | <p>First settling time for the DPLL when switching from a higher bandwidth to lower bandwidth.</p> <p>When switching to a DPLL loop bandwidth that is larger than 35 MHz, and less than or equal to 554 MHz, the time in seconds it takes to transition to the new bandwidth is dictated by this register value.</p> <p>Time = bw_switch_time1_cnfg * 1 second</p> <p>Note: When switching from a smaller to a larger bandwidth, or when switching to a bandwidth greater than 554 MHz, switching happens immediately without settling time.</p> |   |   |   |   | 0000_0010  |

### dpII1 Bandwidth Software Time 2 Configuration Register

| Register (Abbrev): dpII1_bw_sw_time2_cnfg<br>Address: 0x14E<br>Type: RW<br>Default Value: 0010_0000 |                             |   |   |   |   |   |            |
|---|-----------------------------|---|---|---|---|---|------------|
| 7   | 6                           | 5   | 4 | 3 | 2 | 1 | 0          |
| dpII1_bw_sw_time2_cnfg[7:0]   |                             |   |   |   |   |   |            |
| Bit   | Name                        | Description   |   |   |   |   | Def. Value |
| 7:0   | dpII1_bw_sw_time2_cnfg[7:0] | <p>Second settling time for the DPLL when switching from a higher bandwidth to lower bandwidth.</p> <p>When switching to a DPLL loop bandwidth that is larger than 2.9 MHz, and less than or equal to 35 MHz, the time in seconds it takes to transition to the new bandwidth is dictated by this register value.</p> <p>Time = register value * 1 second</p> |   |   |   |   | 0010_0000  |

dpII1 Bandwidth Software Time 3 Configuration Register

| Register (Abbrev): dpII1_bw_sw_time3_cfg<br>Address: 0x14F<br>Type: RW<br>Default Value: 0100_0000 |                            |  |   |   |   |   |   |            |
|--|----------------------------|--|---|---|---|---|---|------------|
| 7  | 6                          | 5  | 4 | 3 | 2 | 1 | 0 |            |
| dpII1_bw_sw_time3_cfg[7:0]   |                            |  |   |   |   |   |   |            |
| Bit  | Name                       | Description  |   |   |   |   |   | Def. Value |
| 7:0  | dpII1_bw_sw_time3_cfg[7:0] | Third settling time for the DPLL when switching from a higher bandwidth to lower bandwidth.<br>When switching to a DPLL loop bandwidth that is less than or equal to 2.9 MHz, the time in seconds it takes to transition to the new bandwidth is dictated by this register value.<br>Time = register value * 4 seconds<br>Note: The resolution here is different than the previous two registers, it is in steps of 4 seconds. |   |   |   |   |   | 0100_0000  |

dpII1 Slave Force Reference Select Configuration Register

| Register (Abbrev): dpII1_slave_force_ref_sel_cfg<br>Address: 0x150<br>Type: RW<br>Default Value: 0000_1011 |                                    |  |   |                                    |   |   |   |            |
|--|------------------------------------|--|---|------------------------------------|---|---|---|------------|
| 7  | 6                                  | 5  | 4 | 3                                  | 2 | 1 | 0 |            |
| reserved   |                                    |  |   | dpII1_slave_force_ref_sel_cfg[3:0] |   |   |   |            |
| Bit  | Name                               | Description  |   |                                    |   |   |   | Def. Value |
| 7:4  | reserved                           | reserved   |   |                                    |   |   |   | 0000       |
| 3:0  | dpII1_slave_force_ref_sel_cfg[3:0] | In slave mode, this 4-bit register determines which input reference will be force selected as DPLL's reference.<br>0000: Reserved<br>0001: dpII forced to select IN1<br>0010: dpII forced to select IN2<br>0011: dpII forced to select IN3<br>0100: dpII forced to select IN4<br>0101: dpII forced to select IN5<br>0110: dpII forced to select IN6<br>0111: dpII forced to select IN7<br>1000: dpII forced to select IN8<br>1001: dpII forced to select IN9<br>1010: dpII forced to select IN10<br>1011: dpII forced to select IN11<br>1100: dpII forced to select IN12<br>1101: dpII forced to select IN13<br>1110: dpII forced to select IN14<br>1111: Reserved |   |                                    |   |   |   | 1011       |

### dpII1 Program Limit Configuration Register [23:0]

| Register (Abbrev): dpII1_prog_ph_limit_cfg[23:0]<br>Address: 0x151, 0x152, 0x153<br>Type: RW<br>Default Value: 0000_0000 |                                |   |   |                               |   |   |            |  |
|--|--------------------------------|---|---|-------------------------------|---|---|------------|--|
| 7  | 6                              | 5 | 4   | 3                             | 2 | 1 | 0          |  |
| dpII1_prog_ph_limit_cfg[7:0]   |                                |   |   | dpII1_prog_ph_limit_cfg[15:8] |   |   |            |  |
| dpII1_prog_ph_limit_cfg[23:16]   |                                |   |   |                               |   |   |            |  |
| Bit  | Name                           |   | Description   |                               |   |   | Def. Value |  |
| 7:0  | dpII1_prog_ph_limit_cfg[7:0]   |   | Programmable phase slope limit value, 2's complement, resolution<br>1 lsb = 88 ps/s |                               |   |   | 0000_0000  |  |
|  | dpII1_prog_ph_limit_cfg[15:8]  |   |   |                               |   |   |            |  |
|  | dpII1_prog_ph_limit_cfg[23:16] |   |   |                               |   |   |            |  |

## 4.5 DPLL2 Registers

### DPLL2 Priority Table Status Register [7:0]

| Register (Abbrev): dpII2_priority_table_sts[7:0]<br>Address: 0x200<br>Type: RO<br>Default Value: 0000_0000 |                              |   |  |                            |   |   |            |
|--|------------------------------|---|--|----------------------------|---|---|------------|
| 7  | 6                            | 5 | 4  | 3                          | 2 | 1 | 0          |
| dpII2_highest_valid_ref[3:0]   |                              |   |  | dpII2_current_sel_ref[3:0] |   |   |            |
| Bit  | Name                         |   | Description  |                            |   |   | Def. Value |
| 7:4  | dpII2_highest_valid_ref[3:0] |   | Indicates the id of the input reference of the highest priority and valid. |                            |   |   | 0000       |
| 3:0  | dpII2_current_sel_ref[3:0]   |   | Indicates the id of the current selected input reference.                  |                            |   |   | 0000       |

### DPLL2 Priority Table Status Register [15:8]

| Register (Abbrev): dpII2_priority_table_sts[15:8]<br>Address: 0x201<br>Type: RO<br>Default Value: 0000_0000 |                          |   |   |                        |   |   |            |
|---|--------------------------|---|---|------------------------|---|---|------------|
| 7   | 6                        | 5 | 4   | 3                      | 2 | 1 | 0          |
| dpII2_3rd_valid_ref[3:0]  |                          |   |   | dpII2_2nd_valid_ref[3] |   |   |            |
| Bit   | Name                     |   | Description   |                        |   |   | Def. Value |
| 7:4   | dpII2_3rd_valid_ref[3:0] |   | 3rd_valid_ref[3:0]. Indicates the id of the input reference of the 3rd<br>priority and valid. |                        |   |   | 0000       |
| 3:0   | dpII2_2nd_valid_ref[3]   |   | 2nd_valid_ref[3:0]. Indicates the id of the input reference of the 2nd<br>priority and valid. |                        |   |   | 0000       |

### DPLL2 Operating Status Register

| Register (Abbrev): dpll2_operating_sts<br>Address: 0x202<br>Type: RO<br>Default Value: 0000_0001 |                               |   |          |                 |                               |   |            |
|--|-------------------------------|---|----------|-----------------|-------------------------------|---|------------|
| 7  | 6                             | 5   | 4        | 3               | 2                             | 1 | 0          |
| reserved   |                               |   | reserved | dpll2_dpll_lock | dpll2_dpll_operating_sts[2:0] |   |            |
| Bit  | Name                          | Description   |          |                 |                               |   | Def. Value |
| 7:6  | reserved                      | reserved  |          |                 |                               |   | 00         |
| 5  | dpll2_dpll_soft_alarm         | 0: DPLL output within <a href="#">dpll2_dpll_soft_limit_cfg[6:0]</a><br>1: DPLL output exceeds <a href="#">dpll2_dpll_soft_limit_cfg[6:0]</a> |          |                 |                               |   | 0          |
| 4  | reserved                      | reserved  |          |                 |                               |   | 0          |
| 3  | dpll2_dpll_lock               | 0: DPLL out of phase locked<br>1: DPLL phase locked   |          |                 |                               |   | 0          |
| 2:0  | dpll2_dpll_operating_sts[2:0] | 000: Not used<br>001: Free run<br>010: Holdover<br>100: Lock<br>Others: Not used  |          |                 |                               |   | 001        |

### DPLL2 Input Mode Configuration Register

| Register (Abbrev): dpll2_input_mode_cfg<br>Address: 0x216<br>Type: RW<br>Default Value: 0000_0000 |                      |  |   |   |   |   |                      |
|---|----------------------|--|---|---|---|---|----------------------|
| 7   | 6                    | 5  | 4 | 3 | 2 | 1 | 0                    |
| reserved  |                      |  |   |   |   |   | dpll2_revertive_mode |
| Bit   | Name                 | Description  |   |   |   |   | Def. Value           |
| 7:1   | reserved             | reserved   |   |   |   |   | 0000_000             |
| 0   | dpll2_revertive_mode | 0: Non-revertive switching<br>1: Revertive switching |   |   |   |   | 0                    |

### DPLL2 Monitor Configuration Register

| Register (Abbrev): dpll2_mon_cfg<br>Address: 0x217<br>Type: RW<br>Default Value: 0000_0001 |                        |   |   |   |   |                        |                        |
|--|------------------------|---|---|---|---|------------------------|------------------------|
| 7  | 6                      | 5   | 4 | 3 | 2 | 1                      | 0                      |
| reserved   |                        |   |   |   |   | dpll2_freq_mon_soft_en | dpll2_freq_mon_hard_en |
| Bit  | Name                   | Description   |   |   |   |                        | Def. Value             |
| 7:2  | reserved               | reserved  |   |   |   |                        | 0000_00                |
| 1  | dpll2_freq_mon_soft_en | 0: Disable soft frequency monitor alarms<br>1: Enable soft frequency monitor alarms |   |   |   |                        | 0                      |
| 0  | dpll2_freq_mon_hard_en | 0: Disable hard frequency monitor alarms<br>1: Enable hard frequency monitor alarms |   |   |   |                        | 1                      |

### DPLL2 Input 1/2 Select Priority Configuration Register

| Register (Abbrev): dpll2_in1_in2_sel_priority_cfg<br>Address: 0x218<br>Type: RW<br>Default Value: 0011_0010 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpll2_in2_priority[3:0]   |                         |   |   | dpll2_in1_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpll2_in2_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                         |   |   | 0011       |
| 3:0   | dpll2_in1_priority[3:0] |   |   |                         |   |   | 0010       |

### DPLL2 Input 3/4 Select Priority Configuration Register

| Register (Abbrev): dpll2_in3_in4_sel_priority_cfg<br>Address: 0x219<br>Type: RW<br>Default Value: 0101_0100 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpll2_in4_priority[3:0]   |                         |   |   | dpll2_in3_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpll2_in4_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                         |   |   | 0101       |
| 3:0   | dpll2_in3_priority[3:0] |   |   |                         |   |   | 0100       |

### DPLL2 Input 5/6 Select Priority Configuration Register

| Register (Abbrev): dpll2_in5_in6_sel_priority_cfg<br>Address: 0x21A<br>Type: RW<br>Default Value: 0111_0110 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpll2_in6_priority[3:0]   |                         |   |   | dpll2_in5_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpll2_in6_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                         |   |   | 0111       |
| 3:0   | dpll2_in5_priority[3:0] |   |   |                         |   |   | 0110       |

### DPLL2 Input 7/8 Select Priority Configuration Register

| Register (Abbrev): dpll2_in7_in8_sel_priority_cfg<br>Address: 0x21B<br>Type: RW<br>Default Value: 1001_1000 |                         |   |   |                         |   |   |            |
|---|-------------------------|---|---|-------------------------|---|---|------------|
| 7   | 6                       | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpll2_in8_priority[3:0]   |                         |   |   | dpll2_in7_priority[3:0] |   |   |            |
| Bit   | Name                    | Description   |   |                         |   |   | Def. Value |
| 7:4   | dpll2_in8_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                         |   |   | 1001       |
| 3:0   | dpll2_in7_priority[3:0] |   |   |                         |   |   | 1000       |

### DPLL2 Input 9/10 Select Priority Configuration Register

| Register (Abbrev): dpll2_in9_in10_sel_priority_cfg<br>Address: 0x21C<br>Type: RW<br>Default Value: 1011_1010 |                          |   |   |                         |   |   |            |
|--|--------------------------|---|---|-------------------------|---|---|------------|
| 7  | 6                        | 5   | 4 | 3                       | 2 | 1 | 0          |
| dpll2_in10_priority[3:0]   |                          |   |   | dpll2_in9_priority[3:0] |   |   |            |
| Bit  | Name                     | Description   |   |                         |   |   | Def. Value |
| 7:4  | dpll2_in10_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                         |   |   | 1011       |
| 3:0  | dpll2_in9_priority[3:0]  |   |   |                         |   |   | 1010       |

### DPLL2 Input 11/12 Select Priority Configuration Register

| Register (Abbrev): dpll2_in11_in12_sel_priority_cfg<br>Address: 0x21D<br>Type: RW<br>Default Value: 1101_1100 |                          |   |   |                          |   |   |            |
|---|--------------------------|---|---|--------------------------|---|---|------------|
| 7   | 6                        | 5   | 4 | 3                        | 2 | 1 | 0          |
| dpll2_in12_priority[3:0]  |                          |   |   | dpll2_in11_priority[3:0] |   |   |            |
| Bit   | Name                     | Description   |   |                          |   |   | Def. Value |
| 7:4   | dpll2_in12_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                          |   |   | 1101       |
| 3:0   | dpll2_in11_priority[3:0] |   |   |                          |   |   | 1100       |

### DPLL2 Input 13/14 Select Priority Configuration Register

| Register (Abbrev): dpll2_in13_in14_sel_priority_cfg<br>Address: 0x21E<br>Type: RW<br>Default Value: 1111_1110 |                          |   |   |                          |   |   |            |
|---|--------------------------|---|---|--------------------------|---|---|------------|
| 7   | 6                        | 5   | 4 | 3                        | 2 | 1 | 0          |
| dpll2_in14_priority[3:0]  |                          |   |   | dpll2_in13_priority[3:0] |   |   |            |
| Bit   | Name                     | Description   |   |                          |   |   | Def. Value |
| 7:4   | dpll2_in14_priority[3:0] | Sets the priority number of the corresponding input reference. The lower the number, the higher the priority.<br>If set to 0000, the corresponding input is disable for auto ref selection. |   |                          |   |   | 1111       |
| 3:0   | dpll2_in13_priority[3:0] |   |   |                          |   |   | 1110       |

### DPLL2 Input Select Configuration Register

| Register (Abbrev): dpll2_input_sel_cfg<br>Address: 0x21F<br>Type: RW<br>Default Value: 0000_0000 |          |             |   |                      |   |   |            |
|--|----------|-------------|---|----------------------|---|---|------------|
| 7  | 6        | 5           | 4 | 3                    | 2 | 1 | 0          |
| reserved   |          |             |   | dpll2_input_sel[3:0] |   |   |            |
| Bit  | Name     | Description |   |                      |   |   | Def. Value |
| 7:4  | reserved | reserved    |   |                      |   |   | 0000       |



DPLL2 Input Select Configuration Register

|  |                      |   |  |   |   |   |      |
|--|----------------------|---|--|---|---|---|------|
| Register (Abbrev): dpll2_input_sel_cfg<br>Address: 0x21F<br>Type: RW<br>Default Value: 0000_0000 |                      |   |  |   |   |   |      |
| 7  | 6                    | 5 | 4  | 3 | 2 | 1 | 0    |
| 3:0  | dpll2_input_sel[3:0] |   | 0000: Automatic input selection<br>0001: DPLL2 forced to select IN1<br>0010: DPLL2 forced to select IN2<br>0011: DPLL2 forced to select IN3<br>0100: DPLL2 forced to select IN4<br>0101: DPLL2 forced to select IN5<br>0110: DPLL2 forced to select IN6<br>0111: DPLL2 forced to select IN7<br>1000: DPLL2 forced to select IN8<br>1001: DPLL2 forced to select IN9<br>1010: DPLL2 forced to select IN10<br>1011: DPLL2 forced to select IN11<br>1100: DPLL2 forced to select IN12<br>1101: DPLL2 forced to select IN13<br>1110: DPLL2 forced to select IN14<br>1111: Reserved |   |   |   | 0000 |

DPLL2 Operating Mode Configuration Register

| Register (Abbrev): dpll2_operating_mode_cfg<br>Address: 0x220<br>Type: RW<br>Default Value: 0000_0000 |                               |   |   |   |                               |   |            |
|---|-------------------------------|---|---|---|-------------------------------|---|------------|
| 7   | 6                             | 5   | 4 | 3 | 2                             | 1 | 0          |
| reserved  |                               |   |   |   | dpll2_operating_mode_cfg[2:0] |   |            |
| Bit   | Name                          | Description   |   |   |                               |   | Def. Value |
| 7:3   | reserved                      | reserved  |   |   |                               |   | 0000_0     |
| 2:0   | dpll2_operating_mode_cfg[2:0] | 000: Automatic<br>001: Free run<br>010: Holdover<br>100: Lock<br>Others: Not used |   |   |                               |   | 000        |

### DPLL2 DPLL Locked Bandwidth Damping Configuration Register

| Register (Abbrev): dpll2_dpll_locked_bw_damping_cfg<br>Address: 0x226<br>Type: RW<br>Default Value: 0110_0000 |                                |   |          |   |   |                           |            |
|---|--------------------------------|---|----------|---|---|---------------------------|------------|
| 7   | 6                              | 5   | 4        | 3 | 2 | 1                         | 0          |
| dpll2_dpll_locked_damping[2:0]  |                                |   | reserved |   |   | dpll2_dpll_locked_bw[1:0] |            |
| Bit   | Name                           | Description   |          |   |   |                           | Def. Value |
| 7:5   | dpll2_dpll_locked_damping[2:0] | 000: Reserved<br>001: 1.2<br>010: 2.5<br>011: 5<br>100: 10<br>101: 20<br>110–111: Reserved  |          |   |   |                           | 011        |
| 4:2   | reserved                       | reserved  |          |   |   |                           | 0_00       |
| 1:0   | dpll2_dpll_locked_bw[1:0]      | Sets the loop bandwidth for DPLL2 in locked state. The bandwidth varies inversely with DivN (see <a href="#">DPLL2 Divisor N Interrupt Configuration Register</a> ). Locked frequency is also constrained by dpll2_hard_freq_limit_cfg.<br>00: 25–52 Hz<br>01: 54–120 Hz<br>10: 74–150 Hz<br>11: Reserved |          |   |   |                           | 00         |

### Reserved

| Register (Abbrev): N/A<br>Address: 0x227<br>Type: RW<br>Default Value: 0000_0011 |          |             |   |   |   |   |            |
|--|----------|-------------|---|---|---|---|------------|
| 7  | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved   |          |             |   |   |   |   |            |
| Bit  | Name     | Description |   |   |   |   | Def. Value |
| 7:0  | reserved | reserved    |   |   |   |   | 0000_0011  |

### DPLL2 Phase Loss Coarse Limit Register

| Register (Abbrev): dpll2_phase_loss_coarse_limit_cfg<br>Address: 0x228<br>Type: RW<br>Default Value: 1000_0101 |                                    |   |                            |                                    |   |   |            |
|--|------------------------------------|---|----------------------------|------------------------------------|---|---|------------|
| 7  | 6                                  | 5   | 4                          | 3                                  | 2 | 1 | 0          |
| dpll2_coarse_phase_loss_limit_en   | dpll2_wide_range_en                | dpll2_multi_phase_app   | dpll2_multi_ph_8k_4k_2k_en | dpll2_phase_loss_coarse_limit[3:0] |   |   |            |
| Bit  | Name                               | Description   |                            |                                    |   |   | Def. Value |
| 7  | dpll2_coarse_phase_loss_limit_en   | 0: Phase loss not triggered by the coarse phase lock detector<br>1: Phase loss triggered when the phase error exceeds the limit programmed in phase_loss_coarse_limit [3:0]   |                            |                                    |   |   | 1          |
| 6  | dpll2_wide_range_en                | 0: Wide range phase detector off<br>1: Wide range phase detector on   |                            |                                    |   |   | 0          |
| 5  | dpll2_multi_phase_app              | 0: DPLL phase detector limited to +/-360 degree (+/- 1 UI). However, it will still remember its original phase position over many thousands of UI if wide_range_en is set.<br>1: DPLL phase detector also uses the full coarse phase detector result.   |                            |                                    |   |   | 0          |
| 4  | dpll2_multi_ph_8k_en               | This bit, together with the wide_range_en and the ph_loss_coarse_limit[3:0] bits, determines the coarse phase limit when the selected input clock is of 8 kHz.<br>0: ph_loss_coarse_limit always set to +/-1 UI<br>1: ph_loss_coarse_limit is set to +/-1 UI if wide_range_en is set to 0. ph_loss_coarse_limit is according to ph_loss_coarse_limit[3:0] if wide_range_en is set to 1. |                            |                                    |   |   | 0          |
| 3:0  | dpll2_phase_loss_coarse_limit[3:0] | 0000: +/- 1 UI<br>0001: +/- 3 UI<br>0010: +/- 7 UI<br>0011: +/- 15 UI<br>0100: +/- 31 UI<br>0101: +/- 63 UI<br>0110: +/- 127 UI<br>0111: +/- 255 UI<br>1000: +/- 511 UI<br>1001: +/- 1023 UI<br>1010–1111: Reserved   |                            |                                    |   |   | 0101       |

### DPLL2 Phase Loss Fine Limit Configuration Register

| Register (Abbrev): dpll2_phase_loss_fine_limit_cnfg<br>Address: 0x229<br>Type: RW<br>Default Value: 1000_0010 |                                  |  |   |   |                                  |   |            |
|---|----------------------------------|--|---|---|----------------------------------|---|------------|
| 7   | 6                                | 5  | 4 | 3 | 2                                | 1 | 0          |
| dpll2_fine_phase_loss_limit_en  |                                  | reserved   |   |   | dpll2_phase_loss_fine_limit[2:0] |   |            |
| Bit   | Name                             | Description  |   |   |                                  |   | Def. Value |
| 7   | dpll2_fine_phase_loss_limit_en   | 0: Disable<br>1: Enable  |   |   |                                  |   | 1          |
| 6:3   | reserved                         | reserved   |   |   |                                  |   | 000_0      |
| 2:0   | dpll2_phase_loss_fine_limit[2:0] | 000: Do not use; indicates phase loss continuously<br>001: +/-45–90°, small phase window for phase lock indication<br>010: +/-90–180°, normal phase window for phase lock indication<br>011: +/-180–360°<br>100: +/-20–25 ns<br>101: +/- 60–65 ns<br>110: +/- 120–125 ns<br>111: +/- 950–955 ns<br>Larger phase window for phase lock indication. The phase position of the inputs to the DPLL has to be within the window limit for 1–2 seconds before the device indicates phase lock. If it is outside the window for any time, then phase loss is indicated immediately. |   |   |                                  |   | 010        |

### DPLL2 Holdover Mode Configuration Register

| Register (Abbrev): dpll2_holdover_mode_cnfg<br>Address: 0x22B<br>Type: RW<br>Default Value: 0000_0000 |                |  |   |   |   |   |            |
|---|----------------|--|---|---|---|---|------------|
| 7   | 6              | 5  | 4 | 3 | 2 | 1 | 0          |
| reserved  | dpll2_auto_avg | reserved   |   |   |   |   |            |
| Bit   | Name           | Description  |   |   |   |   | Def. Value |
| 7   | reserved       | reserved   |   |   |   |   | 0          |
| 6   | dpll2_auto_avg | 0: Holdover frequency is the instantaneous value of integral path just before entering holdover<br>1: Averaged frequency value is used as holdover frequency |   |   |   |   | 0          |
| 5:0   | reserved       | reserved   |   |   |   |   | 00_0000    |

### DPLL2 DPLL Frequency Soft Limit Configuration Register

| Register (Abbrev): dpll2_dpll_freq_soft_limit_cfg<br>Address: 0x231<br>Type: RW<br>Default Value: 1000_1100 |                                |   |   |   |   |   |            |
|---|--------------------------------|---|---|---|---|---|------------|
| 7   | 6                              | 5   | 4 | 3 | 2 | 1 | 0          |
| dpll2_freq_limit_ph_loss  | dpll2_dpll_soft_limit_cfg[6:0] |   |   |   |   |   |            |
| Bit   | Name                           | Description   |   |   |   |   | Def. Value |
| 7   | dpll2_freq_limit_ph_loss       | Determines whether the DPLL in hard alarm status will result in it unlocked.<br>0: Disabled<br>1: Enabled   |   |   |   |   | 1          |
| 6:0   | dpll2_dpll_soft_limit_cfg[6:0] | Soft frequency threshold, unsigned number. If the output frequency of DPLL2 exceeds this limit, <a href="#">dpll2_dpll_soft_alarm</a> will be high.<br>Resolution is inversely related to DivN (see <a href="#">dpll2_divn_int_cfg[5:0]</a> ) and is given by the equation:<br>$\text{LSB} = (2 / \text{DivN}) * 1/2^{16} = 2 * \text{dpll2\_fout} / 1.6384 \text{ GHz} * 1/2^{16}$ Default:<br>$\text{LSB} = 2 * 98.304 \text{ MHz} / 1.6384 \text{ MHz} * 1/2^{16} = 1.83 \text{ ppm}$ Max range = +/-234 ppm |   |   |   |   | 000_1100   |

### DPLL2 DPLL Frequency Hard Limit Configuration Register [7:0]

| Register (Abbrev): dpll2_dpll_freq_hard_limit_cfg[7:0]<br>Address: 0x232<br>Type: RW<br>Default Value: 1010_1011 |                                |  |   |   |   |   |            |
|--|--------------------------------|--|---|---|---|---|------------|
| 7  | 6                              | 5  | 4 | 3 | 2 | 1 | 0          |
| dpll2_dpll_hard_limit_cfg[7:0]   |                                |  |   |   |   |   |            |
| Bit  | Name                           | Description  |   |   |   |   | Def. Value |
| 7:0  | dpll2_dpll_hard_limit_cfg[7:0] | Hard frequency threshold; unsigned number. The output frequency of DPLL2 will not exceed the limit set by this register.<br>Resolution is inversely related to DivN (see <a href="#">dpll2_divn_int_cfg[5:0]</a> ) and is given by the equation:<br>$\text{LSB} = (2 / \text{DivN}) * 1/2^{25} = 2 * \text{dpll2\_fout} / 1.6384 \text{ GHz} * 1/2^{25}$ Default:<br>$\text{LSB} = 2 * 98.304 \text{ MHz} / 1.6384 \text{ MHz} * 1/2^{25} = 3.57 \text{ ppb}$ Max range = +/-234 ppm |   |   |   |   | 1010_1011  |

### DPLL2 DPLL Frequency Hard Limit Configuration Register [15:8]

| Register (Abbrev): dpll2_dpll_freq_hard_limit_cfg[15:8]<br>Address: 0x233<br>Type: RW<br>Default Value: 0001_1001 |                                 |   |   |   |   |   |   |            |
|---|---------------------------------|---|---|---|---|---|---|------------|
| 7   | 6                               | 5   | 4 | 3 | 2 | 1 | 0 |            |
| dpll2_dpll_hard_limit_cfg[15:8]   |                                 |   |   |   |   |   |   |            |
| Bit   | Name                            | Description   |   |   |   |   |   | Def. Value |
| 7:0   | dpll2_dpll_hard_limit_cfg[15:8] | Hard frequency threshold; unsigned number. The output frequency of DPLL2 will not exceed the limit set by this register.<br>Resolution is inversely related to DivN (see <a href="#">dpll2_divn_int_cfg[5:0]</a> ) and is given by the equation:<br>$LSB = (2 / DivN) * 1/2^{25} = 2 * dpll2\_fout / 1.6384 \text{ GHz} * 1/2^{25}$<br>Default:<br>$LSB = 2 * 98.304 \text{ MHz} / 1 \text{ 638.4 MHz} * 1/2^{25} = 3.57 \text{ ppb}$<br>Max range = +/-234 ppm |   |   |   |   |   | 0001_1001  |

### DPLL2 Feedback Divisor Configuration Register [7:0]

| Register (Abbrev): dpll2_fbdiv_cfg[7:0]<br>Address: 0x250<br>Type: RW<br>Default Value: 1111_1111 |                      |   |   |   |   |   |   |            |
|---|----------------------|---|---|---|---|---|---|------------|
| 7   | 6                    | 5   | 4 | 3 | 2 | 1 | 0 |            |
| dpll2_fbdiv_cfg[7:0]  |                      |   |   |   |   |   |   |            |
| Bit   | Name                 | Description   |   |   |   |   |   | Def. Value |
| 7:0   | dpll2_fbdiv_cfg[7:0] | DPLL2 integer feedback divider ratio. The DPLL2 output frequency is divided by the this value plus 1 to give the 8 kHz feedback required by DPLL2.<br>$f_{out\_dpll2} = (fbdiv\_cfg + 1) * 8 \text{ kHz}$<br>(The output frequency of DPLL2 here must agree with the setting of DivN; see <a href="#">dpll2_divn_int_cfg[5:0]</a> .)<br>Default:<br>$f_{out\_dpll2} = (x2FFF + 1) * 8\text{kHz} = 98.304 \text{ MHz}$ |   |   |   |   |   | 1111_1111  |

### DPLL2 Feedback Divisor Configuration Register [13:8]

| Register (Abbrev): dpll2_fbdiv_cfg[13:8]<br>Address: 0x251<br>Type: RW<br>Default Value: 0010_1111 |          |                       |   |   |   |   |   |            |
|--|----------|-----------------------|---|---|---|---|---|------------|
| 7  | 6        | 5                     | 4 | 3 | 2 | 1 | 0 |            |
| reserved   |          | dpll2_fbdiv_cfg[13:8] |   |   |   |   |   |            |
| Bit  | Name     | Description           |   |   |   |   |   | Def. Value |
| 7:6  | reserved | reserved              |   |   |   |   |   | 00         |

DPLL2 Feedback Divisor Configuration Register [13:8]

|  |                       |   |   |   |   |   |         |
|--|-----------------------|---|---|---|---|---|---------|
| Register (Abbrev): dpll2_fbdiv_cfg[13:8]<br>Address: 0x251<br>Type: RW<br>Default Value: 0010_1111 |                       |   |   |   |   |   |         |
| 7  | 6                     | 5 | 4   | 3 | 2 | 1 | 0       |
| 5:0  | dpll2_fbdiv_cfg[13:8] |   | DPLL2 integer feedback divider ratio. The DPLL2 output frequency is divided by the this value plus 1 to give the 8 kHz feedback required by DPLL2.<br>$f_{out\_dpll2} = (fbdiv\_cfg + 1) * 8 \text{ kHz}$<br>(The output frequency of DPLL2 here must agree with the setting of DivN; see <a href="#">dpll2_divn_int_cfg[5:0]</a> .)<br>Default:<br>$f_{out\_dpll2} = (x2FFF + 1) * 8\text{kHz} = 98.304 \text{ MHz}$ |   |   |   | 10_1111 |

DPLL2 Divisor N Fractional L Configuration Register

| Register (Abbrev): dpll2_divn_frac_l_cfg<br>Address: 0x252<br>Type: RW<br>Default Value: 0101_0101 |                          |  |   |   |   |   |            |
|--|--------------------------|--|---|---|---|---|------------|
| 7  | 6                        | 5  | 4 | 3 | 2 | 1 | 0          |
| dpll2_divn_frac_cfg[7:0]   |                          |  |   |   |   |   |            |
| Bit  | Name                     | Description  |   |   |   |   | Def. Value |
| 7:0  | dpll2_divn_frac_cfg[7:0] | divn_frac_cfg[23:0]: Fractional part of dpll2 output divisor; Unsigned |   |   |   |   | 0101_0101  |

DPLL2 Divisor N Fractional M Configuration Register

| Register (Abbrev): dpll2_divn_frac_m_cfg<br>Address: 0x253<br>Type: RW<br>Default Value: 0101_0101 |                           |  |   |   |   |   |            |
|--|---------------------------|--|---|---|---|---|------------|
| 7  | 6                         | 5  | 4 | 3 | 2 | 1 | 0          |
| dpll2_divn_frac_cfg[15:8]  |                           |  |   |   |   |   |            |
| Bit  | Name                      | Description  |   |   |   |   | Def. Value |
| 7:0  | dpll2_divn_frac_cfg[15:8] | divn_frac_cfg[23:0]: Fractional part of dpll2 output divisor; Unsigned |   |   |   |   | 0101_0101  |

### DPLL2 Divisor N Fractional H Configuration Register

| Register (Abbrev): dpll2_divn_frac_h_cfg<br>Address: 0x254<br>Type: RW<br>Default Value: 0001_0101 |                            |  |                            |   |   |   |            |
|--|----------------------------|--|----------------------------|---|---|---|------------|
| 7  | 6                          | 5  | 4                          | 3 | 2 | 1 | 0          |
| reserved   |                            |  | dpll2_divn_frac_cfg[20:16] |   |   |   |            |
| Bit  | Name                       | Description  |                            |   |   |   | Def. Value |
| 7:5  | reserved                   | reserved   |                            |   |   |   | 000        |
| 4:0  | dpll2_divn_frac_cfg[20:16] | divn_frac_cfg[23:0]: Fractional part of dpll2 output divisor; Unsigned |                            |   |   |   | 1_0101     |

### DPLL2 Divisor N Denominator L Configuration Register

| Register (Abbrev): dpll2_divn_den_l_cfg<br>Address: 0x255<br>Type: RW<br>Default Value: 0000_0000 |                         |  |   |   |   |   |            |
|---|-------------------------|--|---|---|---|---|------------|
| 7   | 6                       | 5  | 4 | 3 | 2 | 1 | 0          |
| dpll2_divn_den_cfg[7:0]   |                         |  |   |   |   |   |            |
| Bit   | Name                    | Description  |   |   |   |   | Def. Value |
| 7:0   | dpll2_divn_den_cfg[7:0] | divn_den_cfg[15:0]: Fractional part of dpll2 output divisor, denominator; Unsigned |   |   |   |   | 0000_0000  |

### DPLL2 Divisor N Denominator H Configuration Register

| Register (Abbrev): dpll2_divn_den_h_cfg<br>Address: 0x256<br>Type: RW<br>Default Value: 0011_0000 |                          |  |   |   |   |   |            |
|---|--------------------------|--|---|---|---|---|------------|
| 7   | 6                        | 5  | 4 | 3 | 2 | 1 | 0          |
| dpll2_divn_den_cfg[15:8]  |                          |  |   |   |   |   |            |
| Bit   | Name                     | Description  |   |   |   |   | Def. Value |
| 7:0   | dpll2_divn_den_cfg[15:8] | divn_den_cfg[15:0]: Fractional part of dpll2 output divisor, denominator; Unsigned |   |   |   |   | 0011_0000  |



### DPLL2 Divisor N Numerator L Configuration Register

| Register (Abbrev): dpll2_divn_num_l_cfg<br>Address: 0x257<br>Type: RW<br>Default Value: 0000_0000 |                         |  |   |   |   |   |   |            |
|---|-------------------------|--|---|---|---|---|---|------------|
| 7   | 6                       | 5  | 4 | 3 | 2 | 1 | 0 |            |
| dpll2_divn_num_cfg[7:0]   |                         |  |   |   |   |   |   |            |
| Bit   | Name                    | Description  |   |   |   |   |   | Def. Value |
| 7:0   | dpll2_divn_num_cfg[7:0] | divn_num_cfg[15:0]: Fractional part of dpll2 output divisor, numerator; Unsigned |   |   |   |   |   | 0000_0000  |

### DPLL2 Divisor N Numerator H Configuration Register

| Register (Abbrev): dpll2_divn_num_h_cfg<br>Address: 0x258<br>Type: RW<br>Default Value: 0001_0000 |                          |  |   |   |   |   |   |            |
|---|--------------------------|--|---|---|---|---|---|------------|
| 7   | 6                        | 5  | 4 | 3 | 2 | 1 | 0 |            |
| dpll2_divn_num_cfg[15:8]  |                          |  |   |   |   |   |   |            |
| Bit   | Name                     | Description  |   |   |   |   |   | Def. Value |
| 7:0   | dpll2_divn_num_cfg[15:8] | divn_num_cfg[15:0]: Fractional part of dpll2 output divisor, numerator; Unsigned |   |   |   |   |   | 0001_0000  |

### DPLL2 Divisor N Interrupt Configuration Register

| Register (Abbrev): dpll2_divn_int_cfg<br>Address: 0x259<br>Type: RW<br>Default Value: 0001_0000 |                         |   |   |   |   |   |   |            |
|---|-------------------------|---|---|---|---|---|---|------------|
| 7   | 6                       | 5   | 4 | 3 | 2 | 1 | 0 |            |
| reserved  |                         | dpll2_divn_int_cfg[5:0]   |   |   |   |   |   |            |
| Bit   | Name                    | Description   |   |   |   |   |   | Def. Value |
| 7:6   | reserved                | reserved  |   |   |   |   |   | 00         |
| 5:0   | dpll2_divn_int_cfg[5:0] | divn_int_cfg[5:0]: Integer part of DPLL2 output divisor; Unsigned.<br>The output frequency of DPLL2 is established by the equation:<br>$f_{out\_dpll2} = 1\ 638.4\ \text{MHz} / \text{DivN}$ $f_{out\_dpll2} = 1\ 638.4\ \text{MHz} / (\text{divn\_int\_cfg} + (\text{divn\_frac\_cfg} + \text{divn\_num\_cfg} / \text{divn\_den\_cfg}) / 2^{21})$ (The output frequency of DPLL2 set here must agree with the setting of dpll2_dpll_fbdiv_cfg.)<br>Valid range of DivN is 16.384 ( $f_{out\_dpll2} = 100\ \text{MHz}$ ) to 31.995 ( $f_{out\_dpll2} = 51.208\ \text{MHz}$ )<br>Default:<br>$f_{out\_dpll2} = 1\ 638.4\ \text{MHz} / (x_{10} + (x_{155555} + x_{1000} / x_{3000}) / 2^{21}) = 1\ 638.4\ \text{MHz} / 16.666 = 98.304\ \text{MHz}$ |   |   |   |   |   | 01_0000    |

### DPLL2 DPLL DSM Configuration Register

| Register (Abbrev): dpll2_dpll_dsm_cfg<br>Address: 0x25C<br>Type: RW<br>Default Value: 0000_0001 |                            |  |   |                        |   |                            |            |
|---|----------------------------|--|---|------------------------|---|----------------------------|------------|
| 7   | 6                          | 5  | 4 | 3                      | 2 | 1                          | 0          |
| reserved  |                            |  |   | dpll2_dither_gain[1:0] |   | dpll2_dsm_ordpll2_der[1:0] |            |
| Bit   | Name                       | Description  |   |                        |   |                            | Def. Value |
| 7:4   | reserved                   | reserved   |   |                        |   |                            | 0000       |
| 3:2   | dpll2_dither_gain[1:0]     | 00: No dither<br>01: LSB<br>10: 2*LSB<br>11: 4*LSB             |   |                        |   |                            | 00         |
| 1:0   | dpll2_dsm_ordpll2_der[1:0] | 00: Integer<br>01: 1st order<br>10: 2nd order<br>11: 3rd order |   |                        |   |                            | 01         |

## 5 APLL1 Registers

### APLL1 Charge Pump Current Control Configuration Register

| Register (Abbrev): apll1_icp_ctrl_cnfg<br>Address: 0x280<br>Type: RW<br>Default Value: 0001_0000 |                          |   |                          |   |   |   |            |
|--|--------------------------|---|--------------------------|---|---|---|------------|
| 7  | 6                        | 5   | 4                        | 3 | 2 | 1 | 0          |
| reserved   |                          |   | apll1_icp_ctrl_code[4:0] |   |   |   |            |
| Bit  | Name                     | Description   |                          |   |   |   | Def. Value |
| 7:5  | reserved                 | reserved  |                          |   |   |   | 000        |
| 4:0  | apll1_icp_ctrl_code[4:0] | APLL charge pump current selection: current is (icp_ctrl_code X 40 uA)<br>Increased charge-pump current results in faster settling but more ringing.<br>0_0000: Charge pump is shut off<br>0_0001: 40 uA<br>0_0010: 80 uA<br>...<br>1_1111: 1240 uA |                          |   |   |   | 1_0000     |

### APLL1 Divisor Fractional L Configuration Register

| Register (Abbrev): apll1_divisor_frac_l_cnfg<br>Address: 0x281<br>Type: RW<br>Default Value: 1101_1100 |                           |   |   |   |   |   |            |
|--|---------------------------|---|---|---|---|---|------------|
| 7  | 6                         | 5   | 4 | 3 | 2 | 1 | 0          |
| apll1_divn_frac_cnfg[7:0]  |                           |   |   |   |   |   |            |
| Bit  | Name                      | Description   |   |   |   |   | Def. Value |
| 7:0  | apll1_divn_frac_cnfg[7:0] | Fractional part of divisor: Unsigned, Default: 'h4cedc ('d315004) |   |   |   |   | 1101_1100  |

### APLL1 Divisor Fractional M Configuration Register

| Register (Abbrev): apll1_divisor_frac_m_cnfg<br>Address: 0x282<br>Type: RW<br>Default Value: 1100_1110 |                            |   |   |   |   |   |            |
|--|----------------------------|---|---|---|---|---|------------|
| 7  | 6                          | 5   | 4 | 3 | 2 | 1 | 0          |
| apll1_divn_frac_cnfg[15:8]   |                            |   |   |   |   |   |            |
| Bit  | Name                       | Description   |   |   |   |   | Def. Value |
| 7:0  | apll1_divn_frac_cnfg[15:8] | Fractional part of divisor: Unsigned, Default: 'h4cedc ('d315004) |   |   |   |   | 1100_1110  |

### APLL1 Divisor Fractional H Configuration Register

| Register (Abbrev): apll1_divisor_frac_h_cfg<br>Address: 0x283<br>Type: RW<br>Default Value: 0000_0000 |                            |   |                            |   |   |   |            |
|---|----------------------------|---|----------------------------|---|---|---|------------|
| 7   | 6                          | 5   | 4                          | 3 | 2 | 1 | 0          |
| reserved  |                            |   | apll1_divn_frac_cfg[20:16] |   |   |   |            |
| Bit   | Name                       | Description   |                            |   |   |   | Def. Value |
| 7:5   | reserved                   | reserved  |                            |   |   |   | 000        |
| 4:0   | apll1_divn_frac_cfg[20:16] | Fractional part of divisor: Unsigned, Default: 'h4cedc ('d315004) |                            |   |   |   | 0_0000     |

### APLL1 Divisor Denominator L Configuration Register

| Register (Abbrev): apll1_divisor_den_l_cfg<br>Address: 0x284<br>Type: RW<br>Default Value: 1110_0110 |                         |   |   |   |   |   |            |
|--|-------------------------|---|---|---|---|---|------------|
| 7  | 6                       | 5   | 4 | 3 | 2 | 1 | 0          |
| apll1_divn_den_cfg[7:0]  |                         |   |   |   |   |   |            |
| Bit  | Name                    | Description   |   |   |   |   | Def. Value |
| 7:0  | apll1_divn_den_cfg[7:0] | Fractional part of divisor, denominator: Unsigned, Default: 'd486 |   |   |   |   | 1110_0110  |

### APLL1 Divisor Denominator H Configuration Register

| Register (Abbrev): apll1_divisor_den_h_cfg<br>Address: 0x285<br>Type: RW<br>Default Value: 0000_0001 |                          |   |   |   |   |   |            |
|--|--------------------------|---|---|---|---|---|------------|
| 7  | 6                        | 5   | 4 | 3 | 2 | 1 | 0          |
| apll1_divn_den_cfg[15:8]   |                          |   |   |   |   |   |            |
| Bit  | Name                     | Description   |   |   |   |   | Def. Value |
| 7:0  | apll1_divn_den_cfg[15:8] | Fractional part of divisor, denominator: Unsigned, Default: 'd486 |   |   |   |   | 0000_0001  |

### APLL1 Divisor Numerator L Configuration Register

| Register (Abbrev): apll1_divisor_num_l_cfg<br>Address: 0x286<br>Type: RW<br>Default Value: 0100_1001 |                         |  |   |   |   |   |            |
|--|-------------------------|--|---|---|---|---|------------|
| 7  | 6                       | 5  | 4 | 3 | 2 | 1 | 0          |
| apll1_divn_num_cfg[7:0]  |                         |  |   |   |   |   |            |
| Bit  | Name                    | Description  |   |   |   |   | Def. Value |
| 7:0  | apll1_divn_num_cfg[7:0] | Fractional part of divisor, numerator: Unsigned, Default: 'd73 |   |   |   |   | 0100_1001  |

### APLL1 Divisor Numerator H Configuration Register

| Register (Abbrev): apll1_divisor_num_h_cfg<br>Address: 0x287<br>Type: RW<br>Default Value: 0000_0000 |                          |  |   |   |   |   |            |
|--|--------------------------|--|---|---|---|---|------------|
| 7  | 6                        | 5  | 4 | 3 | 2 | 1 | 0          |
| apll1_divn_num_cfg[15:8]   |                          |  |   |   |   |   |            |
| Bit  | Name                     | Description  |   |   |   |   | Def. Value |
| 7:0  | apll1_divn_num_cfg[15:8] | Fractional part of divisor, numerator: Unsigned, Default: 'd73 |   |   |   |   | 0000_0000  |

### APLL1 DSM Configuration Register

| Register (Abbrev): apll1_dsm_cfg<br>Address: 0x288<br>Type: RW<br>Default Value: 0010_0011 |                            |   |                  |                        |   |                            |            |
|--|----------------------------|---|------------------|------------------------|---|----------------------------|------------|
| 7  | 6                          | 5   | 4                | 3                      | 2 | 1                          | 0          |
| apll1_path_freq_cfg[2:0]   |                            |   | apll1_dsm_cfg_en | apll1_dither_gain[1:0] |   | apll1_dsm_orapll1_der[1:0] |            |
| Bit  | Name                       | Description   |                  |                        |   |                            | Def. Value |
| 7:5  | apll1_path_freq_cfg[2:0]   | These bits select reference clock path and output clock rate of APLL.<br>000: 622.08 MHz from DPLL1<br>001: 625 MHz from DPLL1<br>010: 625 * FEC MHz from DPLL1<br>Others: Reserved |                  |                        |   |                            | 001        |
| 4  | apll1_dsm_cfg_en           | 0: DSM uses pre-set parameters<br>1: DSM uses programmable parameters   |                  |                        |   |                            | 0          |
| 3:2  | apll1_dither_gain[1:0]     | 00: No dither<br>01: LSB<br>10: 2 * LSB<br>11: 4 * LSB  |                  |                        |   |                            | 00         |
| 1:0  | apll1_dsm_orapll1_der[1:0] | 00: Integer<br>01: 1st order<br>10: 2nd order<br>11: 3rd order  |                  |                        |   |                            | 11         |

### APLL1 Divisor Integer Configuration Register

| Register (Abbrev): apll1_divisor_int_cfg<br>Address: 0x289<br>Type: RW<br>Default Value: 0010_0000 |                         |  |   |   |   |   |            |
|--|-------------------------|--|---|---|---|---|------------|
| 7  | 6                       | 5  | 4 | 3 | 2 | 1 | 0          |
| reserved   |                         | apll1_divn_int_cfg[5:0]  |   |   |   |   |            |
| Bit  | Name                    | Description  |   |   |   |   | Def. Value |
| 7:6  | reserved                | reserved   |   |   |   |   | 00         |
| 5:0  | apll1_divn_int_cfg[5:0] | Integer part of divisor: Unsigned, $N=0\sim 2^6$ , div by $N+1$ . Default: 'd31, div by 32 |   |   |   |   | 10_0000    |

### APLL1 Frame/Multi-Frame Ratio Configuration Register [7:0]

| Register (Abbrev): apll1_fr_ratio_cfg[7:0]<br>Address: 0x28A<br>Type: RW<br>Default Value: 0001_1111 |                         |   |   |   |   |   |            |
|--|-------------------------|---|---|---|---|---|------------|
| 7  | 6                       | 5   | 4 | 3 | 2 | 1 | 0          |
| apll1_fr_ratio_cfg[7:0]  |                         |   |   |   |   |   |            |
| Bit  | Name                    | Description   |   |   |   |   | Def. Value |
| 7:0  | apll1_fr_ratio_cfg[7:0] | For debug purposes only. manually configure fr_gen in APLL.<br>$fr\_ratio\_cfg=fapll\_out/2-1$<br>For example: $fapll\_out = 625MHz$ , $fr\_ratio\_cfg=625000000/2-1$ |   |   |   |   | 0001_1111  |

### APLL1 Frame/Multi-Frame Ratio Configuration Register [15:8]

| Register (Abbrev): apll1_fr_ratio_cfg[15:8]<br>Address: 0x28B<br>Type: RW<br>Default Value: 0101_1111 |                          |   |   |   |   |   |            |
|---|--------------------------|---|---|---|---|---|------------|
| 7   | 6                        | 5   | 4 | 3 | 2 | 1 | 0          |
| apll1_fr_ratio_cfg[15:8]  |                          |   |   |   |   |   |            |
| Bit   | Name                     | Description   |   |   |   |   | Def. Value |
| 7:0   | apll1_fr_ratio_cfg[15:8] | For debug purposes only. Manually configure fr_gen in APLL.<br>$fr\_ratio\_cfg=fapll\_out/2-1$<br>For example: $fapll\_out = 625MHz$ , $fr\_ratio\_cfg=625000000/2-1$ |   |   |   |   | 0101_1111  |

APLL1 Frame/Multi-Frame Ratio Configuration Register [23:16]

| Register (Abbrev): apll1_fr_ratio_cnfg[23:16]<br>Address: 0x28C<br>Type: RW<br>Default Value: 1010_0000 |                            |  |   |   |   |   |            |
|---|----------------------------|--|---|---|---|---|------------|
| 7   | 6                          | 5  | 4 | 3 | 2 | 1 | 0          |
| apll1_fr_ratio_cnfg[23:16]  |                            |  |   |   |   |   |            |
| Bit   | Name                       | Description  |   |   |   |   | Def. Value |
| 7:0   | apll1_fr_ratio_cnfg[23:16] | For debug purposes only. Manually configure fr_gen in APLL.<br>fr_ratio_cnfg=fapll_out/2-1<br>For example: fapll_out = 625MHz, fr_ratio_cnfg=625000000/2-1 |   |   |   |   | 1010_0000  |

APLL1 Frame/Multi-Frame Ratio Configuration Register [28:24]

| Register (Abbrev): apll1_fr_ratio_cnfg[28:24]<br>Address: 0x28D<br>Type: RW<br>Default Value: 0001_0010 |                            |  |                            |   |   |   |            |
|---|----------------------------|--|----------------------------|---|---|---|------------|
| 7   | 6                          | 5  | 4                          | 3 | 2 | 1 | 0          |
| reserved  |                            |  | apll1_fr_ratio_cnfg[28:24] |   |   |   |            |
| Bit   | Name                       | Description  |                            |   |   |   | Def. Value |
| 7:5   | reserved                   | reserved   |                            |   |   |   | 000        |
| 4:0   | apll1_fr_ratio_cnfg[28:24] | For debug purposes only. Manually configure fr_gen in APLL.<br>fr_ratio_cnfg=fapll_out/2-1<br>For example: fapll_out = 625MHz, fr_ratio_cnfg=625000000/2-1 |                            |   |   |   | 1_0010     |

## 6 APLL2 Registers

### APLL2 Change Pump Current Control Configuration Register

| Register (Abbrev): apll2_icp_ctrl_cnfg<br>Address: 0x28E<br>Type: RW<br>Default Value: 0001_0000 |                          |   |                          |   |   |   |            |
|--|--------------------------|---|--------------------------|---|---|---|------------|
| 7  | 6                        | 5   | 4                        | 3 | 2 | 1 | 0          |
| reserved   |                          |   | apll2_icp_ctrl_code[4:0] |   |   |   |            |
| Bit  | Name                     | Description   |                          |   |   |   | Def. Value |
| 7:5  | reserved                 | reserved  |                          |   |   |   | 000        |
| 4:0  | apll2_icp_ctrl_code[4:0] | APLL charge pump current selection: current is (icp_ctrl_code X 40 uA)<br>Increased charge-pump current results in faster settling but more ringing.<br>0_0000: Charge pump is shut off<br>0_0001: 40 uA<br>0_0010: 80 uA<br>...<br>1_1111: 1240 uA |                          |   |   |   | 1_0000     |

### APLL2 Divisor Fractional L Configuration Register

| Register (Abbrev): apll2_divisor_frac_l_cnfg<br>Address: 0x28F<br>Type: RW<br>Default Value: 1101_1100 |                           |   |   |   |   |   |            |
|--|---------------------------|---|---|---|---|---|------------|
| 7  | 6                         | 5   | 4 | 3 | 2 | 1 | 0          |
| apll2_divn_frac_cnfg[7:0]  |                           |   |   |   |   |   |            |
| Bit  | Name                      | Description   |   |   |   |   | Def. Value |
| 7:0  | apll2_divn_frac_cnfg[7:0] | divn_frac_cnfg[20:0]: Fractional part of divisor: Unsigned, Default: 'h4cedc ('d315004) |   |   |   |   | 1101_1100  |

### APLL2 Divisor Fractional M Configuration Register

| Register (Abbrev): apll2_divisor_frac_m_cnfg<br>Address: 0x290<br>Type: RW<br>Default Value: 1100_1110 |                            |   |   |   |   |   |            |
|--|----------------------------|---|---|---|---|---|------------|
| 7  | 6                          | 5   | 4 | 3 | 2 | 1 | 0          |
| apll2_divn_frac_cnfg[15:8]   |                            |   |   |   |   |   |            |
| Bit  | Name                       | Description   |   |   |   |   | Def. Value |
| 7:0  | apll2_divn_frac_cnfg[15:8] | divn_frac_cnfg[20:0]: Fractional part of divisor: Unsigned, Default: 'h4cedc ('d315004) |   |   |   |   | 1100_1110  |



### APLL2 Divisor Fractional H Configuration Register

| Register (Abbrev): apll2_divisor_frac_h_cfg<br>Address: 0x291<br>Type: RW<br>Default Value: 0000_0000 |                            |  |                            |   |   |   |            |
|---|----------------------------|--|----------------------------|---|---|---|------------|
| 7   | 6                          | 5  | 4                          | 3 | 2 | 1 | 0          |
| reserved  |                            |  | apll2_divn_frac_cfg[20:16] |   |   |   |            |
| Bit   | Name                       | Description  |                            |   |   |   | Def. Value |
| 7:5   | reserved                   | reserved   |                            |   |   |   | 000        |
| 4:0   | apll2_divn_frac_cfg[20:16] | divn_frac_cfg[20:0]: Fractional part of divisor: Unsigned, Default: 'h4cedc ('d315004) |                            |   |   |   | 0_0000     |

### APLL2 Divisor Denominator L Configuration Register

| Register (Abbrev): apll2_divisor_den_l_cfg<br>Address: 0x292<br>Type: RW<br>Default Value: 1110_0110 |                         |   |   |   |   |   |            |
|--|-------------------------|---|---|---|---|---|------------|
| 7  | 6                       | 5   | 4 | 3 | 2 | 1 | 0          |
| apll2_divn_den_cfg[7:0]  |                         |   |   |   |   |   |            |
| Bit  | Name                    | Description   |   |   |   |   | Def. Value |
| 7:0  | apll2_divn_den_cfg[7:0] | divn_den_cfg[15:0]: Fractional part of divisor, denominator: Unsigned, Default: 'd486 |   |   |   |   | 1110_0110  |

### APLL2 Divisor Denominator H Configuration Register

| Register (Abbrev): apll2_divisor_den_h_cfg<br>Address: 0x293<br>Type: RW<br>Default Value: 0000_0001 |                          |             |   |   |   |   |            |
|--|--------------------------|-------------|---|---|---|---|------------|
| 7  | 6                        | 5           | 4 | 3 | 2 | 1 | 0          |
| apll2_divn_den_cfg[15:8]   |                          |             |   |   |   |   |            |
| Bit  | Name                     | Description |   |   |   |   | Def. Value |
| 7:0  | apll2_divn_den_cfg[15:8] |             |   |   |   |   | 0000_0001  |

### APLL2 Divisor Numerator L Configuration Register

| Register (Abbrev): apll2_divisor_num_l_cfg<br>Address: 0x294<br>Type: RW<br>Default Value: 0100_1001 |                         |  |   |   |   |   |   |            |
|--|-------------------------|--|---|---|---|---|---|------------|
| 7  | 6                       | 5  | 4 | 3 | 2 | 1 | 0 |            |
| apll2_divn_num_cfg[7:0]  |                         |  |   |   |   |   |   |            |
| Bit  | Name                    | Description  |   |   |   |   |   | Def. Value |
| 7:0  | apll2_divn_num_cfg[7:0] | divn_num_cfg[15:0]: Fractional part of divisor, numerator: Unsigned, Default: 'd73 |   |   |   |   |   | 0100_1001  |

### APLL2 Divisor Numerator H Configuration Register

| Register (Abbrev): apll2_divisor_num_h_cfg<br>Address: 0x295<br>Type: RW<br>Default Value: 0000_0000 |                          |  |   |   |   |   |   |            |
|--|--------------------------|--|---|---|---|---|---|------------|
| 7  | 6                        | 5  | 4 | 3 | 2 | 1 | 0 |            |
| apll2_divn_num_cfg[15:8]   |                          |  |   |   |   |   |   |            |
| Bit  | Name                     | Description  |   |   |   |   |   | Def. Value |
| 7:0  | apll2_divn_num_cfg[15:8] | divn_num_cfg[15:0]: Fractional part of divisor, numerator: Unsigned, Default: 'd73 |   |   |   |   |   | 0000_0000  |

### APLL2 DSM Configuration Register

| Register (Abbrev): apll2_dsm_cfg<br>Address: 0x296<br>Type: RW<br>Default Value: 1010_0011 |                          |   |                  |                        |   |                            |   |            |
|--|--------------------------|---|------------------|------------------------|---|----------------------------|---|------------|
| 7  | 6                        | 5   | 4                | 3                      | 2 | 1                          | 0 |            |
| apll2_path_freq_cfg[2:0]   |                          |   | apll2_dsm_cfg_en | apll2_dither_gain[1:0] |   | apll2_dsm_orapll2_der[1:0] |   |            |
| Bit  | Name                     | Description   |                  |                        |   |                            |   | Def. Value |
| 7:5  | apll2_path_freq_cfg[2:0] | These bits select reference clock path and output clock rate of APLL.<br>3'b000: 622.08 MHz from DPPLL1<br>3'b001: 625 MHz from DPPLL1<br>3'b010: 625 * FEC MHz from DPPLL1<br>Others: Reserved |                  |                        |   |                            |   | 101        |
| 4  | apll2_dsm_cfg_en         | 0: dsm uses pre-set parameters<br>1: dsm uses programmable parameters   |                  |                        |   |                            |   | 0          |

### APLL2 DSM Configuration Register

|  |                            |   |  |   |   |   |    |
|--|----------------------------|---|--|---|---|---|----|
| Register (Abbrev): apll2_dsm_cfg<br>Address: 0x296<br>Type: RW<br>Default Value: 1010_0011 |                            |   |  |   |   |   |    |
| 7  | 6                          | 5 | 4  | 3 | 2 | 1 | 0  |
| 3:2  | apll2_dither_gain[1:0]     |   | 00: No dither<br>01: LSB<br>10: 2 * LSB<br>11: 4 * LSB         |   |   |   | 00 |
| 1:0  | apll2_dsm_orapll2_der[1:0] |   | 00: Integer<br>01: 1st order<br>10: 2nd order<br>11: 3rd order |   |   |   | 11 |

### APLL2 Divisor Integer Configuration Register

| Register (Abbrev): apll2_divisor_int_cfg<br>Address: 0x297<br>Type: RW<br>Default Value: 0010_0000 |                         |   |   |   |   |   |            |
|--|-------------------------|---|---|---|---|---|------------|
| 7  | 6                       | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved   |                         | apll2_divn_int_cfg[5:0]   |   |   |   |   |            |
| Bit  | Name                    | Description   |   |   |   |   | Def. Value |
| 7:6  | reserved                | reserved  |   |   |   |   | 00         |
| 5:0  | apll2_divn_int_cfg[5:0] | Integer part of divisor: Unsigned, N=0~2 <sup>6</sup> , div by N+1. Default: 'd31, div by 32. |   |   |   |   | 10_0000    |

### APLL2 Frame/Multi-Frame Ratio Configuration Register [7:0]

| Register (Abbrev): apll2_fr_ratio_cfg[7:0]<br>Address: 0x298<br>Type: RW<br>Default Value: 0001_1111 |                         |   |   |   |   |   |            |
|--|-------------------------|---|---|---|---|---|------------|
| 7  | 6                       | 5   | 4 | 3 | 2 | 1 | 0          |
| apll2_fr_ratio_cfg[7:0]  |                         |   |   |   |   |   |            |
| Bit  | Name                    | Description   |   |   |   |   | Def. Value |
| 7:0  | apll2_fr_ratio_cfg[7:0] | For debug purposes only. Manually configure fr_gen in apll<br>fr_ratio_cfg=fapll_out/2-1<br>For example: fapll_out = 625MHz, fr_ratio_cfg=625000000/2-1 |   |   |   |   | 0001_1111  |

APLL2 Frame/Multi-Frame Ratio Configuration Register [15:8]

| Register (Abbrev): apll2_fr_ratio_cnfg[15:8]<br>Address: 0x299<br>Type: RW<br>Default Value: 0101_1111 |                           |   |   |   |   |   |            |
|--|---------------------------|---|---|---|---|---|------------|
| 7  | 6                         | 5   | 4 | 3 | 2 | 1 | 0          |
| apll2_fr_ratio_cnfg[15:0]  |                           |   |   |   |   |   |            |
| Bit  | Name                      | Description   |   |   |   |   | Def. Value |
| 7:0  | apll2_fr_ratio_cnfg[15:0] | For debug purposes only. Manually configure fr_gen in APLL.<br>fr_ratio_cnfg=fapll_out/2-1<br>For example: fapll_out = 625 MHz, fr_ratio_cnfg=625000000/2-1 |   |   |   |   | 0101_1111  |

APLL2 Frame/Multi-Frame Ratio Configuration Register [23:16]

| Register (Abbrev): apll2_fr_ratio_cnfg[23:16]<br>Address: 0x29A<br>Type: RW<br>Default Value: 1010_0000 |                           |   |   |   |   |   |            |
|---|---------------------------|---|---|---|---|---|------------|
| 7   | 6                         | 5   | 4 | 3 | 2 | 1 | 0          |
| apll2_fr_ratio_cnfg[23:0]   |                           |   |   |   |   |   |            |
| Bit   | Name                      | Description   |   |   |   |   | Def. Value |
| 7:0   | apll2_fr_ratio_cnfg[23:0] | For debug purposes only. Manually configure fr_gen in APLL.<br>fr_ratio_cnfg=fapll_out/2-1<br>For example: fapll_out = 625 MHz, fr_ratio_cnfg=625000000/2-1 |   |   |   |   | 1010_0000  |

APLL2 Frame/Multi-Frame Ratio Configuration Register [28:24]

| Register (Abbrev): apll2_fr_ratio_cnfg[28:24]<br>Address: 0x29B<br>Type: RW<br>Default Value: 0001_0010 |                            |   |                            |   |   |   |            |
|---|----------------------------|---|----------------------------|---|---|---|------------|
| 7   | 6                          | 5   | 4                          | 3 | 2 | 1 | 0          |
| reserved  |                            |   | apll2_fr_ratio_cnfg[28:24] |   |   |   |            |
| Bit   | Name                       | Description   |                            |   |   |   | Def. Value |
| 7:5   | reserved                   | reserved  |                            |   |   |   | 000        |
| 4:0   | apll2_fr_ratio_cnfg[28:24] | For debug purposes only. Manually configure fr_gen in APLL.<br>fr_ratio_cnfg=fapll_out/2-1<br>For example: fapll_out = 625 MHz, fr_ratio_cnfg=625000000/2-1 |                            |   |   |   | 1_0010     |

### System Charge Pump Current Control Configuration Register

| Register (Abbrev): sys_icp_ctrl_cnfg |                        |   |                        |   |   |   |            |
|--------------------------------------|------------------------|---|------------------------|---|---|---|------------|
| Address: 0x29C                       |                        |   |                        |   |   |   |            |
| Type: RW                             |                        |   |                        |   |   |   |            |
| Default Value: 0000_1010             |                        |   |                        |   |   |   |            |
| 7                                    | 6                      | 5   | 4                      | 3 | 2 | 1 | 0          |
| reserved                             |                        |   | sys_icp_ctrl_code[4:0] |   |   |   |            |
| Bit                                  | Name                   | Description   |                        |   |   |   | Def. Value |
| 7:5                                  | reserved               | reserved  |                        |   |   |   | 000        |
| 4:0                                  | sys_icp_ctrl_code[4:0] | APLL charge pump current selection: current is (icp_ctrl_code X 40 uA)<br>Increased charge-pump current results in faster settling but more ringing.<br>0_0000: Charge pump is shut off<br>0_0001: 40 uA<br>0_0010: 80 uA<br>...<br>1_1111: 1240 uA |                        |   |   |   | 0_1010     |

### System Divisor Fractional L Configuration Register

| Register (Abbrev): sys_divisor_frac_l_cnfg |                         |  |   |   |   |   |            |
|--|-------------------------|--|---|---|---|---|------------|
| Address: 0x29D                             |                         |  |   |   |   |   |            |
| Type: RW                                   |                         |  |   |   |   |   |            |
| Default Value: 1011_1010                   |                         |  |   |   |   |   |            |
| 7  | 6                       | 5  | 4 | 3 | 2 | 1 | 0          |
| sys_divn_frac_cnfg[7:0]                    |                         |  |   |   |   |   |            |
| Bit  | Name                    | Description  |   |   |   |   | Def. Value |
| 7:0  | sys_divn_frac_cnfg[7:0] | divn_frac_cnfg[20:0]: Fractional part of divisor: Unsigned |   |   |   |   | 1011_1010  |

### System Divisor Fractional M Configuration Register

| Register (Abbrev): sys_divisor_frac_m_cnfg |                          |  |   |   |   |   |            |
|--|--------------------------|--|---|---|---|---|------------|
| Address: 0x29E                             |                          |  |   |   |   |   |            |
| Type: RW                                   |                          |  |   |   |   |   |            |
| Default Value: 0100_1001                   |                          |  |   |   |   |   |            |
| 7  | 6                        | 5  | 4 | 3 | 2 | 1 | 0          |
| sys_divn_frac_cnfg[15:8]                   |                          |  |   |   |   |   |            |
| Bit  | Name                     | Description  |   |   |   |   | Def. Value |
| 7:0  | sys_divn_frac_cnfg[15:8] | divn_frac_cnfg[20:0]: Fractional part of divisor: Unsigned |   |   |   |   | 0100_1001  |

### System Divisor Fractional H Configuration Register

| Register (Abbrev): sys_divisor_frac_h_cfg<br>Address: 0x29F<br>Type: RW<br>Default Value: 0000_1100 |                          |   |                          |   |   |   |            |
|---|--------------------------|---|--------------------------|---|---|---|------------|
| 7   | 6                        | 5   | 4                        | 3 | 2 | 1 | 0          |
| reserved  |                          |   | sys_divn_frac_cfg[20:16] |   |   |   |            |
| Bit   | Name                     | Description   |                          |   |   |   | Def. Value |
| 7:5   | reserved                 | reserved  |                          |   |   |   | 000        |
| 4:0   | sys_divn_frac_cfg[20:16] | divn_frac_cfg[20:0]: Fractional part of divisor: Unsigned |                          |   |   |   | 0_1100     |

### System Divisor Denominator L Configuration Register

| Register (Abbrev): sys_divisor_den_l_cfg<br>Address: 0x2A0<br>Type: RW<br>Default Value: 0111_1101 |                       |   |   |   |   |   |            |
|--|-----------------------|---|---|---|---|---|------------|
| 7  | 6                     | 5   | 4 | 3 | 2 | 1 | 0          |
| sys_divn_den_cfg[7:0]  |                       |   |   |   |   |   |            |
| Bit  | Name                  | Description   |   |   |   |   | Def. Value |
| 7:0  | sys_divn_den_cfg[7:0] | divn_den_cfg[15:0]: Fractional part of divisor, denominator: Unsigned |   |   |   |   | 0111_1101  |

### System Divisor Denominator L Configuration Register

| Register (Abbrev): sys_divisor_den_l_cfg<br>Address: 0x2A1<br>Type: RW<br>Default Value: 0000_0000 |                        |   |   |   |   |   |            |
|--|------------------------|---|---|---|---|---|------------|
| 7  | 6                      | 5   | 4 | 3 | 2 | 1 | 0          |
| sys_divn_den_cfg[15:8]   |                        |   |   |   |   |   |            |
| Bit  | Name                   | Description   |   |   |   |   | Def. Value |
| 7:0  | sys_divn_den_cfg[15:8] | divn_den_cfg[15:0]: Fractional part of divisor, denominator: Unsigned |   |   |   |   | 0000_0000  |

### System Divisor Numerator L Configuration Register

| Register (Abbrev): sys_divisor_num_l_cfg<br>Address: 0x2A2<br>Type: RW<br>Default Value: 0010_1110 |                       |   |   |   |   |   |            |
|--|-----------------------|---|---|---|---|---|------------|
| 7  | 6                     | 5   | 4 | 3 | 2 | 1 | 0          |
| sys_divn_num_cfg[7:0]  |                       |   |   |   |   |   |            |
| Bit  | Name                  | Description   |   |   |   |   | Def. Value |
| 7:0  | sys_divn_num_cfg[7:0] | divn_num_cfg[15:0]: Fractional part of divisor, numerator: Unsigned |   |   |   |   | 0010_1110  |

### System Divisor Numerator L Configuration Register

| Register (Abbrev): sys_divisor_num_l_cfg<br>Address: 0x2A3<br>Type: RW<br>Default Value: 0000_0000 |                        |   |   |   |   |   |            |
|--|------------------------|---|---|---|---|---|------------|
| 7  | 6                      | 5   | 4 | 3 | 2 | 1 | 0          |
| sys_divn_num_cfg[15:8]   |                        |   |   |   |   |   |            |
| Bit  | Name                   | Description   |   |   |   |   | Def. Value |
| 7:0  | sys_divn_num_cfg[15:8] | divn_num_cfg[15:0]: Fractional part of divisor, numerator: Unsigned |   |   |   |   | 0000_0000  |

### System DSM Configuration Register

| Register (Abbrev): sys_dsm_cfg<br>Address: 0x2A4<br>Type: RW<br>Default Value: 0000_0011 |                        |   |                |                      |   |                        |            |
|--|------------------------|---|----------------|----------------------|---|------------------------|------------|
| 7  | 6                      | 5   | 4              | 3                    | 2 | 1                      | 0          |
| reserved   |                        |   | sys_dsm_cfg_en | sys_dither_gain[1:0] |   | sys_dsm_orsys_der[1:0] |            |
| Bit  | Name                   | Description   |                |                      |   |                        | Def. Value |
| 7:5  | reserved               | reserved  |                |                      |   |                        | 000        |
| 4  | sys_dsm_cfg_en         | 0: DSM uses pre-set parameters<br>1: DSM uses programmable parameters |                |                      |   |                        | 0          |
| 3:2  | sys_dither_gain[1:0]   | 00: No dither<br>01: LSB<br>10: 2 * LSB<br>11: 4 * LSB                |                |                      |   |                        | 00         |
| 1:0  | sys_dsm_orsys_der[1:0] | 00: Integer<br>01: 1st order<br>10: 2nd order<br>11: 3rd order        |                |                      |   |                        | 11         |

### System Divisor Integer Configuration Register

| Register (Abbrev): sys_divisor_int_cfg<br>Address: 0x2A5<br>Type: RW<br>Default Value: 0001_1110 |                       |  |   |   |   |   |            |
|--|-----------------------|--|---|---|---|---|------------|
| 7  | 6                     | 5  | 4 | 3 | 2 | 1 | 0          |
| reserved   |                       | sys_divn_int_cfg[5:0]  |   |   |   |   |            |
| Bit  | Name                  | Description  |   |   |   |   | Def. Value |
| 7:6  | reserved              | reserved   |   |   |   |   | 00         |
| 5:0  | sys_divn_int_cfg[5:0] | Integer part of divisor: Unsigned, $N=0\sim 2^6$ , div by $N+1$ . Default: 'd31, div by 32 |   |   |   |   | 01_0000    |

### PLL204 Divisor N Configuration Register

| Register (Abbrev): pll204_divn_cfg<br>Address: 0x2A6<br>Type: RW<br>Default Value: 0000_1001 |                          |   |                          |   |   |   |            |
|--|--------------------------|---|--------------------------|---|---|---|------------|
| 7  | 6                        | 5   | 4                        | 3 | 2 | 1 | 0          |
| sys_pll204_divn_cfg_en   | reserved                 |   | sys_pll204_divn_cfg[4:0] |   |   |   |            |
| Bit  | Name                     | Description   |                          |   |   |   | Def. Value |
| 7  | sys_pll204_divn_cfg_en   | For debug purposes only. Manually configure pll204 fb div ratio. $N+1$ is the actual div ratio. |                          |   |   |   | 0          |
| 6:5  | reserved                 | reserved  |                          |   |   |   | 00         |
| 4:0  | sys_pll204_divn_cfg[4:0] | For debug purposes only. Manually configure pll204 fb div ratio. $N+1$ is the actual div ratio. |                          |   |   |   | 0_1001     |

## 6.1 Output Registers

For 83P33xxx I/O Mapping, see section [8 82P337xx I/O Mapping](#)

### Output 1 Mux Configuration Register

| Register (Abbrev): out1_mux_cfg<br>Address: 0x300<br>Type: RW<br>Default Value: 0000_0000 |          |  |   |                   |   |   |            |
|---|----------|--|---|-------------------|---|---|------------|
| 7   | 6        | 5  | 4 | 3                 | 2 | 1 | 0          |
| out1_pdn  | out1_inv | out1_squelch[1:0]  |   | out1_mux_cfg[3:0] |   |   |            |
| Bit   | Name     | Description  |   |                   |   |   | Def. Value |
| 7   | out1_pdn | 0: Output divider not powered-down<br>1: Output divider powered-down |   |                   |   |   | 0          |



### Output 1 Mux Configuration Register

|  |                    |   |  |   |   |   |      |
|--|--------------------|---|--|---|---|---|------|
| Register (Abbrev): out1_mux_cnfg<br>Address: 0x300<br>Type: RW<br>Default Value: 0000_0000 |                    |   |  |   |   |   |      |
| 7  | 6                  | 5 | 4  | 3 | 2 | 1 | 0    |
| 6  | out1_inv           |   | 0: Output not inverted<br>1: Output inverted   |   |   |   | 0    |
| 5:4  | out1_squelch[1:0]  |   | 0x: no squelch<br>10: Squelch to 0<br>11: Squelch to 1   |   |   |   | 00   |
| 3:0  | out1_mux_cnfg[3:0] |   | 0000: APLL1<br>0011: DPLL1 25 MHz<br>0100: DPLL1 77.76 MHz<br>0101: DPLL1 12E1/GPS/E3/T3, dependent on <a href="#">dpll1 DPLL Path Configuration Register</a><br>0110: DPLL1 16E1/16T1<br>0111: DPLL1 GSM/OBSAI/16E1/16T1, dependent on <a href="#">dpll1 DPLL Path Configuration Register</a> register<br>Others: Reserved (do not use) |   |   |   | 0000 |

### Output 1 Divisor 1 Configuration Register [4:0]

|  |                     |   |  |   |   |   |            |
|--|---------------------|---|--|---|---|---|------------|
| Register (Abbrev): out1_div1_cnfg[4:0]<br>Address: 0x301<br>Type: RW<br>Default Value: 1001_1000 |                     |   |  |   |   |   |            |
| 7  | 6                   | 5 | 4  | 3 | 2 | 1 | 0          |
| out1_sync_en   | reserved            |   | out1_div1_cnfg[4:0]  |   |   |   |            |
| Bit  | Name                |   | Description  |   |   |   | Def. Value |
| 7  | out1_sync_en        |   | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync<br>1: Enable sync |   |   |   | 1          |
| 6:5  | reserved            |   | reserved   |   |   |   | 00         |
| 4:0  | out1_div1_cnfg[4:0] |   | N1, actual ratio is N1+1. out divider ratio config for N1, integer number from 1 to 2^5.                         |   |   |   | 1_1000     |

### Output 1 Divisor 2 Configuration Register [26:0]

| Register (Abbrev): out1_div2_cnfg[26:0]<br>Address: 0x302, 0x303, 0x304, 0x305<br>Type: RW<br>Default Value: 0000_0000 |                       |  |            |                       |   |   |   |
|--|-----------------------|--|------------|-----------------------|---|---|---|
| 7  | 6                     | 5  | 4          | 3                     | 2 | 1 | 0 |
| out1_div2_cnfg[7:0]  |                       |  |            |                       |   |   |   |
| out1_div2_cnfg[15:8]   |                       |  |            |                       |   |   |   |
| out1_div2_cnfg[23:16]  |                       |  |            |                       |   |   |   |
| reserved   |                       |  |            | out1_div2_cnfg[26:24] |   |   |   |
| Bit  | Name                  | Description  | Def. Value |                       |   |   |   |
| 7:0  | out1_div2_cnfg[7:0]   | out1_div2_cnfg[24:0]:N2, actual ratio is N2+1<br>out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> | 0000_0000  |                       |   |   |   |
|  | out1_div2_cnfg[15:8]  |  |            |                       |   |   |   |
|  | out1_div2_cnfg[23:16] |  |            |                       |   |   |   |
| 7:3  | reserved              | reserved   | 0000_0     |                       |   |   |   |
| 2:0  | out1_div2_cnfg[26:24] | out1_div2_cnfg[24:0]:N2, actual ratio is N2+1<br>out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> | 000        |                       |   |   |   |

### Output 1 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out1_ph1_cnfg[4:0]<br>Address: 0x306<br>Type: RW<br>Default Value: 0000_0000 |                    |  |            |                    |   |   |   |
|---|--------------------|--|------------|--------------------|---|---|---|
| 7   | 6                  | 5  | 4          | 3                  | 2 | 1 | 0 |
| reserved  |                    |  |            | out1_ph1_cnfg[4:0] |   |   |   |
| Bit   | Name               | Description  | Def. Value |                    |   |   |   |
| 7:5   | reserved           | reserved   | 000        |                    |   |   |   |
| 4:0   | out1_ph1_cnfg[4:0] | This value represents the first stage phase adjustment for OUT01. The output phase of OUT01 will be moved in a POSITIVE direction in an amount calculated by this value times the phase 1 quanta.<br>The phase 1 quanta is dependent on the configured output frequency passed to OUT01. The calculation is (1/FREQ). E.G.: If OUT01 is configured to use a frequency of 625 MHz from APLL1, the phase 1 quanta is (1/625) = 1.6ns. If this value were 10, the phase will be moved forward by 16ns (10*1.6). | 0_0000     |                    |   |   |   |

Output 1 Phase 2 Configuration Register [26:0]

| Register (Abbrev): out1_ph2_cnfg[26:0]<br>Address: 0x307, 0x308, 0x309, 0x30A<br>Type: RW<br>Default Value: 0000_0000 |                      |  |                      |   |   |   |   |
|---|----------------------|--|----------------------|---|---|---|---|
| 7   | 6                    | 5  | 4                    | 3 | 2 | 1 | 0 |
| out1_ph2_cnfg[7:0]  |                      |  |                      |   |   |   |   |
| out1_ph2_cnfg[15:8]   |                      |  |                      |   |   |   |   |
| out1_ph2_cnfg[23:16]  |                      |  |                      |   |   |   |   |
| reserved  |                      |  | out1_ph2_cnfg[26:24] |   |   |   |   |
| Bit   | Name                 | Description  | Def. Value           |   |   |   |   |
| 7:0   | out1_ph2_cnfg[7:0]   | This value represents the second stage phase adjustment for OUT01. The output phase of OUT01 will be moved in a POSITIVE direction in an amount calculated by this value times the phase 2 quanta. The phase 2 quanta is dependent on the configured output frequency passed to OUT01 and the divider specified in OUT01_DIV1_CNFG+1.. The calculation is (1/FREQ)(DIV1+1). E.G.: If OUT01 is configured to use a frequency of 625 MHz from APLL1 and OUT01_DIV_CNFG is set to 24, the phase 2 quanta is (1/625)/24 = 40ns. If this value were 5, the phase will be moved forward by 200ns (5*40). | 0000_0000            |   |   |   |   |
|   | out1_ph2_cnfg[15:8]  |  |                      |   |   |   |   |
|   | out1_ph2_cnfg[23:16] |  |                      |   |   |   |   |
| 7:5   | reserved             | reserved   | 000                  |   |   |   |   |
| 4:0   | out1_ph2_cnfg[26:24] | This value represents the second stage phase adjustment for OUT01. The output phase of OUT01 will be moved in a POSITIVE direction in an amount calculated by this value times the phase 2 quanta. The phase 2 quanta is dependent on the configured output frequency passed to OUT01 and the divider specified in OUT01_DIV1_CNFG+1.. The calculation is (1/FREQ)(DIV1+1). E.G.: If OUT01 is configured to use a frequency of 625 MHz from APLL1 and OUT01_DIV_CNFG is set to 24, the phase 2 quanta is (1/625)/24 = 40ns. If this value were 5, the phase will be moved forward by 200ns (5*40). | 0_0000               |   |   |   |   |

### Output 1 Fine Phase Configuration Register

| Register (Abbrev): out1_fine_ph_cfg<br>Address: 0x30B<br>Type: RW<br>Default Value: 1100_0000 |                       |  |   |   |                       |   |            |
|---|-----------------------|--|---|---|-----------------------|---|------------|
| 7   | 6                     | 5  | 4 | 3 | 2                     | 1 | 0          |
| out1_pulse_cfg[1:0]   |                       | reserved   |   |   | out1_fine_ph_cfg[2:0] |   |            |
| Bit   | Name                  | Description  |   |   |                       |   | Def. Value |
| 7:6   | out1_pulse_cfg[1:0]   | Output pulse configure for 1 PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                       |   | 11         |
| 5:3   | reserved              | reserved   |   |   |                       |   | 00_0       |
| 2:0   | out1_fine_ph_cfg[2:0] | Fine phase adjustment. step size equals to 1/2 of VCO period.  |   |   |                       |   | 000        |

### Output 2 Mux Configuration Register

| Register (Abbrev): out2_mux_cfg<br>Address: 0x30C<br>Type: RW<br>Default Value: 0000_0000 |                   |  |   |          |   |   |            |
|---|-------------------|--|---|----------|---|---|------------|
| 7   | 6                 | 5  | 4 | 3        | 2 | 1 | 0          |
| reserved  | out2_inv          | out2_squelch[1:0]  |   | reserved |   |   | out2_pdn   |
| Bit   | Name              | Description  |   |          |   |   | Def. Value |
| 7   | reserved          | reserved   |   |          |   |   | 0          |
| 6   | out2_inv          | 0: Output not inverted<br>1: Output inverted                         |   |          |   |   | 0          |
| 5:4   | out2_squelch[1:0] | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1               |   |          |   |   | 00_0       |
| 3:1   | reserved          | reserved   |   |          |   |   | 000        |
| 0   | out2_pdn          | 0: Output divider not powered-down<br>1: Output divider powered-down |   |          |   |   | 0          |

Output 2 Divisor 1 Configuration Register [4:0]

| Register (Abbrev): out2_div1_cnfg[4:0]<br>Address: 0x30D<br>Type: RW<br>Default Value: 1000_0100 |                     |  |                     |   |   |   |            |
|--|---------------------|--|---------------------|---|---|---|------------|
| 7  | 6                   | 5  | 4                   | 3 | 2 | 1 | 0          |
| out2_sync_en   | reserved            |  | out2_div1_cnfg[4:0] |   |   |   |            |
| Bit  | Name                | Description  |                     |   |   |   | Def. Value |
| 7  | out2_sync_en        | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync<br>1: Enable sync |                     |   |   |   | 1          |
| 6:5  | reserved            | reserved   |                     |   |   |   | 00         |
| 4:0  | out2_div1_cnfg[4:0] | N1, actual ratio is N1+1. out divider ratio config for N1, integer number from 1 to 2 <sup>5</sup> .             |                     |   |   |   | 0_0100     |

Output 2 Divisor 2 Configuration Register [26:0]

| Register (Abbrev): out2_div2_cnfg[26:0]<br>Address: 0x30E, 0x30F, 0x310, 0x311<br>Type: RW<br>Default Value: 0000_0000 |                       |   |   |                       |   |   |            |
|--|-----------------------|---|---|-----------------------|---|---|------------|
| 7  | 6                     | 5   | 4 | 3                     | 2 | 1 | 0          |
| out2_div2_cnfg[7:0]  |                       |   |   |                       |   |   |            |
| out2_div2_cnfg[15:8]   |                       |   |   |                       |   |   |            |
| out2_div2_cnfg[23:16]  |                       |   |   |                       |   |   |            |
| reserved   |                       |   |   | out2_div2_cnfg[26:24] |   |   |            |
| Bit  | Name                  | Description   |   |                       |   |   | Def. Value |
| 7:0  | out2_div2_cnfg[7:0]   | N2, actual ratio is N2+1. out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |                       |   |   | 0000_0000  |
|  | out2_div2_cnfg[15:8]  |   |   |                       |   |   |            |
|  | out2_div2_cnfg[23:16] |   |   |                       |   |   |            |
| 7:3  | reserved              | reserved  |   |                       |   |   | 0000_0     |
| 2:0  | out2_div2_cnfg[26:24] | N2, actual ratio is N2+1. out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |                       |   |   | 000        |

### Output 2 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out2_ph1_cnfg[4:0]<br>Address: 0x312<br>Type: RW<br>Default Value: 0000_0000 |                    |   |                    |   |   |   |            |
|---|--------------------|---|--------------------|---|---|---|------------|
| 7   | 6                  | 5   | 4                  | 3 | 2 | 1 | 0          |
| reserved  |                    |   | out2_ph1_cnfg[4:0] |   |   |   |            |
| Bit   | Name               | Description   |                    |   |   |   | Def. Value |
| 7:5   | reserved           | reserved  |                    |   |   |   | 000        |
| 4:0   | out2_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not be larger than the number in the <a href="#">Output 2 Divisor 1 Configuration Register [4:0]</a> . |                    |   |   |   | 0_0000     |

### Output 2 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out2_ph2_cnfg[7:0]<br>Address: 0x313<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0          |
| out2_ph2_cnfg[7:0]  |                    |  |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   | Def. Value |
| 7:0   | out2_ph2_cnfg[7:0] | out2_ph2_cnfg[24:0]: Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in the <a href="#">Output 2 Divisor 2 Configuration Register [26:0]</a> . |   |   |   |   | 0000_0000  |

### Output 2 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out2_ph2_cnfg[15:8]<br>Address: 0x314<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0          |
| out2_ph2_cnfg[15:8]  |                     |  |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   | Def. Value |
| 7:0  | out2_ph2_cnfg[15:8] | out2_ph2_cnfg[24:0]: Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in the <a href="#">Output 2 Divisor 2 Configuration Register [26:0]</a> . |   |   |   |   | 0000_0000  |

### Output 2 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out2_ph2_cfg[23:16]<br>Address: 0x315<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|--|---------------------|---|---|---|---|---|------------|
| 7  | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out2_ph2_cfg[23:16]  |                     |   |   |   |   |   |            |
| Bit  | Name                | Description   |   |   |   |   | Def. Value |
| 7:0  | out2_ph2_cfg[23:16] | out2_ph2_cfg[24:0]: Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in the <a href="#">Output 2 Divisor 2 Configuration Register [26:0]</a> . |   |   |   |   | 0000_0000  |

### Output 2 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out2_ph2_cfg[26:24]<br>Address: 0x316<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |                     |   |            |
|--|---------------------|--|---|---|---------------------|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2                   | 1 | 0          |
| reserved   |                     |  |   |   | out2_ph2_cfg[26:24] |   |            |
| Bit  | Name                | Description  |   |   |                     |   | Def. Value |
| 7:3  | reserved            | reserved   |   |   |                     |   | 0000_0     |
| 2:0  | out2_ph2_cfg[26:24] | out2_ph2_cfg[24:0]: phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not larger than the number in the <a href="#">Output 2 Divisor 2 Configuration Register [26:0]</a> . |   |   |                     |   | 000        |

### Output 2 Fine Phase Configuration Register

| Register (Abbrev): out2_fine_ph_cfg<br>Address: 0x317<br>Type: RW<br>Default Value: 1100_0000 |                   |  |   |   |                       |   |            |
|---|-------------------|--|---|---|-----------------------|---|------------|
| 7   | 6                 | 5  | 4 | 3 | 2                     | 1 | 0          |
| out2_pulse_cfg[1:0]   |                   | reserved   |   |   | out2_fine_ph_cfg[2:0] |   |            |
| Bit   | Name              | Description  |   |   |                       |   | Def. Value |
| 7:6   | out2_ph2_cfg[7:0] | Output pulse configure for 1 PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                       |   | 11         |

### Output 2 Fine Phase Configuration Register

|   |                       |   |   |   |   |      |   |
|---|-----------------------|---|---|---|---|------|---|
| Register (Abbrev): out2_fine_ph_cfg<br>Address: 0x317<br>Type: RW<br>Default Value: 1100_0000 |                       |   |   |   |   |      |   |
| 7   | 6                     | 5 | 4   | 3 | 2 | 1    | 0 |
| 5:3   | reserved              |   | reserved  |   |   | 00_0 |   |
| 2:0   | out2_fine_ph_cfg[2:0] |   | Fine phase adjustment. Step size equals to 1/2 of VCO period. |   |   | 000  |   |

### Output 3 Mux Configuration Register

| Register (Abbrev): out3_mux_cfg<br>Address: 0x318<br>Type: RW<br>Default Value: 0000_0000 |                   |  |   |          |   |              |            |
|---|-------------------|--|---|----------|---|--------------|------------|
| 7   | 6                 | 5  | 4 | 3        | 2 | 1            | 0          |
| lvds_pecl   | out3_inv          | out3_squelch[1:0]  |   | reserved |   | out3_pad_pdn | out3_pdn   |
| Bit   | Name              | Description  |   |          |   |              | Def. Value |
| 7   | lvds_pecl         | 0: LVDS mode output<br>1: PECL mode output                           |   |          |   |              | 0          |
| 6   | out3_inv          | 0: Output not inverted<br>1: Output inverted                         |   |          |   |              | 0          |
| 5:4   | out3_squelch[1:0] | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1               |   |          |   |              | 00         |
| 3:2   | reserved          | reserved   |   |          |   |              | 00         |
| 1   | out3_pad_pdn      | 0: Output pad not powered-down<br>1: Output pad powered-down         |   |          |   |              | 0          |
| 0   | out3_pdn          | 0: Output divider not powered-down<br>1: Output divider powered-down |   |          |   |              | 0          |



Output 3 Divisor 1 Configuration Register [4:0]

| Register (Abbrev): out3_div1_cnfg[4:0]<br>Address: 0x319<br>Type: RW<br>Default Value: 1000_0011 |                     |  |                     |   |   |   |            |
|--|---------------------|--|---------------------|---|---|---|------------|
| 7  | 6                   | 5  | 4                   | 3 | 2 | 1 | 0          |
| out3_sync_en   | reserved            |  | out3_div1_cnfg[4:0] |   |   |   |            |
| Bit  | Name                | Description  |                     |   |   |   | Def. Value |
| 7  | out3_sync_en        | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync.<br>1: Enable sync.       |                     |   |   |   | 1          |
| 6:5  | reserved            | reserved   |                     |   |   |   | 00         |
| 4:0  | out3_div1_cnfg[4:0] | out3_div1_cnfg[4:0]:N1, actual ratio is N1+1<br>out divider ratio config for N1, integer number from 1 to 2 <sup>5</sup> |                     |   |   |   | 0_0011     |

Output 3 Divisor 2 Configuration Register [7:0]

| Register (Abbrev): out3_div2_cnfg[7:0]<br>Address: 0x31A<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|--|---------------------|---|---|---|---|---|------------|
| 7  | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out3_div2_cnfg[7:0]  |                     |   |   |   |   |   |            |
| Bit  | Name                | Description   |   |   |   |   | Def. Value |
| 7:0  | out3_div2_cnfg[7:0] | N2, actual ratio is N2+1<br>out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> |   |   |   |   | 0000_0000  |

Output 3 Divisor 2 Configuration Register [15:8]

| Register (Abbrev): out3_div2_cnfg[15:8]<br>Address: 0x31B<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |   |   |            |
|---|----------------------|---|---|---|---|---|------------|
| 7   | 6                    | 5   | 4 | 3 | 2 | 1 | 0          |
| out3_div2_cnfg[15:8]  |                      |   |   |   |   |   |            |
| Bit   | Name                 | Description   |   |   |   |   | Def. Value |
| 7:0   | out3_div2_cnfg[15:8] | N2, actual ratio is N2+1<br>out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> |   |   |   |   | 0000_0000  |

### Output 3 Divisor 2 Configuration Register [23:16]

| Register (Abbrev): out3_div2_cnfg[23:16]<br>Address: 0x31C<br>Type: RW<br>Default Value: 0000_0000 |                       |   |   |   |   |   |   |            |
|--|-----------------------|---|---|---|---|---|---|------------|
| 7  | 6                     | 5   | 4 | 3 | 2 | 1 | 0 |            |
| out3_div2_cnfg[23:16]  |                       |   |   |   |   |   |   |            |
| Bit  | Name                  | Description   |   |   |   |   |   | Def. Value |
| 7:0  | out3_div2_cnfg[23:16] | N2, actual ratio is N2+1<br>out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> |   |   |   |   |   | 0000_0000  |

### Output 3 Divisor 2 Configuration Register [26:24]

| Register (Abbrev): out3_div2_cnfg[26:24]<br>Address: 0x31D<br>Type: RW<br>Default Value: 0000_0000 |                       |   |   |   |                       |   |   |            |
|--|-----------------------|---|---|---|-----------------------|---|---|------------|
| 7  | 6                     | 5   | 4 | 3 | 2                     | 1 | 0 |            |
| reserved   |                       |   |   |   | out3_div2_cnfg[26:24] |   |   |            |
| Bit  | Name                  | Description   |   |   |                       |   |   | Def. Value |
| 7:3  | reserved              | reserved  |   |   |                       |   |   | 0000_0     |
| 2:0  | out3_div2_cnfg[26:24] | N2, actual ratio is N2+1<br>out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> |   |   |                       |   |   | 000        |

### Output 3 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out3_ph1_cnfg[4:0]<br>Address: 0x31E<br>Type: RW<br>Default Value: 0000_0000 |                    |  |                    |   |   |   |   |            |
|---|--------------------|--|--------------------|---|---|---|---|------------|
| 7   | 6                  | 5  | 4                  | 3 | 2 | 1 | 0 |            |
| reserved  |                    |  | out3_ph1_cnfg[4:0] |   |   |   |   |            |
| Bit   | Name               | Description  |                    |   |   |   |   | Def. Value |
| 7:5   | reserved           | reserved   |                    |   |   |   |   | 000        |
| 4:0   | out3_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not be larger than the number in out3_div1_cnfg[4:0]. |                    |   |   |   |   |            |

### Output 3 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out3_ph2_cfg[7:0]<br>Address: 0x31F<br>Type: RW<br>Default Value: 0000_0000 |                   |  |   |   |   |   |            |
|--|-------------------|--|---|---|---|---|------------|
| 7  | 6                 | 5  | 4 | 3 | 2 | 1 | 0          |
| out3_ph2_cfg[7:0]  |                   |  |   |   |   |   |            |
| Bit  | Name              | Description  |   |   |   |   | Def. Value |
| 7:0  | out3_ph2_cfg[7:0] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out3_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 3 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out3_ph2_cfg[15:8]<br>Address: 0x320<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0          |
| out3_ph2_cfg[15:8]  |                    |  |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   | Def. Value |
| 7:0   | out3_ph2_cfg[15:8] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out3_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 3 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out3_ph2_cfg[23:16]<br>Address: 0x321<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0          |
| out3_ph2_cfg[23:16]  |                     |  |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   | Def. Value |
| 7:0  | out3_ph2_cfg[23:16] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out3_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 3 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out3_ph2_cfg[26:24]<br>Address: 0x322<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |                     |   |   |            |
|--|---------------------|--|---|---------------------|---|---|------------|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1 | 0          |
| reserved   |                     |  |   | out3_ph2_cfg[26:24] |   |   |            |
| Bit  | Name                | Description  |   |                     |   |   | Def. Value |
| 7:3  | reserved            | reserved   |   |                     |   |   | 0000_0     |
| 2:0  | out3_ph2_cfg[26:24] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out3_div2_cfg[24:0]. |   |                     |   |   | 000        |

### Output 3 Fine Phase Configuration Register

| Register (Abbrev): out3_fine_ph_cfg<br>Address: 0x323<br>Type: RW<br>Default Value: 1100_0000 |                       |   |   |   |                       |   |            |
|---|-----------------------|---|---|---|-----------------------|---|------------|
| 7   | 6                     | 5   | 4 | 3 | 2                     | 1 | 0          |
| out3_pulse_cfg[1:0]   |                       | reserved  |   |   | out3_fine_ph_cfg[2:0] |   |            |
| Bit   | Name                  | Description   |   |   |                       |   | Def. Value |
| 7:6   | out3_pulse_cfg[1:0]   | Output pulse configure for 1PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                       |   | 11         |
| 5:3   | reserved              | reserved  |   |   |                       |   | 00_0       |
| 2:0   | out3_fine_ph_cfg[2:0] | Fine phase adjustment. Step size equals to 1/2 of VCO period.   |   |   |                       |   | 000        |

### Output 4 Mux Configuration Register

| Register (Abbrev): out4_mux_cfg<br>Address: 0x324<br>Type: RW<br>Default Value: 0010_0000 |           |  |   |          |   |              |            |
|---|-----------|--|---|----------|---|--------------|------------|
| 7   | 6         | 5  | 4 | 3        | 2 | 1            | 0          |
| lvds_pecl   | out4_inv  | out4_sqelch[1:0]                           |   | reserved |   | out4_pad_pdn | out4_pdn   |
| Bit   | Name      | Description                                |   |          |   |              | Def. Value |
| 7   | lvds_pecl | 0: LVDS mode output<br>1: PECL mode output |   |          |   |              | 0          |

Output 4 Mux Configuration Register

|  |                   |   |  |   |   |   |    |
|--|-------------------|---|--|---|---|---|----|
| Register (Abbrev): out4_mux_cnfg<br>Address: 0x324<br>Type: RW<br>Default Value: 0010_0000 |                   |   |  |   |   |   |    |
| 7  | 6                 | 5 | 4  | 3 | 2 | 1 | 0  |
| 6  | out4_inv          |   | 0: Output not inverted<br>1: Output inverted                         |   |   |   | 0  |
| 5:4  | out4_squelch[1:0] |   | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1               |   |   |   | 10 |
| 3:2  | reserved          |   | reserved   |   |   |   | 00 |
| 1  | out4_pad_pdn      |   | 0: Output pad not powered-down<br>1: Output pad powered-down         |   |   |   | 0  |
| 0  | out4_pdn          |   | 0: Output divider not powered-down<br>1: Output divider powered-down |   |   |   | 0  |

Output 4 Divisor 1 Configuration Register [4:0]

| Register (Abbrev): out4_div1_cnfg[4:0]<br>Address: 0x325<br>Type: RW<br>Default Value: 1000_0100 |                    |   |  |   |   |   |            |
|--|--------------------|---|--|---|---|---|------------|
| 7  | 6                  | 5 | 4  | 3 | 2 | 1 | 0          |
| out4_sync_en   | reserved           |   | out4_div_cnfg[4:0]   |   |   |   |            |
| Bit  | Name               |   | Description  |   |   |   | Def. Value |
| 7  | out4_sync_en       |   | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync.<br>1: Enable sync. |   |   |   | 1          |
| 6:5  | reserved           |   | reserved   |   |   |   | 00         |
| 4:0  | out4_div_cnfg[4:0] |   | N1, actual ratio is N1+1. out divider ratio config for N1, integer number from 1 to 2^5.                           |   |   |   | 0_0100     |

Output 4 Divisor 2 Configuration Register [7:0]

| Register (Abbrev): out4_div2_cnfg[7:0]<br>Address: 0x326<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|--|--------------------|---|---|---|---|---|------------|
| 7  | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out4_div_cnfg[7:0]   |                    |   |   |   |   |   |            |
| Bit  | Name               | Description   |   |   |   |   | Def. Value |
| 7:0  | out4_div_cnfg[7:0] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

Output 4 Divisor 2 Configuration Register [15:8]

| Register (Abbrev): out4_div2_cnfg[15:8]<br>Address: 0x327<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|---|---------------------|---|---|---|---|---|------------|
| 7   | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out4_div_cnfg[15:8]   |                     |   |   |   |   |   |            |
| Bit   | Name                | Description   |   |   |   |   | Def. Value |
| 7:0   | out4_div_cnfg[15:8] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

Output 4 Divisor 2 Configuration Register [23:16]

| Register (Abbrev): out4_div2_cnfg[23:16]<br>Address: 0x328<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|--|---------------------|---|---|---|---|---|------------|
| 7  | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out4_div_cnfg[15:8]  |                     |   |   |   |   |   |            |
| Bit  | Name                | Description   |   |   |   |   | Def. Value |
| 7:0  | out4_div_cnfg[15:8] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

### Output 4 Divisor 2 Configuration Register [26:24]

| Register (Abbrev): out4_div2_cnfg[26:24]<br>Address: 0x329<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |                      |   |   |            |
|--|----------------------|---|---|----------------------|---|---|------------|
| 7  | 6                    | 5   | 4 | 3                    | 2 | 1 | 0          |
| reserved   |                      |   |   | out4_div_cnfg[26:24] |   |   |            |
| Bit  | Name                 | Description   |   |                      |   |   | Def. Value |
| 7:3  | reserved             | reserved  |   |                      |   |   | 0000_0     |
| 2:0  | out4_div_cnfg[26:24] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |                      |   |   | 000        |

### Output 4 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out4_ph1_cnfg[4:0]<br>Address: 0x32A<br>Type: RW<br>Default Value: 0000_0000 |                    |  |                    |   |   |   |            |
|---|--------------------|--|--------------------|---|---|---|------------|
| 7   | 6                  | 5  | 4                  | 3 | 2 | 1 | 0          |
| reserved  |                    |  | out4_ph1_cnfg[4:0] |   |   |   |            |
| Bit   | Name               | Description  |                    |   |   |   | Def. Value |
| 7:5   | reserved           | reserved   |                    |   |   |   | 000        |
| 4:0   | out4_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not be larger than the number in out4_div1_cnfg[4:0]. |                    |   |   |   | 0_0000     |

### Output 4 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out4_ph2_cnfg[7:0]<br>Address: 0x32B<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|---|--------------------|---|---|---|---|---|------------|
| 7   | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out4_ph2_cnfg[7:0]  |                    |   |   |   |   |   |            |
| Bit   | Name               | Description   |   |   |   |   | Def. Value |
| 7:0   | out4_ph2_cnfg[7:0] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out4_div2_cnfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 4 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out4_ph2_cfg[15:8]<br>Address: 0x32C<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0 |            |
| out4_ph2_cfg[15:8]  |                    |  |   |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   |   | Def. Value |
| 7:0   | out4_ph2_cfg[15:8] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out4_div2_cfg[24:0]. |   |   |   |   |   | 0000_0000  |

### Output 4 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out4_ph2_cfg[23:16]<br>Address: 0x32D<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0 |            |
| out4_ph2_cfg[23:16]  |                     |  |   |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   |   | Def. Value |
| 7:0  | out4_ph2_cfg[23:16] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out4_div2_cfg[24:0]. |   |   |   |   |   | 0000_0000  |

### Output 4 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out4_ph2_cfg[26:24]<br>Address: 0x32E<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |                     |   |   |            |
|--|---------------------|--|---|---|---------------------|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2                   | 1 | 0 |            |
| reserved   |                     |  |   |   | out4_ph2_cfg[26:24] |   |   |            |
| Bit  | Name                | Description  |   |   |                     |   |   | Def. Value |
| 7:3  | reserved            | reserved   |   |   |                     |   |   | 0000_0     |
| 2:0  | out4_ph2_cfg[26:24] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out4_div2_cfg[24:0]. |   |   |                     |   |   | 000        |



### Output 4 Fine Phase Configuration Register

| Register (Abbrev): out4_fine_ph_cfg<br>Address: 0x32F<br>Type: RW<br>Default Value: 1100_0000 |                     |  |   |   |                     |   |            |
|---|---------------------|--|---|---|---------------------|---|------------|
| 7   | 6                   | 5  | 4 | 3 | 2                   | 1 | 0          |
| out4_pulse_cfg[1:0]   |                     | reserved   |   |   | out4_fine_ph_cfg[2] |   |            |
| Bit   | Name                | Description  |   |   |                     |   | Def. Value |
| 7:6   | out4_pulse_cfg[1:0] | Output pulse configure for 1 PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                     |   | 11         |
| 5:3   | reserved            | reserved   |   |   |                     |   | 00_0       |
| 2:0   | out4_fine_ph_cfg[2] | Fine phase adjustment. Step size equals to 1/2 of VCO period.  |   |   |                     |   | 000        |

### Output 5 Mux Configuration Register

| Register (Abbrev): out5_mux_cfg<br>Address: 0x330<br>Type: RW<br>Default Value: 0010_0000 |                   |  |   |          |   |              |            |
|---|-------------------|--|---|----------|---|--------------|------------|
| 7   | 6                 | 5  | 4 | 3        | 2 | 1            | 0          |
| lvds_pecl   | out5_inv          | out5_squelch[1:0]  |   | reserved |   | out5_pad_pdn | out5_pdn   |
| Bit   | Name              | Description  |   |          |   |              | Def. Value |
| 7   | lvds_pecl         | 0: LVDS mode output<br>1: PECL mode output                           |   |          |   |              | 0          |
| 6   | out5_inv          | 0: Output not inverted<br>1: Output inverted                         |   |          |   |              | 0          |
| 5:4   | out5_squelch[1:0] | 10: Squelch to 0<br>11: Squelch to 1                                 |   |          |   |              | 10         |
| 3:2   | reserved          | reserved   |   |          |   |              | 00         |
| 1   | out5_pad_pdn      | 0: Output pad not powered-down<br>1: Output pad powered-down         |   |          |   |              | 0          |
| 0   | out5_pdn          | 0: Output divider not powered-down<br>1: Output divider powered-down |   |          |   |              | 0          |

### Output 5 Divisor 1 Configuration Register [4:0]

| Register (Abbrev): out5_div1_cnfg[4:0]<br>Address: 0x331<br>Type: RW<br>Default Value: 1000_0100 |                    |  |                    |   |   |   |            |
|--|--------------------|--|--------------------|---|---|---|------------|
| 7  | 6                  | 5  | 4                  | 3 | 2 | 1 | 0          |
| out5_sync_en   | reserved           |  | out5_div_cnfg[4:0] |   |   |   |            |
| Bit  | Name               | Description  |                    |   |   |   | Def. Value |
| 7  | out5_sync_en       | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync.<br>1: Enable sync. |                    |   |   |   | 1          |
| 6:5  | reserved           | reserved   |                    |   |   |   | 00         |
| 4:0  | out5_div_cnfg[4:0] | N1, actual ratio is N1+1. out divider ratio config for N1, integer number from 1 to 2 <sup>5</sup> .               |                    |   |   |   | 0_0100     |

### Output 5 Divisor 2 Configuration Register [7:0]

| Register (Abbrev): out5_div2_cnfg[7:0]<br>Address: 0x332<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|--|--------------------|---|---|---|---|---|------------|
| 7  | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out5_div_cnfg[7:0]   |                    |   |   |   |   |   |            |
| Bit  | Name               | Description   |   |   |   |   | Def. Value |
| 7:0  | out5_div_cnfg[7:0] | N2, actual ratio is N2+1. Uut divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

### Output 5 Divisor 2 Configuration Register [15:8]

| Register (Abbrev): out5_div2_cnfg[15:8]<br>Address: 0x333<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|---|---------------------|---|---|---|---|---|------------|
| 7   | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out5_div_cnfg[15:8]   |                     |   |   |   |   |   |            |
| Bit   | Name                | Description   |   |   |   |   | Def. Value |
| 7:0   | out5_div_cnfg[15:8] | N2, actual ratio is N2+1. Uut divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

### Output 5 Divisor 2 Configuration Register [23:16]

| Register (Abbrev): out5_div2_cnfg[23:16]<br>Address: 0x334<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |   |   |            |
|--|----------------------|---|---|---|---|---|------------|
| 7  | 6                    | 5   | 4 | 3 | 2 | 1 | 0          |
| out5_div_cnfg[23:16]   |                      |   |   |   |   |   |            |
| Bit  | Name                 | Description   |   |   |   |   | Def. Value |
| 7:0  | out5_div_cnfg[23:16] | N2, actual ratio is N2+1. Uut divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

### Output 5 Divisor 2 Configuration Register [26:24]

| Register (Abbrev): out5_div2_cnfg[26:24]<br>Address: 0x335<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |                      |   |   |            |
|--|----------------------|---|---|----------------------|---|---|------------|
| 7  | 6                    | 5   | 4 | 3                    | 2 | 1 | 0          |
| reserved   |                      |   |   | out5_div_cnfg[26:24] |   |   |            |
| Bit  | Name                 | Description   |   |                      |   |   | Def. Value |
| 7:3  | reserved             | reserved  |   |                      |   |   | 0000_0     |
| 2:0  | out5_div_cnfg[26:24] | N2, actual ratio is N2+1. Uut divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |                      |   |   | 000        |

### Output 5 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out5_ph1_cnfg[4:0]<br>Address: 0x336<br>Type: RW<br>Default Value: 0000_0000 |                    |  |                    |   |   |   |            |
|---|--------------------|--|--------------------|---|---|---|------------|
| 7   | 6                  | 5  | 4                  | 3 | 2 | 1 | 0          |
| reserved  |                    |  | out5_ph1_cnfg[4:0] |   |   |   |            |
| Bit   | Name               | Description  |                    |   |   |   | Def. Value |
| 7:5   | reserved           | reserved   |                    |   |   |   | 000        |
| 4:0   | out5_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not be larger than the number in out5_div1_cnfg[4:0]. |                    |   |   |   | 0_0000     |

### Output 5 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out5_ph2_cfg[7:0]<br>Address: 0x337<br>Type: RW<br>Default Value: 0000_0000 |                   |  |   |   |   |   |            |
|--|-------------------|--|---|---|---|---|------------|
| 7  | 6                 | 5  | 4 | 3 | 2 | 1 | 0          |
| out5_ph2_cfg[7:0]  |                   |  |   |   |   |   |            |
| Bit  | Name              | Description  |   |   |   |   | Def. Value |
| 7:0  | out5_ph2_cfg[7:0] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out5_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 5 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out5_ph2_cfg[15:8]<br>Address: 0x338<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0          |
| out5_ph2_cfg[15:8]  |                    |  |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   | Def. Value |
| 7:0   | out5_ph2_cfg[15:8] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out5_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 5 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out5_ph2_cfg[23:16]<br>Address: 0x339<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0          |
| out5_ph2_cfg[23:16]  |                     |  |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   | Def. Value |
| 7:0  | out5_ph2_cfg[23:16] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out5_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 5 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out5_ph2_cfg[26:24]<br>Address: 0x33A<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |                     |   |   |            |
|--|---------------------|--|---|---------------------|---|---|------------|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1 | 0          |
| reserved   |                     |  |   | out5_ph2_cfg[26:24] |   |   |            |
| Bit  | Name                | Description  |   |                     |   |   | Def. Value |
| 7:3  | reserved            | reserved   |   |                     |   |   | 0000_0     |
| 2:0  | out5_ph2_cfg[26:24] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out5_div2_cfg[24:0]. |   |                     |   |   | 000        |

### Output 5 Fine Phase Configuration Register

| Register (Abbrev): out5_fine_ph_cfg<br>Address: 0x33B<br>Type: RW<br>Default Value: 1100_0000 |                       |   |   |   |                       |   |            |
|---|-----------------------|---|---|---|-----------------------|---|------------|
| 7   | 6                     | 5   | 4 | 3 | 2                     | 1 | 0          |
| out5_pulse_cfg[1:0]   |                       | reserved  |   |   | out5_fine_ph_cfg[2:0] |   |            |
| Bit   | Name                  | Description   |   |   |                       |   | Def. Value |
| 7:6   | out5_pulse_cfg[1:0]   | Output pulse configure for 1PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                       |   | 11         |
| 5:3   | reserved              | reserved  |   |   |                       |   | 00_0       |
| 2:0   | out5_fine_ph_cfg[2:0] | Fine phase adjustment. Step size equals to 1/2 of VCO period.   |   |   |                       |   | 000        |

### Output 6 Mux Configuration Register

| Register (Abbrev): out6_mux_cfg<br>Address: 0x33C<br>Type: RW<br>Default Value: 0010_0000 |           |  |   |          |   |              |            |
|---|-----------|--|---|----------|---|--------------|------------|
| 7   | 6         | 5  | 4 | 3        | 2 | 1            | 0          |
| lvds_pecl   | out6_inv  | out6_sqelch[1:0]                           |   | reserved |   | out6_pad_pdn | out6_pdn   |
| Bit   | Name      | Description                                |   |          |   |              | Def. Value |
| 7   | lvds_pecl | 0: LVDS mode output<br>1: PECL mode output |   |          |   |              | 0          |

### Output 6 Mux Configuration Register

|  |                   |   |  |   |   |   |    |
|--|-------------------|---|--|---|---|---|----|
| Register (Abbrev): out6_mux_cnfg<br>Address: 0x33C<br>Type: RW<br>Default Value: 0010_0000 |                   |   |  |   |   |   |    |
| 7  | 6                 | 5 | 4  | 3 | 2 | 1 | 0  |
| 6  | out6_inv          |   | 0: Output not inverted<br>1: Output inverted                         |   |   |   | 0  |
| 5:4  | out6_squelch[1:0] |   | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1               |   |   |   | 10 |
| 3:2  | reserved          |   | reserved   |   |   |   | 00 |
| 1  | out6_pad_pdn      |   | 0: Output pad not powered-down<br>1: Output pad powered-down         |   |   |   | 0  |
| 0  | out6_pdn          |   | 0: Output divider not powered-down<br>1: Output divider powered-down |   |   |   | 0  |

### Output 6 Divisor 1 Configuration Register [7:0]

| Register (Abbrev): out6_div1_cnfg[7:0]<br>Address: 0x33D<br>Type: RW<br>Default Value: 0000_0000 |                    |   |  |   |   |   |            |
|--|--------------------|---|--|---|---|---|------------|
| 7  | 6                  | 5 | 4  | 3 | 2 | 1 | 0          |
| out6_sync_en   | reserved           |   | out6_div_cnfg[4:0]   |   |   |   |            |
| Bit  | Name               |   | Description  |   |   |   | Def. Value |
| 7  | out6_sync_en       |   | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync.<br>1: Enable sync. |   |   |   |            |
| 6:5  | reserved           |   | reserved   |   |   |   | 00         |
| 4:0  | out6_div_cnfg[4:0] |   | N1, actual ratio is N1+1. Out divider ratio config for N1, integer number from 1 to 2^5.                           |   |   |   |            |

Output 6 Divisor 2 Configuration Register [7:0]

| Register (Abbrev): out6_div2_cnfg[7:0]<br>Address: 0x33E<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|--|--------------------|---|---|---|---|---|------------|
| 7  | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out6_div_cnfg[7:0]   |                    |   |   |   |   |   |            |
| Bit  | Name               | Description   |   |   |   |   | Def. Value |
| 7:0  | out6_div_cnfg[7:0] | N2, actual ratio is N2+1. out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

Output 6 Divisor 2 Configuration Register [15:8]

| Register (Abbrev): out6_div2_cnfg[15:8]<br>Address: 0x33F<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|---|---------------------|---|---|---|---|---|------------|
| 7   | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out6_div_cnfg[15:8]   |                     |   |   |   |   |   |            |
| Bit   | Name                | Description   |   |   |   |   | Def. Value |
| 7:0   | out6_div_cnfg[15:8] | N2, actual ratio is N2+1. out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

Output 6 Divisor 2 Configuration Register [23:16]

| Register (Abbrev): out6_div2_cnfg[23:16]<br>Address: 0x340<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |   |   |            |
|--|----------------------|---|---|---|---|---|------------|
| 7  | 6                    | 5   | 4 | 3 | 2 | 1 | 0          |
| out6_div_cnfg[23:16]   |                      |   |   |   |   |   |            |
| Bit  | Name                 | Description   |   |   |   |   | Def. Value |
| 7:0  | out6_div_cnfg[23:16] | N2, actual ratio is N2+1. out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

### Output 6 Divisor 2 Configuration Register [26:24]

| Register (Abbrev): out6_div2_cnfg[26:24]<br>Address: 0x341<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |                      |   |   |            |
|--|----------------------|---|---|----------------------|---|---|------------|
| 7  | 6                    | 5   | 4 | 3                    | 2 | 1 | 0          |
| reserved   |                      |   |   | out6_div_cnfg[26:24] |   |   |            |
| Bit  | Name                 | Description   |   |                      |   |   | Def. Value |
| 7:3  | reserved             | reserved  |   |                      |   |   | 00         |
| 2:0  | out6_div_cnfg[26:24] | N2, actual ratio is N2+1. out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |                      |   |   | 00_0000    |

### Output 6 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out6_ph1_cnfg[4:0]<br>Address: 0x342<br>Type: RW<br>Default Value: 0000_0000 |                    |  |                    |   |   |   |            |
|---|--------------------|--|--------------------|---|---|---|------------|
| 7   | 6                  | 5  | 4                  | 3 | 2 | 1 | 0          |
| reserved  |                    |  | out6_ph1_cnfg[4:0] |   |   |   |            |
| Bit   | Name               | Description  |                    |   |   |   | Def. Value |
| 7:5   | reserved           | reserved   |                    |   |   |   | 00         |
| 4:0   | out6_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not be larger than the number in out6_div1_cnfg[4:0]. |                    |   |   |   | 00_0000    |

### Output 6 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out6_ph2_cnfg[7:0]<br>Address: 0x343<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|---|--------------------|---|---|---|---|---|------------|
| 7   | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out6_ph2_cnfg[7:0]  |                    |   |   |   |   |   |            |
| Bit   | Name               | Description   |   |   |   |   | Def. Value |
| 7:0   | out6_ph2_cnfg[7:0] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in out6_div2_cnfg[24:0] |   |   |   |   | 0000_0000  |



### Output 6 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out6_ph2_cfg[15:8]<br>Address: 0x344<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0          |
| out6_ph2_cfg[15:8]  |                    |  |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   | Def. Value |
| 7:0   | out6_ph2_cfg[15:8] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in out6_div2_cfg[24:0] |   |   |   |   | 0000_0000  |

### Output 6 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out6_ph2_cfg[23:16]<br>Address: 0x345<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0          |
| out6_ph2_cfg[23:16]  |                     |  |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   | Def. Value |
| 7:0  | out6_ph2_cfg[23:16] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in out6_div2_cfg[24:0] |   |   |   |   | 0000_0000  |

### Output 6 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out6_ph2_cfg[26:24]<br>Address: 0x346<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |                     |   |            |
|--|---------------------|--|---|---|---------------------|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2                   | 1 | 0          |
| reserved   |                     |  |   |   | out6_ph2_cfg[26:24] |   |            |
| Bit  | Name                | Description  |   |   |                     |   | Def. Value |
| 7:3  | reserved            | reserved   |   |   |                     |   | 00         |
| 2:0  | out6_ph2_cfg[26:24] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1 the number in this register should not be larger than the number in out6_div2_cfg[24:0] |   |   |                     |   | 00_0000    |

### Output 6 Fine Phase Configuration Register

| Register (Abbrev): out6_fine_ph_cfg<br>Address: 0x347<br>Type: RW<br>Default Value: 1100_0000 |                       |   |   |   |                       |   |            |
|---|-----------------------|---|---|---|-----------------------|---|------------|
| 7   | 6                     | 5   | 4 | 3 | 2                     | 1 | 0          |
| out6_pulse_cfg[1:0]   |                       | reserved  |   |   | out6_fine_ph_cfg[2:0] |   |            |
| Bit   | Name                  | Description   |   |   |                       |   | Def. Value |
| 7:6   | out6_pulse_cfg[1:0]   | Output pulse configure for 1PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                       |   | 11         |
| 5:3   | reserved              | reserved  |   |   |                       |   | 00         |
| 2:0   | out6_fine_ph_cfg[2:0] | Fine phase adjustment. Step size equals to 1/2 of VCO period.   |   |   |                       |   | 0000       |

### Output 7 Mux Configuration Register

| Register (Abbrev): out7_mux_cfg<br>Address: 0x348<br>Type: RW<br>Default Value: 0010_0000 |                   |  |   |          |   |   |            |
|---|-------------------|--|---|----------|---|---|------------|
| 7   | 6                 | 5  | 4 | 3        | 2 | 1 | 0          |
| reserved  | out7_inv          | out7_squelch[1:0]  |   | reserved |   |   | out7_pdn   |
| Bit   | Name              | Description  |   |          |   |   | Def. Value |
| 7   | reserved          | reserved   |   |          |   |   | 00         |
| 6   | out7_inv          | 0: Output not inverted<br>1: Output inverted                         |   |          |   |   | 1          |
| 5:4   | out7_squelch[1:0] | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1               |   |          |   |   | 00         |
| 3:1   | reserved          | reserved   |   |          |   |   | 000        |
| 0   | out7_pdn          | 0: Output divider not powered-down<br>1: Output divider powered-down |   |          |   |   | 0          |

Output 7 Divisor 1 Configuration Register [7:0]

| Register (Abbrev): out7_div1_cnfg[7:0]<br>Address: 0x349<br>Type: RW<br>Default Value: 1000_0100 |                  |  |                  |   |   |   |            |
|--|------------------|--|------------------|---|---|---|------------|
| 7  | 6                | 5  | 4                | 3 | 2 | 1 | 0          |
| out7_sync_en   | reserved         |  | out7_div_cnfg[4] |   |   |   |            |
| Bit  | Name             | Description  |                  |   |   |   | Def. Value |
| 7  | out7_sync_en     | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync.<br>1: Enable sync. |                  |   |   |   | 1          |
| 6:5  | reserved         | reserved   |                  |   |   |   | 00         |
| 4:0  | out7_div_cnfg[4] | N1, actual ratio is N1+1. out divider ratio config for N1, integer number from 1 to 2 <sup>5</sup> .               |                  |   |   |   | 0_0100     |

Output 7 Divisor 2 Configuration Register [7:0]

| Register (Abbrev): out7_div2_cnfg[7:0]<br>Address: 0x34A<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|--|--------------------|---|---|---|---|---|------------|
| 7  | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out7_div_cnfg[7:0]   |                    |   |   |   |   |   |            |
| Bit  | Name               | Description   |   |   |   |   | Def. Value |
| 7:0  | out7_div_cnfg[7:0] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

Output 7 Divisor 2 Configuration Register [15:8]

| Register (Abbrev): out7_div2_cnfg[15:8]<br>Address: 0x34B<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|---|---------------------|---|---|---|---|---|------------|
| 7   | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out7_div_cnfg[15:8]   |                     |   |   |   |   |   |            |
| Bit   | Name                | Description   |   |   |   |   | Def. Value |
| 7:0   | out7_div_cnfg[15:8] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

### Output 7 Divisor 2 Configuration Register [23:16]

| Register (Abbrev): out7_div2_cnfg[23:16]<br>Address: 0x34C<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |   |   |   |            |
|--|----------------------|---|---|---|---|---|---|------------|
| 7  | 6                    | 5   | 4 | 3 | 2 | 1 | 0 |            |
| out7_div_cnfg[23:16]   |                      |   |   |   |   |   |   |            |
| Bit  | Name                 | Description   |   |   |   |   |   | Def. Value |
| 7:0  | out7_div_cnfg[23:16] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   |   | 0000_0000  |

### Output 7 Divisor 2 Configuration Register [26:24]

| Register (Abbrev): out7_div2_cnfg[26:24]<br>Address: 0x34D<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |                      |   |   |            |
|--|----------------------|---|---|---|----------------------|---|---|------------|
| 7  | 6                    | 5   | 4 | 3 | 2                    | 1 | 0 |            |
| reserved   |                      |   |   |   | out7_div_cnfg[26:24] |   |   |            |
| Bit  | Name                 | Description   |   |   |                      |   |   | Def. Value |
| 7:3  | reserved             | reserved  |   |   |                      |   |   | 0000_0     |
| 2:0  | out7_div_cnfg[26:24] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |                      |   |   | 000        |

### Output 7 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out7_ph1_cnfg[4:0]<br>Address: 0x34E<br>Type: RW<br>Default Value: 0000_0000 |                    |  |                    |   |   |   |   |            |
|---|--------------------|--|--------------------|---|---|---|---|------------|
| 7   | 6                  | 5  | 4                  | 3 | 2 | 1 | 0 |            |
| reserved  |                    |  | out7_ph1_cnfg[4:0] |   |   |   |   |            |
| Bit   | Name               | Description  |                    |   |   |   |   | Def. Value |
| 7:5   | reserved           | reserved   |                    |   |   |   |   | 000        |
| 4:0   | out7_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not be larger than the number in out7_div1_cnfg[4:0]. |                    |   |   |   |   | 0_0000     |

### Output 7 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out7_ph2_cfg[7:0]<br>Address: 0x34F<br>Type: RW<br>Default Value: 0000_0000 |                   |  |   |   |   |   |            |
|--|-------------------|--|---|---|---|---|------------|
| 7  | 6                 | 5  | 4 | 3 | 2 | 1 | 0          |
| out7_ph2_cfg[7:0]  |                   |  |   |   |   |   |            |
| Bit  | Name              | Description  |   |   |   |   | Def. Value |
| 7:0  | out7_ph2_cfg[7:0] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. the number in this register should not be larger than the number in out7_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 7 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out7_ph2_cfg[15:8]<br>Address: 0x350<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0          |
| out7_ph2_cfg[15:8]  |                    |  |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   | Def. Value |
| 7:0   | out7_ph2_cfg[15:8] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. the number in this register should not be larger than the number in out7_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 7 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out7_ph2_cfg[23:16]<br>Address: 0x351<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0          |
| out7_ph2_cfg[23:16]  |                     |  |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   | Def. Value |
| 7:0  | out7_ph2_cfg[23:16] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. the number in this register should not be larger than the number in out7_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

### Output 7 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out7_ph2_cfg[26:24]<br>Address: 0x352<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |                     |   |   |            |
|--|---------------------|--|---|---------------------|---|---|------------|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1 | 0          |
| reserved   |                     |  |   | out7_ph2_cfg[26:24] |   |   |            |
| Bit  | Name                | Description  |   |                     |   |   | Def. Value |
| 7:3  | reserved            | reserved   |   |                     |   |   | 0000_0     |
| 2:0  | out7_ph2_cfg[26:24] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. the number in this register should not be larger than the number in out7_div2_cfg[24:0]. |   |                     |   |   | 000        |

### Output 7 Fine Phase Configuration Register

| Register (Abbrev): out7_fine_ph_cfg<br>Address: 0x353<br>Type: RW<br>Default Value: 1100_0000 |                       |  |   |   |                       |   |            |
|---|-----------------------|--|---|---|-----------------------|---|------------|
| 7   | 6                     | 5  | 4 | 3 | 2                     | 1 | 0          |
| out7_pulse_cfg[1:0]   |                       | reserved   |   |   | out7_fine_ph_cfg[2:0] |   |            |
| Bit   | Name                  | Description  |   |   |                       |   | Def. Value |
| 7:6   | out7_pulse_cfg[1:0]   | Output pulse configure for 1 PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                       |   | 11         |
| 5:3   | reserved              | reserved   |   |   |                       |   | 00_0       |
| 2:0   | out7_fine_ph_cfg[2:0] | Fine phase adjustment. Step size equals to 1/2 of VCO period.  |   |   |                       |   | 000        |

### Output 8 Mux Configuration Register

| Register (Abbrev): out8_mux_cfg<br>Address: 0x354<br>Type: RW<br>Default Value: 0010_0000 |          |  |   |                 |   |   |            |
|---|----------|--|---|-----------------|---|---|------------|
| 7   | 6        | 5  | 4 | 3               | 2 | 1 | 0          |
| out8_pdn  | out8_inv | out8_sqelch[1:0]   |   | out8_mux_cfg[3] |   |   |            |
| Bit   | Name     | Description  |   |                 |   |   | Def. Value |
| 7   | out8_pdn | 0: Output divider not powered-down<br>1: Output divider powered-down |   |                 |   |   | 0          |

Output 8 Mux Configuration Register

|  |                   |   |   |   |   |   |      |
|--|-------------------|---|---|---|---|---|------|
| Register (Abbrev): out8_mux_cnfg<br>Address: 0x354<br>Type: RW<br>Default Value: 0010_0000 |                   |   |   |   |   |   |      |
| 7  | 6                 | 5 | 4   | 3 | 2 | 1 | 0    |
| 6  | out8_inv          |   | 0: Output not inverted<br>1: Output inverted  |   |   |   | 0    |
| 5:4  | out8_squelch[1:0] |   | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1  |   |   |   | 10   |
| 3:0  | out8_mux_cnfg[3]  |   | 0000: APLL2<br>0011: DPLL1 25M<br>0100: DPLL1 77.76 MHz<br>0101: DPLL1 12E1/GPS/E3/T3, dependent on <a href="#">dpll1 DPLL Path Configuration Register</a> register<br>0110: DPLL1 16E1/16T1<br>0111: DPLL1 GSM/OBSAI/16E1/16T1, dependent on <a href="#">dpll1 DPLL Path Configuration Register</a><br>Others: Reserved (do not use) |   |   |   | 0000 |

Output 8 Divisor 1 Configuration Register [7:0]

|  |                    |   |  |   |   |   |            |
|--|--------------------|---|--|---|---|---|------------|
| Register (Abbrev): out8_div1_cnfg[7:0]<br>Address: 0x355<br>Type: RW<br>Default Value: 1001_1000 |                    |   |  |   |   |   |            |
| 7  | 6                  | 5 | 4  | 3 | 2 | 1 | 0          |
| out8_sync_en   | reserved           |   | out8_div_cnfg[4:0]   |   |   |   |            |
| Bit  | Name               |   | Description  |   |   |   | Def. Value |
| 7  | out8_sync_en       |   | Enables the 1 Hz synchronization of both the div1 and div2 output dividers.<br>0: Disable sync.<br>1: Enable sync. |   |   |   | 1          |
| 6:5  | reserved           |   | reserved   |   |   |   | 00         |
| 4:0  | out8_div_cnfg[4:0] |   | N1, actual ratio is N1+1. Out divider ratio config for N1, integer number from 1 to 2^5.                           |   |   |   | 1_1000     |

Output 8 Divisor 2 Configuration Register [7:0]

| Register (Abbrev): out8_div2_cnfg[7:0]<br>Address: 0x356<br>Type: RW<br>Default Value: 0001_0000 |                    |   |   |   |   |   |            |
|--|--------------------|---|---|---|---|---|------------|
| 7  | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out8_div_cnfg[7:0]   |                    |   |   |   |   |   |            |
| Bit  | Name               | Description   |   |   |   |   | Def. Value |
| 7:0  | out8_div_cnfg[7:0] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0001_0000  |

Output 8 Divisor Configuration Register [15:8]

| Register (Abbrev): out8_div2_cnfg[15:8]<br>Address: 0x357<br>Type: RW<br>Default Value: 0000_0000 |                     |   |   |   |   |   |            |
|---|---------------------|---|---|---|---|---|------------|
| 7   | 6                   | 5   | 4 | 3 | 2 | 1 | 0          |
| out8_div_cnfg[15:8]   |                     |   |   |   |   |   |            |
| Bit   | Name                | Description   |   |   |   |   | Def. Value |
| 7:0   | out8_div_cnfg[15:8] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |

Output 8 Divisor Configuration Register [23:16]

| Register (Abbrev): out8_div2_cnfg[23:16]<br>Address: 0x358<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |   |   |   |            |
|--|----------------------|---|---|---|---|---|------------|
| 7  | 6                    | 5   | 4 | 3 | 2 | 1 | 0          |
| out8_div_cnfg[23:16]   |                      |   |   |   |   |   |            |
| Bit  | Name                 | Description   |   |   |   |   | Def. Value |
| 7:0  | out8_div_cnfg[23:16] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |   |   |   | 0000_0000  |



### Output 8 Divisor 2 Configuration Register [26:24]

| Register (Abbrev): out8_div2_cnfg[26:24]<br>Address: 0x359<br>Type: RW<br>Default Value: 0000_0000 |                      |   |   |                      |   |   |            |
|--|----------------------|---|---|----------------------|---|---|------------|
| 7  | 6                    | 5   | 4 | 3                    | 2 | 1 | 0          |
| reserved   |                      |   |   | out8_div_cnfg[26:24] |   |   |            |
| Bit  | Name                 | Description   |   |                      |   |   | Def. Value |
| 7:3  | reserved             | reserved  |   |                      |   |   | 0000_0     |
| 2:0  | out8_div_cnfg[26:24] | N2, actual ratio is N2+1. Out divider ratio config for N2, integer number from 1 to 2 <sup>25</sup> . |   |                      |   |   | 000        |

### Output 8 Phase 1 Configuration Register [4:0]

| Register (Abbrev): out8_ph1_cnfg[4:0]<br>Address: 0x35A<br>Type: RW<br>Default Value: 0000_0000 |                    |  |                    |   |   |   |            |
|---|--------------------|--|--------------------|---|---|---|------------|
| 7   | 6                  | 5  | 4                  | 3 | 2 | 1 | 0          |
| reserved  |                    |  | out8_ph1_cnfg[4:0] |   |   |   |            |
| Bit   | Name               | Description  |                    |   |   |   | Def. Value |
| 7:5   | reserved           | reserved   |                    |   |   |   | 000        |
| 4:0   | out8_ph1_cnfg[4:0] | Phase adjustment configure of N1. The step size equals to the input clock period of N1. The number in this register should not larger be than the number in out8_div1_cnfg[4:0]. |                    |   |   |   | 0_0000     |

### Output 8 Phase 2 Configuration Register [7:0]

| Register (Abbrev): out8_ph2_cnfg[7:0]<br>Address: 0x35B<br>Type: RW<br>Default Value: 0000_0000 |                    |   |   |   |   |   |            |
|---|--------------------|---|---|---|---|---|------------|
| 7   | 6                  | 5   | 4 | 3 | 2 | 1 | 0          |
| out8_ph2_cnfg[7:0]  |                    |   |   |   |   |   |            |
| Bit   | Name               | Description   |   |   |   |   | Def. Value |
| 7:0   | out8_ph2_cnfg[7:0] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out8_div2_cnfg[24:0]. |   |   |   |   | 0000_0000  |

Output 8 Phase 2 Configuration Register [15:8]

| Register (Abbrev): out8_ph2_cfg[15:8]<br>Address: 0x35C<br>Type: RW<br>Default Value: 0000_0000 |                    |  |   |   |   |   |            |
|---|--------------------|--|---|---|---|---|------------|
| 7   | 6                  | 5  | 4 | 3 | 2 | 1 | 0          |
| out8_ph2_cfg[15:8]  |                    |  |   |   |   |   |            |
| Bit   | Name               | Description  |   |   |   |   | Def. Value |
| 7:0   | out8_ph2_cfg[15:8] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out8_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

Output 8 Phase 2 Configuration Register [23:16]

| Register (Abbrev): out8_ph2_cfg[23:16]<br>Address: 0x35D<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |   |   |   |            |
|--|---------------------|--|---|---|---|---|------------|
| 7  | 6                   | 5  | 4 | 3 | 2 | 1 | 0          |
| out8_ph2_cfg[23:16]  |                     |  |   |   |   |   |            |
| Bit  | Name                | Description  |   |   |   |   | Def. Value |
| 7:0  | out8_ph2_cfg[23:16] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out8_div2_cfg[24:0]. |   |   |   |   | 0000_0000  |

Output 8 Phase 2 Configuration Register [26:24]

| Register (Abbrev): out8_ph2_cfg[26:24]<br>Address: 0x35E<br>Type: RW<br>Default Value: 0000_0000 |                     |  |   |                     |   |   |            |
|--|---------------------|--|---|---------------------|---|---|------------|
| 7  | 6                   | 5  | 4 | 3                   | 2 | 1 | 0          |
| reserved   |                     |  |   | out8_ph2_cfg[26:24] |   |   |            |
| Bit  | Name                | Description  |   |                     |   |   | Def. Value |
| 7:3  | reserved            | reserved   |   |                     |   |   | 0000_0     |
| 2:0  | out8_ph2_cfg[26:24] | Phase adjustment of N2. The step size equals to the input clock period of N2 which is the output of N1. The number in this register should not be larger than the number in out8_div2_cfg[24:0]. |   |                     |   |   | 000        |

### Output 8 Fine Phase Configuration Register

| Register (Abbrev): out8_fine_ph_cnfg |                        |   |   |   |                        |   |            |
|--------------------------------------|------------------------|---|---|---|------------------------|---|------------|
| Address: 0x35F                       |                        |   |   |   |                        |   |            |
| Type: RW                             |                        |   |   |   |                        |   |            |
| Default Value: 1100_0000             |                        |   |   |   |                        |   |            |
| 7                                    | 6                      | 5   | 4 | 3 | 2                      | 1 | 0          |
| out8_pulse_cnfg[1:0]                 |                        | reserved  |   |   | out8_fine_ph_cnfg[2:0] |   |            |
| Bit                                  | Name                   | Description   |   |   |                        |   | Def. Value |
| 7:6                                  | out8_pulse_cnfg[1:0]   | Output pulse configure for 1PPS output, N1 should be set to 'd32, T equals to output clock period of N1 which is 128 VCO period.<br>00: 2 T<br>01: 20 T<br>10: 2000 T<br>11: 50% duty cycle |   |   |                        |   | 11         |
| 5:3                                  | reserved               | reserved  |   |   |                        |   | 00_0       |
| 2:0                                  | out8_fine_ph_cnfg[2:0] | Fine phase adjustment. Step size equals to 1/2 of VCO period.   |   |   |                        |   | 000        |

### Output 9 Frequency Configuration Register

| Register (Abbrev): out9_freq_cnfg |                  |   |              |           |          |   |               |
|-----------------------------------|------------------|---|--------------|-----------|----------|---|---------------|
| Address: 0x360                    |                  |   |              |           |          |   |               |
| Type: RW                          |                  |   |              |           |          |   |               |
| Default Value: 1000_0000          |                  |   |              |           |          |   |               |
| 7                                 | 6                | 5   | 4            | 3         | 2        | 1 | 0             |
| out9_pdn                          | out9_inv         | dpll2_input_fail  | ami_out_duty | 400hz_sel | reserved |   | out9_path_sel |
| Bit                               | Name             | Description   |              |           |          |   | Def. Value    |
| 7                                 | out9_pdn         | 0: Disable (output low)<br>1: Enable (see dpll2_input_fail)   |              |           |          |   | 1             |
| 6                                 | out9_inv         | 0: Not inverted<br>1: Inverted  |              |           |          |   | 0             |
| 5                                 | dpll2_input_fail | 0: out9 enable/disable depends on out_en only<br>1: out9 is disabled if dpll2 input failed.             |              |           |          |   | 0             |
| 4                                 | ami_out_duty     | 0: 50:50 duty cycle<br>1: 5:8 duty cycle  |              |           |          |   | 0             |
| 3                                 | 400hz_sel        | This bit defines the ami format on out9.<br>0: 64k + 8kHz<br>1: 64k + 8k + 400Hz                        |              |           |          |   | 0             |
| 2:1                               | reserved         | reserved  |              |           |          |   | 00            |
| 0                                 | out9_path_sel    | These bits select an input to OUT9.<br>0: The output of DPLL2 DPLL path<br>1: The output of DPLL1 path. |              |           |          |   | 0             |

### Output 10 Configuration Register

| Register (Abbrev): out10_cnfg<br>Address: 0x36C<br>Type: RW<br>Default Value: 1000_0000 |                  |   |   |          |   |   |            |
|---|------------------|---|---|----------|---|---|------------|
| 7   | 6                | 5   | 4 | 3        | 2 | 1 | 0          |
| out10_sync_en   | out_inv          | out_squelch[1:0]  |   | reserved |   |   |            |
| Bit   | Name             | Description   |   |          |   |   | Def. Value |
| 7   | out10_sync_en    | Enables the 1 Hz synchronization for the output divider.<br>0: Sync disabled<br>1: Sync enabled |   |          |   |   | 1          |
| 6   | out_inv          | 0: Output not inverted<br>1: Output inverted  |   |          |   |   | 0          |
| 5:4   | out_squelch[1:0] | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1  |   |          |   |   | 00         |
| 3:0   | reserved         | reserved  |   |          |   |   | 0000       |

### Output 10 Frequency Configuration Register [7:0]

| Register (Abbrev): out10_freq_cnfg[7:0]<br>Address: 0x36D<br>Type: RW<br>Default Value: 0000_0101 |                   |   |   |   |   |   |            |
|---|-------------------|---|---|---|---|---|------------|
| 7   | 6                 | 5   | 4 | 3 | 2 | 1 | 0          |
| out_div_cnfg[7:0]   |                   |   |   |   |   |   |            |
| Bit   | Name              | Description   |   |   |   |   | Def. Value |
| 7:0   | out_div_cnfg[7:0] | out divider ratio config, actual ratio is M+1<br>$f_{out} = f_{clk\_sdm} / (M+1)$<br>here, $f_{clk\_sdm} = N * 64kHz$ |   |   |   |   | 0000_0101  |

### Output 10 Frequency Configuration Register [14:8]

| Register (Abbrev): out10_freq_cnfg[14:8]<br>Address: 0x36E<br>Type: RW<br>Default Value: 0000_0000 |                     |             |   |   |                   |   |            |
|--|---------------------|-------------|---|---|-------------------|---|------------|
| 7  | 6                   | 5           | 4 | 3 | 2                 | 1 | 0          |
| reserved   | out_div_cnfg[14:10] |             |   |   | out_div_cnfg[9:8] |   |            |
| Bit  | Name                | Description |   |   |                   |   | Def. Value |
| 7  | reserved            | reserved    |   |   |                   |   | 0          |

### Output 10 Frequency Configuration Register [14:8]

|  |                     |   |  |   |   |   |      |
|--|---------------------|---|--|---|---|---|------|
| Register (Abbrev): out10_freq_cnfg[14:8]<br>Address: 0x36E<br>Type: RW<br>Default Value: 0000_0000 |                     |   |  |   |   |   |      |
| 7  | 6                   | 5 | 4  | 3 | 2 | 1 | 0    |
| 6:2  | out_div_cnfg[14:10] |   | out divider ratio config, actual ratio is M+1<br>f <sub>out</sub> = fclk_sdm/(M+1)<br>here, fclk_sdm = N*64kHz |   |   |   | 0000 |
| 1:0  | out_div_cnfg[9:8]   |   | out divider ratio config, actual ratio is M+1<br>f <sub>out</sub> = fclk_sdm/(M+1)<br>here, fclk_sdm = N*64kHz |   |   |   | 0000 |

### Output 11 Configuration Register

| Register (Abbrev): out11_cnfg<br>Address: 0x378<br>Type: RW<br>Default Value: 1000_0000 |                  |                  |   |          |   |   |            |
|---|------------------|------------------|---|----------|---|---|------------|
| 7   | 6                | 5                | 4   | 3        | 2 | 1 | 0          |
| out11_sync_en   | out_inv          | out_squelch[1:0] |   | reserved |   |   |            |
| Bit   | Name             |                  | Description   |          |   |   | Def. Value |
| 7   | out11_sync_en    |                  | Enables the 1 Hz synchronization for the output divider.<br>0: Disable sync.<br>1: Enable sync. |          |   |   | 1          |
| 6   | out_inv          |                  | 0: Output not inverted<br>1: Output inverted  |          |   |   | 0          |
| 5:4   | out_squelch[1:0] |                  | 0x: No squelch<br>10: Squelch to 0<br>11: Squelch to 1  |          |   |   | 00         |
| 3:0   | reserved         |                  | reserved  |          |   |   | 0000       |

### Output 11 Frequency Configuration Register [7:0]

| Register (Abbrev): out11_freq_cfg[7:0]<br>Address: 0x379<br>Type: RW<br>Default Value: 0010_1111 |                  |  |   |   |   |   |   |            |
|--|------------------|--|---|---|---|---|---|------------|
| 7  | 6                | 5  | 4 | 3 | 2 | 1 | 0 |            |
| out_div_cfg[7:0]   |                  |  |   |   |   |   |   |            |
| Bit  | Name             | Description  |   |   |   |   |   | Def. Value |
| 7:0  | out_div_cfg[7:0] | M. Out divider ratio config, actual ratio is M+1<br>$f_{out}=f_{clk\_sdm}/(M+1)$<br>here, $f_{clk\_sdm}=N*64kHz$ |   |   |   |   |   | 0010_1111  |

### Output 11 Frequency Configuration Register [14:8]

| Register (Abbrev): out11_freq_cfg[14:8]<br>Address: 0x37A<br>Type: RW<br>Default Value: 0000_0000 |                   |  |   |   |   |                  |   |            |
|---|-------------------|--|---|---|---|------------------|---|------------|
| 7   | 6                 | 5  | 4 | 3 | 2 | 1                | 0 |            |
| reserved  | out_div_cfg[14:8] |  |   |   |   | out_div_cfg[9:8] |   |            |
| Bit   | Name              | Description  |   |   |   |                  |   | Def. Value |
| 7   | reserved          | reserved   |   |   |   |                  |   | 0          |
| 6:2   | out_div_cfg[14:8] | M. Out divider ratio config, actual ratio is M+1<br>$f_{out}=f_{clk\_sdm}/(M+1)$<br>here, $f_{clk\_sdm}=N*64kHz$ |   |   |   |                  |   | 000_00     |
| 1:0   | out_div_cfg[9:8]  |  |   |   |   |                  |   | 00         |

### Output Frame/Multi-Frame Sync Configuration Register

| Register (Abbrev): fr_mfr_path_cfg<br>Address: 0x37E<br>Type: RW<br>Default Value: 0000_0000 |             |   |   |        |             |         |              |            |
|--|-------------|---|---|--------|-------------|---------|--------------|------------|
| 7  | 6           | 5   | 4 | 3      | 2           | 1       | 0            |            |
| reserved   |             |   |   | fr_pdn | fr_path_sel | mfr_pdn | mfr_path_sel |            |
| Bit  | Name        | Description   |   |        |             |         |              | Def. Value |
| 7:4  | reserved    | reserved  |   |        |             |         |              | 0000       |
| 3  | fr_pdn      | 0: frsync_8k output active<br>1: frsync_8k output power down to 0 |   |        |             |         |              | 0          |
| 2  | fr_path_sel | 0: frsync_8k_1pps from DPLL1<br>1: reserved                       |   |        |             |         |              | 0          |

Output Frame/Multi-Frame Sync Configuration Register

|  |              |   |   |   |   |   |   |
|--|--------------|---|---|---|---|---|---|
| Register (Abbrev): fr_mfr_path_cfg<br>Address: 0x37E<br>Type: RW<br>Default Value: 0000_0000 |              |   |   |   |   |   |   |
| 7  | 6            | 5 | 4   | 3 | 2 | 1 | 0 |
| 1  | mfr_pdn      |   | 0: mfrsync_2k output active<br>1: mfrsync_2k output power down to 0 |   |   |   | 0 |
| 0  | mfr_path_sel |   | 0: mfrsync_2k_1pps from DPLL1<br>1: reserved                        |   |   |   | 0 |

6.2 Power-Down Registers

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x380<br>Type: RW<br>Default Value: 0000_0000 |          |             |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
|   |          |             |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   | Def. Value |
| 7:0   | Reserved | Reserved    |   |   |   |   | 0000       |

Soft Reset Register

| Register (Abbrev): soft_rst<br>Address: 0x381<br>Type: RW<br>Default Value: 0001_0110 |          |  |          |          |          |          |            |
|---|----------|--|----------|----------|----------|----------|------------|
| 7   | 6        | 5  | 4        | 3        | 2        | 1        | 0          |
| soft_rst  | reserved |  | reserved | reserved | reserved | reserved | reserved   |
| Bit   | Name     | Description  |          |          |          |          | Def. Value |
| 7   | soft_rst | A soft reset is required to ensure the APLLs recalibrate based on the registers values loaded at boot time from the EEPROM. The soft reset will perform the same functions as a hard reset with the exception of reverting the register values to the default values and re-sampling the bootstrap pins. The soft reset should be performed following each power up sequence. The soft-rst bit is self clearing. |          |          |          |          | 0          |
| 6:5   | reserved | reserved   |          |          |          |          | 00         |
| 4   | reserved | reserved   |          |          |          |          | 00         |
| 3   | reserved | reserved   |          |          |          |          | 00         |
| 2   | reserved | reserved   |          |          |          |          | 00         |
| 1   | reserved | reserved   |          |          |          |          | 00         |

### Soft Reset Register

|   |          |   |          |   |   |    |   |
|---|----------|---|----------|---|---|----|---|
| Register (Abbrev): soft_rst<br>Address: 0x381<br>Type: RW<br>Default Value: 0001_0110 |          |   |          |   |   |    |   |
| 7   | 6        | 5 | 4        | 3 | 2 | 1  | 0 |
| 0   | reserved |   | reserved |   |   | 00 |   |

### Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x382<br>Type: RW<br>Default Value: 0000_0000 |           |   |   |   |   |   |            |
|---|-----------|---|---|---|---|---|------------|
| 7   | 6         | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |           |   |   |   |   |   | ms_invert  |
| Bit   | Name      | Description   |   |   |   |   | Def. Value |
| 7:1   | reserved  | reserved  |   |   |   |   | 0000_000   |
| 0   | ms_invert | 0: MS_SL pin used as is<br>1: MS_SL pin is inverted before used |   |   |   |   | 0          |

### Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x383<br>Type: RW<br>Default Value: 1000_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only: the EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 1000_0000  |



Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x384<br>Type: RW<br>Default Value: 0010_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only: the EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0010_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x385, 0x386, 0x387<br>Type: RO<br>Default Value: 0010_0000 |          |             |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |             |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   | Def. Value |
| 7:0   | reserved | reserved    |   |   |   |   | 0010_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x388, 0x389, 0x38A<br>Type: RW<br>Default Value: 0010_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0010_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x38B, 0x38C, 0x38D<br>Type: RW<br>Default Value: 0000_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x38E<br>Type: RW<br>Default Value: 0000_0100 |          |             |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |             |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   | Def. Value |
| 7:0   | reserved | reserved    |   |   |   |   | 0000_0100  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x38F<br>Type: RW<br>Default Value: 0001_0000 |          |             |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |             |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   | Def. Value |
| 7:0   | reserved | reserved    |   |   |   |   | 0001_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x390<br>Type: RW<br>Default Value: 1110_0101 |          |             |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |             |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   | Def. Value |
| 7:0   | reserved | reserved    |   |   |   |   | 1110_0101  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x391<br>Type: RW<br>Default Value: 0000_0111 |          |             |   |   |   |   |            |
|---|----------|-------------|---|---|---|---|------------|
| 7   | 6        | 5           | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |             |   |   |   |   |            |
| Bit   | Name     | Description |   |   |   |   | Def. Value |
| 7:0   | reserved | reserved    |   |   |   |   | 0000_0111  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x392, 0x393<br>Type: RW<br>Default Value: 0000_0000 |          |   |   |   |   |   |            |
|--|----------|---|---|---|---|---|------------|
| 7  | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved   |          |   |   |   |   |   |            |
| Bit  | Name     | Description   |   |   |   |   | Def. Value |
| 7:0  | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x394<br>Type: RW<br>Default Value: 0000_0011 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0011  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x395<br>Type: RW<br>Default Value: 1010_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 1010_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x396<br>Type: RW<br>Default Value: 0000_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0000  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x397<br>Type: RW<br>Default Value: 1100_0001 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 1100_0001  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x398<br>Type: RW<br>Default Value: 0000_0010 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0010  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x399<br>Type: RW<br>Default Value: 0100_0011 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0100_0011  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x39A<br>Type: RW<br>Default Value: 0000_0011 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0011  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x39B<br>Type: RW<br>Default Value: 0000_0100 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0100  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x39C<br>Type: RW<br>Default Value: 0000_0011 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0000_0011  |

Reserved Register

| Register (Abbrev): rsvd<br>Address: 0x39D<br>Type: RW<br>Default Value: 0101_0000 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   |            |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:0   | reserved | EEPROM only. The EEPROM at this address must contain the value shown in the "Default Value" column. |   |   |   |   | 0101_0000  |

EEPROM CRC Register

| Register (Abbrev): eeprom_crc<br>Address: 0x39E<br>Type: RW<br>Default Value: N/A |          |  |   |   |   |   |            |
|---|----------|--|---|---|---|---|------------|
| 7   | 6        | 5  | 4 | 3 | 2 | 1 | 0          |
| crc[7:0]  |          |  |   |   |   |   |            |
| Bit   | Name     | Description  |   |   |   |   | Def. Value |
| 7:0   | crc[7:0] | EEPROM only. Must contain the CRC8 value of all EEPROM data from x000 to x39D. |   |   |   |   | N/A        |

## 7 APLL3 Register Map (82P33731 only)

Table 2: APLL3 Register Map

| Address                  | Register (Abbrev)                    | Register Name                       |
|--------------------------|--------------------------------------|-------------------------------------|
| Global Control Registers |                                      |                                     |
| 0x00                     | control                              | Register Configuration Select       |
| 0x01                     | clk_sel                              | Input Clock Select                  |
| 0x0E                     | fsel                                 | Crystal Select                      |
| 0x0F                     | out{11:12}_config – Starting address | Output{11:12} Configuration         |
| Configuration Registers  |                                      |                                     |
| 0x02                     | pd0_sel[7:0] – Starting address      | Pre-divider{0:1} Select             |
| 0x03                     | pd0_sel[14:8] – Starting address     | Pre-divider{0:1} Select             |
| 0x06                     | m0[7:0] – Starting address           | Feedback Divider{0:1}               |
| 0x07                     | m0[14:8] – Starting address          | Feedback Divider{0:1}               |
| 0x0A                     | OUT11_odsel0 – Starting address      | OUT11 Output Divider Selection{0:1} |
| 0x0C                     | OUT12_odsel0 – Starting address      | OUT12 Output Divider Selection{0:1} |

### 7.1 Global Control Registers

#### Register Configuration Select

| Register (Abbrev): control<br>Address: 0x00<br>Type: RW<br>Default Value: 0000_0000 |          |  |   |   |   |        |            |
|---|----------|--|---|---|---|--------|------------|
| 7   | 6        | 5  | 4 | 3 | 2 | 1      | 0          |
| reserved  |          |  |   |   |   | config | reserved   |
| Bit   | Name     | Description  |   |   |   |        | Def. Value |
| 7:2   | reserved | reserved   |   |   |   |        | 0000_00    |
| 1   | config   | This bit selects which of 2 register configurations is used.<br>0: Configuration 0<br>1: Configuration 1 |   |   |   |        | 0          |
| 0   | reserved | reserved   |   |   |   |        | 0          |



Input Clock Select

| Register (Abbrev): clk_sel<br>Address: 0x01<br>Type: RW<br>Default Value: 0000_0001 |          |   |   |   |   |   |            |
|---|----------|---|---|---|---|---|------------|
| 7   | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved  |          |   |   |   |   |   | clk_sel    |
| Bit   | Name     | Description   |   |   |   |   | Def. Value |
| 7:1   | reserved | reserved  |   |   |   |   | 0000_000   |
| 0   | clk_sel  | This bit selects which input is used.<br>0: External<br>1: Internal (default) |   |   |   |   | 1          |

Crystal Select

| Register (Abbrev): fsel<br>Address: 0x0E<br>Type: RW<br>Default Value: 0000_0000 |          |   |   |   |   |   |            |
|--|----------|---|---|---|---|---|------------|
| 7  | 6        | 5   | 4 | 3 | 2 | 1 | 0          |
| reserved   |          |   |   |   |   |   | fsel       |
| Bit  | Name     | Description   |   |   |   |   | Def. Value |
| 7:1  | reserved | reserved  |   |   |   |   | 0000_000   |
| 0  | fsel     | This bit selects the reference XTAL used by VCXO.<br>0: XTAL1 (default)<br>1: XTAL2 |   |   |   |   | 0          |

Output{11:12} Configuration

| Register (Abbrev): out{11:12}_config<br>Address: 0x0F, 0x10<br>Type: RW<br>Default Value: 0000_0000 |                      |  |   |   |   |                      |                   |
|---|----------------------|--|---|---|---|----------------------|-------------------|
| 7   | 6                    | 5  | 4 | 3 | 2 | 1                    | 0                 |
| reserved  |                      |  |   |   |   | out{11:12}_pecl_lvds | out{11:12}_enable |
| Bit   | Name                 | Description  |   |   |   |                      | Def. Value        |
| 7:2   | reserved             | reserved   |   |   |   |                      | 0000_000          |
| 1   | out{11:12}_pecl_lvds | This bit selects output {11:12} output signal configuration.<br>0: LVPECL (default)<br>1: LVDS |   |   |   |                      | 0                 |

### Output{11:12} Configuration

|   |                   |   |   |   |   |   |   |
|---|-------------------|---|---|---|---|---|---|
| Register (Abbrev): out{11:12}_config<br>Address: 0x0F, 0x10<br>Type: RW<br>Default Value: 0000_0000 |                   |   |   |   |   |   |   |
| 7   | 6                 | 5 | 4   | 3 | 2 | 1 | 0 |
| 0   | out{11:12}_enable |   | This bit selects output {11:12} output enable.<br>0: Disable (default)<br>1: Enable |   |   |   | 0 |

## 7.2 Configuration Registers

### Pre-divider{0:1} Select

| Register (Abbrev): pd{0:1}_sel<br>Address: 0x02, 0x04, 0x03, 0x05<br>Type: RW<br>Default Value: 0000_1100_0011_0101 |                   |   |   |   |   |   |            |
|---|-------------------|---|---|---|---|---|------------|
| 7   | 6                 | 5   | 4 | 3 | 2 | 1 | 0          |
| pd0_sel[7:0]  |                   |   |   |   |   |   |            |
| reserved  | pd0_sel[14:0]     |   |   |   |   |   |            |
| Bit   | Name              | Description   |   |   |   |   | Def. Value |
| 7:0   | pd{0:1}_sel[7:0]  | The PDSEL0[14:0] bits represent a unsigned integer for the APLL pre-divider value for configuration 0.<br>These bits must always be programed to 000 0000 0000 0100 (/4) or higher, except for /1 where they can be programmed to 000 0000 0000 0001.<br>The default value of 0xC35 represents /3125. |   |   |   |   | 0011_0101  |
| 7   | reserved          | reserved  |   |   |   |   | 0          |
| 6:0   | pd{0:1}_sel[14:8] | The PDSEL0[14:0] bits represent a unsigned integer for the APLL pre-divider value for configuration 0.<br>These bits must always be programed to 000 0000 0000 0100 (/4) or higher, except for /1 where they can be programmed to 000 0000 0000 0001.<br>The default value of 0xC35 represents /3125. |   |   |   |   | 000_1100   |

### Feedback Divider{0:1}

|  |          |   |   |   |   |   |   |
|--|----------|---|---|---|---|---|---|
| Register (Abbrev): m{0:1}<br>Address: 0x06, 0x08, 0x07, 0x09<br>Type: RW<br>Default Value: 0000_1100_0011_0101 |          |   |   |   |   |   |   |
| 7  | 6        | 5 | 4 | 3 | 2 | 1 | 0 |
| m0[7:0]  |          |   |   |   |   |   |   |
| reserved   | m0[14:0] |   |   |   |   |   |   |

**Feedback Divider{0:1}**

| Register (Abbrev): m{0:1}<br>Address: 0x06, 0x08, 0x07, 0x09<br>Type: RW<br>Default Value: 0000_1100_0011_0101 |              |   |   |   |   |   |            |
|--|--------------|---|---|---|---|---|------------|
| 7  | 6            | 5   | 4 | 3 | 2 | 1 | 0          |
| Bit  | Name         | Description   |   |   |   |   | Def. Value |
| 7:0  | m{0:1}[7:0]  | The M0[15:0] bits represent a unsigned integer for the APLL feedback divider value for configuration 0.<br>These bits must always be programed to 000 0000 0000 0101 (/5) or higher.<br>The default value of C35H represents /3125. |   |   |   |   | 0011_0101  |
| 7  | reserved     | reserved  |   |   |   |   | 0          |
| 6:0  | m{0:1}[14:8] | The M0[15:0] bits represent a unsigned integer for the APLL feedback divider value for configuration 0.<br>These bits must always be programed to 000 0000 0000 0101 (/5) or higher.<br>The default value of C35H represents /3125. |   |   |   |   | 000_1100   |

**OUT11 Output Divider Selection{0:1}**

| Register (Abbrev): out11_odsel{0:1}<br>Address: 0x0A, 0x0B<br>Type: RW<br>Default Value: 0000_0000 |                  |   |   |   |                  |   |            |
|--|------------------|---|---|---|------------------|---|------------|
| 7  | 6                | 5   | 4 | 3 | 2                | 1 | 0          |
| reserved   |                  |   |   |   | out11_odsel[2:0] |   |            |
| Bit  | Name             | Description   |   |   |                  |   | Def. Value |
| 7:3  | reserved         | reserved  |   |   |                  |   | 0000_0     |
| 2:0  | out11_odsel{0:1} | The OUT11_ODSEL{0:1} bits represent an output divider value for OUT11 for configuration 0.<br>000: Divide by 25 (default)<br>001: Divide by 5<br>010: Divide by 4<br>011: Divide by 2<br>1XX: Divide by 1 |   |   |                  |   | 000        |

### OUT12 Output Divider Selection{0:1}

| Register (Abbrev): out12_odsel{0:1}<br>Address: 0x0C, 0x0D<br>Type: RW<br>Default Value: 0000_0000 |                  |  |   |                   |   |   |            |
|--|------------------|--|---|-------------------|---|---|------------|
| 7  | 6                | 5  | 4 | 3                 | 2 | 1 | 0          |
| reserved   |                  |  |   | out12_odsel0[2:0] |   |   |            |
| Bit  | Name             | Description  |   |                   |   |   | Def. Value |
| 7:3  | reserved         | reserved   |   |                   |   |   | 0000_0     |
| 2:0  | out12_odsel{0:1} | The OUT12_ODSEL{0:1} bits represent an output divider value for OUT12 for configuration 0.<br>000: Divide by 8 (default)<br>001: Divide by 5<br>010: Divide by 4<br>011: Divide by 2<br>1XX: Divide by 1 |   |                   |   |   | 000        |

## 8 82P337xx I/O Mapping

| Type | Register Map | 82P33731 | 82P33714 |
|------|--------------|----------|----------|
| AMI  | IN01         | IN01     |          |
|      | IN02         | IN02     |          |
| DIFF | IN03         | IN03     | IN01     |
|      | IN04         | IN04     | IN02     |
|      | IN05         | IN05     | IN03     |
|      | IN06         | IN06     | IN04     |
|      | IN07         | IN07     |          |
|      | IN08         | IN08     |          |
| CMOS | IN09         | IN09     | IN05     |
|      | IN10         | IN10     | IN06     |
|      | IN11         | IN11     |          |
|      | IN12         | IN12     |          |
|      | IN13         | IN13     |          |
|      | IN14         | IN14     |          |

|             | Type | Register Map | 82P33731 | 82P33714 |
|-------------|------|--------------|----------|----------|
| DPLL1/APLL1 | CMOS | OUT01        | OUT01    | OUT01    |
|             |      | OUT02        | OUT02    | OUT02    |
| APLL1       | DIFF | OUT03        | OUT03    | OUT03    |
|             |      | OUT04        | OUT04    | OUT04    |
| OUT05       |      | OUT05        | OUT05    |          |
| OUT06       |      | OUT06        | OUT06    |          |
| APLL2       | CMOS | OUT07        | OUT07    | OUT07    |
|             |      | OUT08        |          | OUT08    |
| DPLL1/APLL2 | AMI  | OUT09        | OUT08    |          |
| DPLL2       | CMOS | OUT10        | OUT09    | OUT09    |
|             |      | OUT11        | OUT10    | OUT10    |
| APLL3       | DIFF | OUT12        | OUT11    |          |
|             |      | OUT13        | OUT12    |          |



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